Ordering number : EN*5223

CMOS LSI

LC78621E

Compact Disc Player DSP

Preliminary

Overview

The LC78621E is a CMOS LSI that implements the signal processing and servo control required by compact disk players, laser disks, CD-V, CD-I and related products. The LC78621E provides several types of signal processing, including demodulation of the optical pickup EFM signal, de-interleaving, error detection and correction, and digital filters that can help reduce the cost of CD player units. It also processes a rich set of servo system commands sent from the control microprocessor. It also incorporates an EFM-PLL circuit and a one-bit D/A converter.

Functions

- Input signal processing: The LC78621E takes an HF signal as input, digitizes (slices) that signal at a precise level, converts that signal to an EFM signal, and generates a PLL clock with an average frequency of 4.3218 MHz by comparing the phases of that signal and an internal VCO.
- Precise reference clock and necessary internal timing generation using an external 16.9344 MHz crystal oscillator
- Disk motor speed control using a frame phase difference signal generated from the playback clock and the reference clock
- Frame synchronization signal detection, protection and interpolation to assure stable data readout
- EFM signal demodulation and conversion to 8-bit symbol data
- Subcode data separation from the EFM demodulated signal and output of that data to an external microprocessor
- Subcode Q signal output to a microprocessor over the serial I/O interface after performing a CRC error check
- Demodulated EFM signal buffering in internal RAM to handle up to ±4 frames of disk rotational jitter
- Demodulated EFM signal reordering in the prescribed order for data unscrambling and de-interleaving
- Error detection, correction, and flag processing (error correction scheme: dual C1 plus dual C2 correction)
- The LC78620E sets the C2 flags based on the C1 flags and a C2 check, and then performs signal interpolation or muting depending on the C2 flags. The interpolation circuit uses a quadruple interpolation scheme. The output value converges to the muting level when four or more consecutive C2 flags occur.
- Support for command input from a control microprocessor: commands include track jump, focus start, disk motor start/stop, muting on/off and track count (8 bit serial input)
- Built-in digital output circuits.
- Arbitrary track counting to support high-speed data access
- Zero cross muting
- Supports the implementation of a double-speed dubbing function.
- D/A converter outputs with data continuity improved by 8× oversampling digital filters. (These filters function as 4× oversampling filters during double-speed playback.)
- Built-in third-order ∑Δ D/A converters (PWM output)
- Built-in digital attenuator (8 bits – alpha, 239 steps)
- Built-in digital de-emphasis
- Built-in digital level and peak meter functions
- Support for bilingual applications

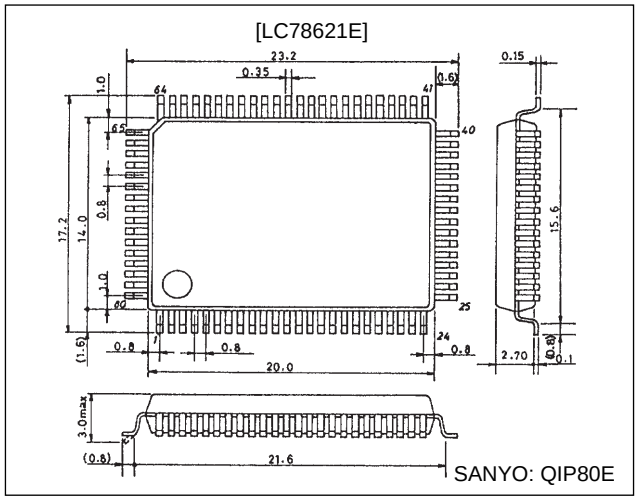
Features

- 80-pin QIP (miniature, reduced space package)
- Silicon gate CMOS process (for low power)
- 5 V single-voltage power supply (for use in portable products)

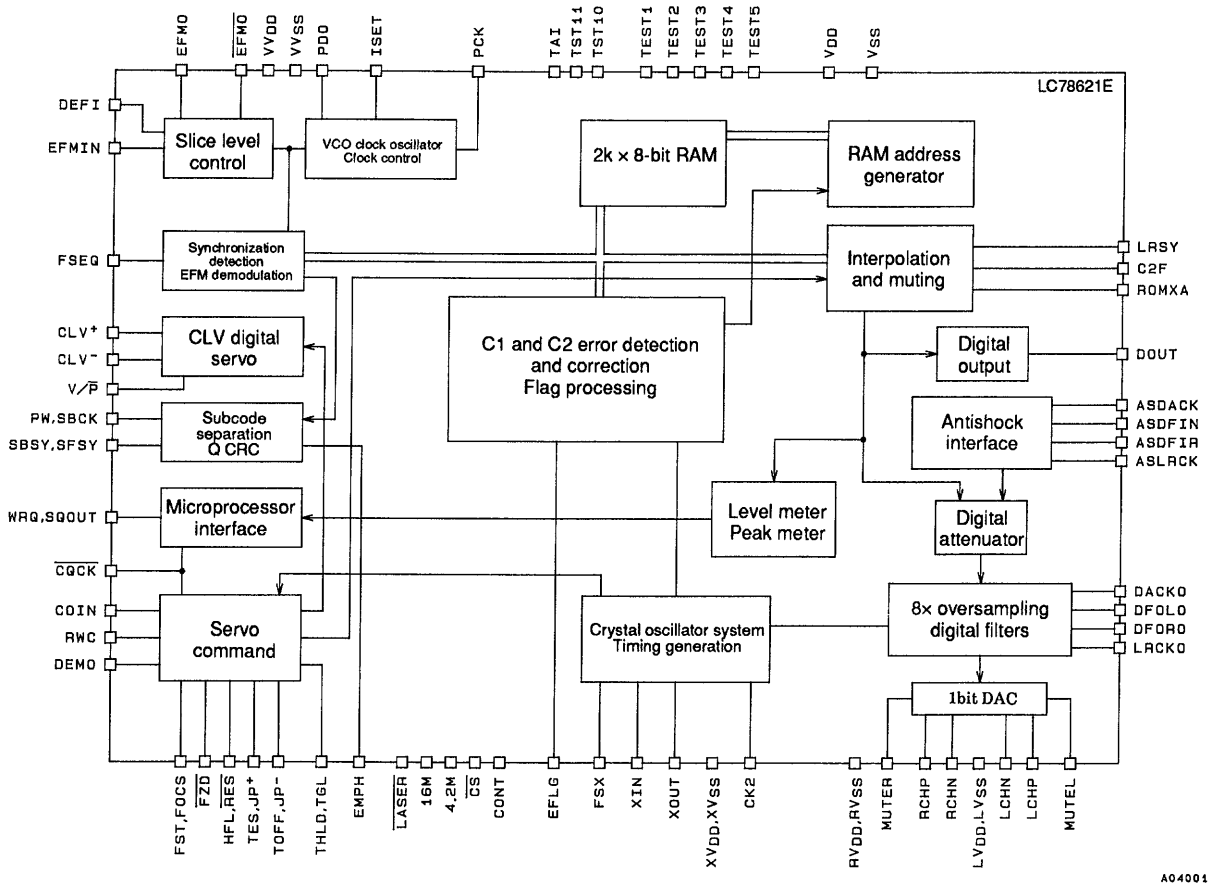
Package Dimensions

unit: mm

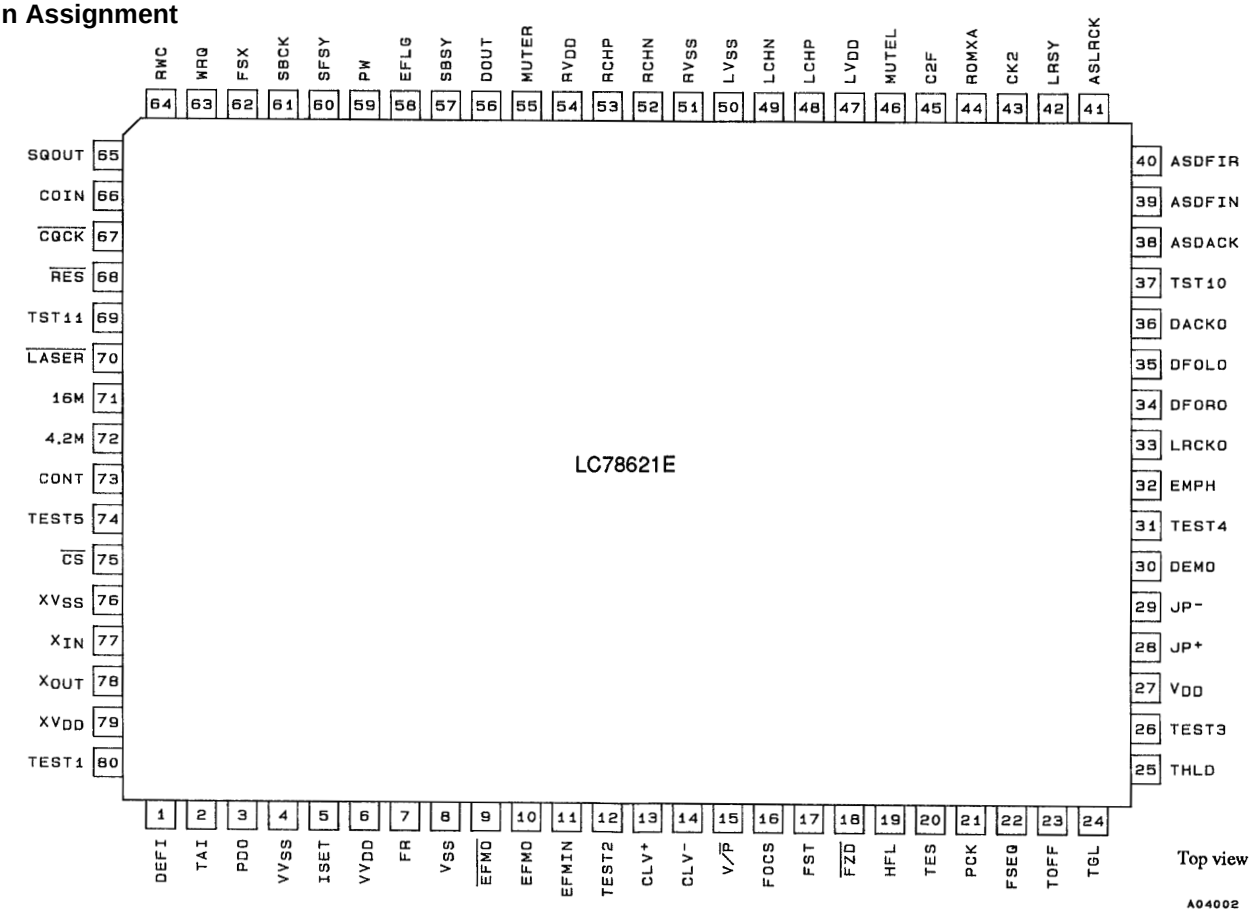
3174-QFP80E



Equivalent Circuit Block Diagram



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}, XV_{DD}, LV_{DD}, RV_{DD}, VV_{DD}	3.6		5.5	V
Input high-level voltage	V_{IH} (1)	DEFI, $\overline{FZD}$, ASDACK, ASDFIN, ASDFIR, ASLRCK, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$, TAI, TEST1 to TEST5, DEMO, $\overline{CS}$	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	EFMIN	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL} (1)	DEFI, $\overline{FZD}$, ASDACK, ASDFIN, ASDFIR, ASLRCK, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$, TAI, TEST1 to TEST5, DEMO, $\overline{CS}$	0		0.3 V_{DD}	V
	V_{IL} (2)	EFMIN	0		0.4 V_{DD}	V
Data setup time	$t_{set\ up}$	COIN, RWC: Figure 1	400			ns
Data hold time	t_{hold}	COIN, RWC: Figure 1	400			ns
High-level clock pulse width	$t_{WøH}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Low-level clock pulse width	$t_{WøL}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Data read access time	t_{RAC}	SQOUT, PW: Figures 2 and 3	0		400	ns
Command transfer time	t_{RWC}	RWC: Figure 1	1000			ns
Subcode Q read enable time	t_{SQE}	WRQ: Figure 2, with no RWC signal		11.2		ms
Subcode read cycle	t_{sc}	SFSY: Figure 3		136		µs
Subcode read enable time	t_{se}	SFSY: Figure 3	400			ns
Input level	V_{IN} (1)	EFMIN	1.0			Vp-p
	V_{IN} (2)	X_{IN}: Input capacitor coupled	1.0			Vp-p
Operating frequency range	fop	EFMIN			10	MHz
Crystal oscillator frequency	fX (1)	X_{IN}, X_{OUT}: In 16M mode		16.9344		MHz
	fX (2)	X_{IN}, X_{OUT}: In 32M mode		33.8688		MHz

Note: Due to the structure of this LSI, an identical voltage must be supplied to all the power supply pins.

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{DD}			30	45	mA
Input high-level current	I_{IH} (1)	DEFI, EFMIN, $\overline{FZD}$, ASDACK, ASDFIN, ASDFIR, ASLRCK, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$: V_{IN} = 5 V			5	µA
	I_{IH} (2)	TAI, TEST1 to TEST5, DEMO, $\overline{CS}$: V_{IN} = V_{DD} = 5.5 V	25		75	µA
Input low-level current	I_{IL}	DEFI, EFMIN, $\overline{FZD}$, ASDACK, ASDFIN, ASDFIR, ASLRCK, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$, TAI, TEST1 to TEST5, DEMO, $\overline{CS}$: V_{IN} = 0 V	–5			µA
Output high-level voltage	V_{OH} (1)	$\overline{EFMO}$, EFMO, CLV^+, CLV^-, V/$\overline{P}$, FOCS, PCK, FSEQ, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX: I_{OH} = –1 mA	4			V
	V_{OH} (2)	MUTEL, MUTER, LRCKO, DFORO, DFOLO, DACKO, TST10, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, TST11, 16M, 4.2M, CONT: I_{OH} = –0.5 mA	4			V
	V_{OH} (3)	$\overline{LASER}$: I_{OH} = –1 mA	4.6			V
	V_{OH} (4)	DOUT: I_{OH} = –12 mA	4.5			V
	V_{OH} (5)	LCHP, RCHP, LCHN, RCHN: I_{OH} = –1mA	3.0		4.5	V

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Parameter	Symbol	Conditions	min	typ	max	Unit
Output low-level voltage	V_{OL} (1)	$\overline{EFMO}$, EFMO, CLV+, CLV–, V/$\overline{P}$, FOCS, PCK, FSEQ, TOFF, TGL, THLD, JP+, JP–, EMPH, EFLG, FSX: I_{OL} = 1 mA			1	V
	V_{OL} (2)	MUTEL, MUTER, LRCKO, DFORO, DFOLO, DACKO, TST10, LRSY, CK2, ROMXA, C2F, SBSY, PW, $\overline{SFSY}$, WRQ, SQOUT, TST11, 16M, 4.2M, CONT, $\overline{LASER}$: I_{OL} = 2 mA			0.4	V
	V_{OL} (3)	DOUT: I_{OL} = 12 mA			0.5	V
	V_{OL} (4)	FST: I_{OL} = 5 mA			0.75	V
	V_{OL} (5)	LCHP, RCHP, LCHN, RCHN: I_{OL} = 1mA	0.5		2.0	V
Output off leakage current	I_{OFF} (1)	PDO, CLV+, CLV–, JP+, JP–, FST: V_{OUT} = 5 V			5	µA
	I_{OFF} (2)	PDO, CLV+, CLV–, JP+, JP–: V_{OUT} = 0 V	–5			µA
Charge pump output current	I_{PDOH}	PDO: R_{ISET} = 68 kΩ	100	125	150	µA
	I_{PDOL}	PDO: R_{ISET} = 68 kΩ	–150	–125	–100	µA

Note: For guaranteed operation, the VCO oscillator frequency range adjustment resistor FR must be a 1.20 kΩ (±5.0%) tolerance resistor.

One-Bit D/A Converter Analog Characteristics

at Ta = 25°C, V_{DD} = LV_{DD} = RV_{DD} = 5 V, V_{SS} = LV_{SS} = RV_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Total harmonic distortion	THD + N	LCHP, RCHP, LCHN, RCHN; 1 kHz: 0 dB data input, using the 20 kHz low-pass filter (AD725D built in)		0.008	0.010	%
Dynamic range	DR	LCHP, RCHP, LCHN, RCHN; 1 kHz: –60 dB data input, using the 20 kHz low-pass filter and the A filter (AD725D built in)	84	88		dB
Signal-to-noise ratio	S/N	LCHP, RCHP, LCHN, RCHN; 1 kHz: 0 dB data input, using the 20 kHz low-pass filter and the A filter (AD725D built in)	98	100		dB
Crosstalk	CT	LCHP, RCHP, LCHN, RCHN; 1 kHz: 0 dB data input, using the 20 kHz low-pass filter (AD725D built in)	96	98		dB

Note: Measured with the normal-speed playback mode in the Sanyo one-bit D/A converter block reference digital attenuator circuit set to EE (hexadecimal).

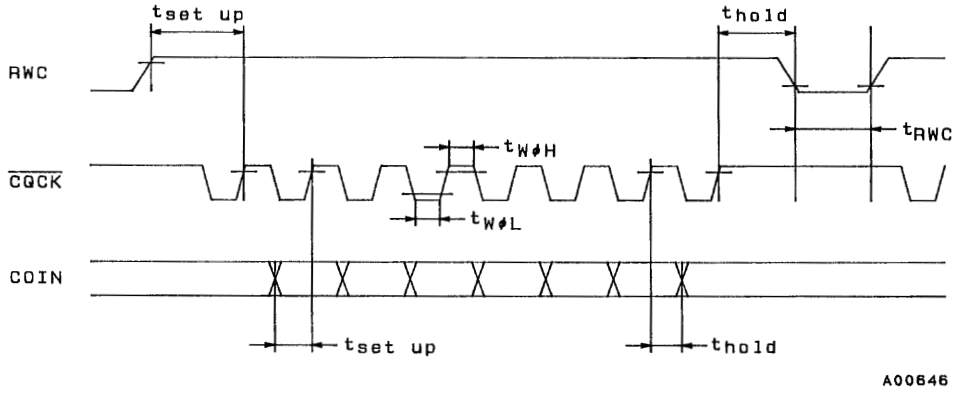


Figure 1 Command Input

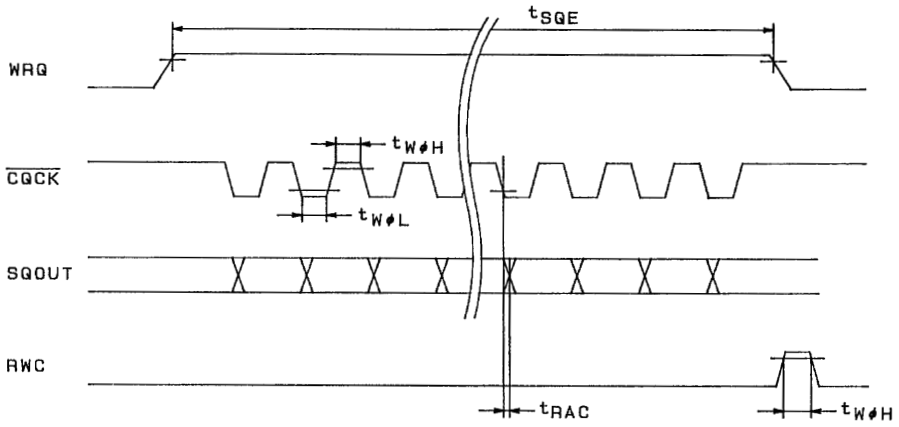
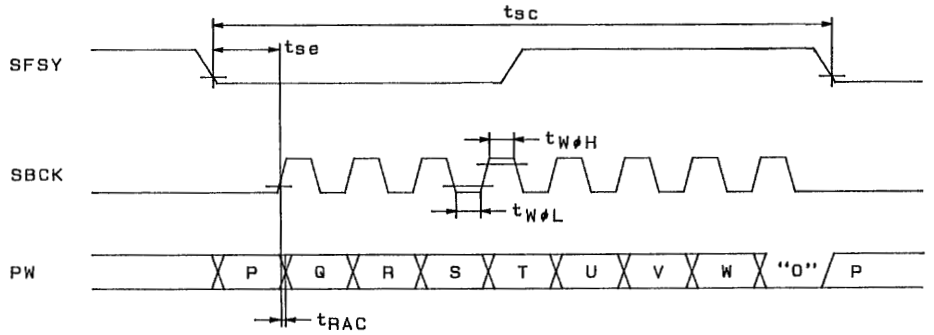


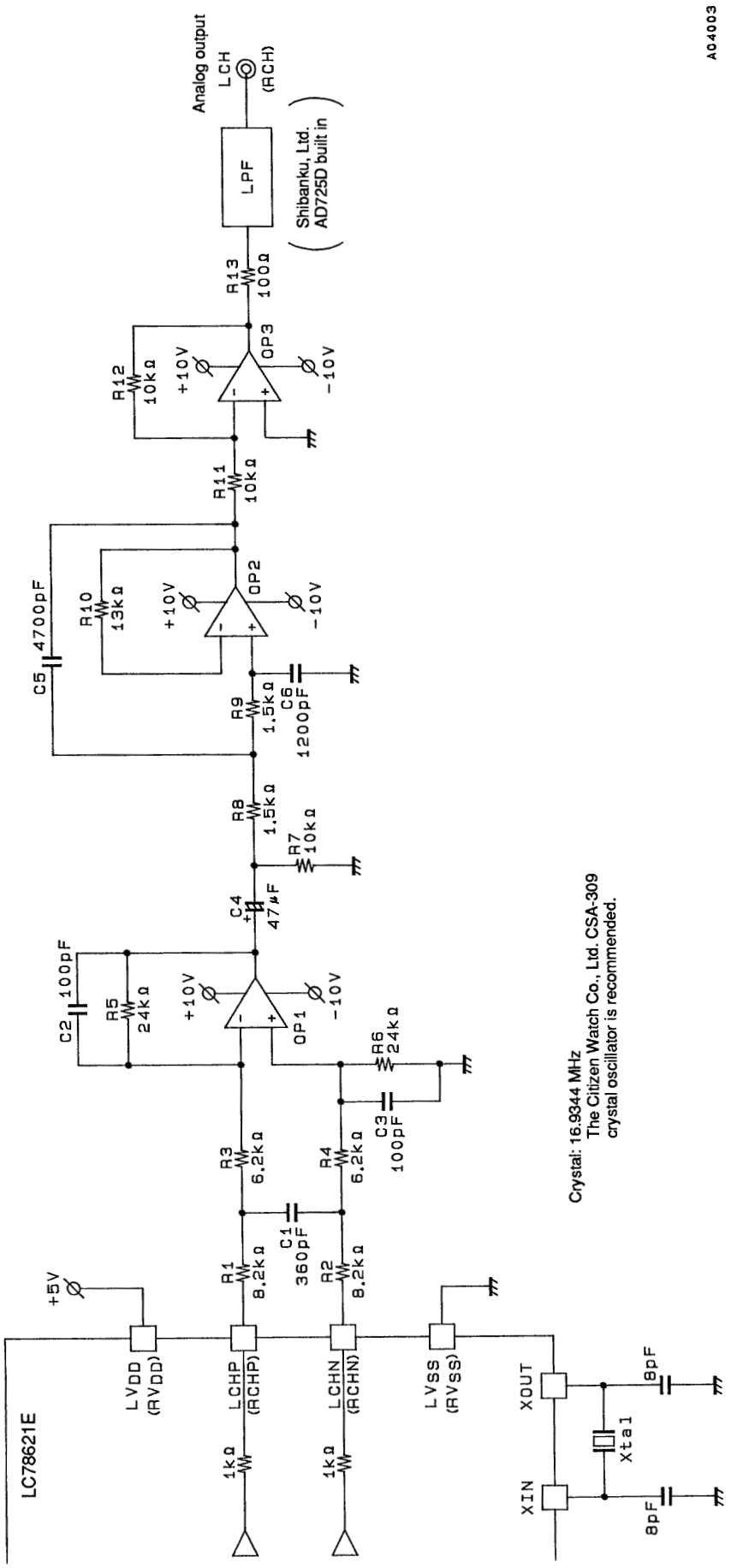
Figure 2 Subcode Q Output A01439



A04134

Figure 3 Subcode Output

One-Bit D/A Converter Output Block Reference Circuit (normal speed playback)



Pin Functions

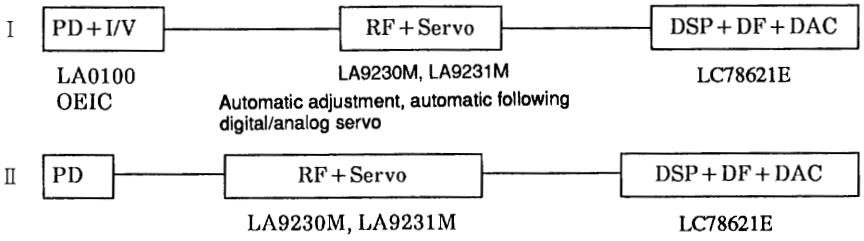
Pin No.	Symbol	I/O	Function	
1	DEFI	I	Defect detection signal (DEF) input (Must be tied low if unused.)	
2	TAI	I	PLL pins	Test input. A pull-down resistor is built in.
3	PDO	O		External VCO control phase comparator output
4	VV_{SS}			Internal VCO ground. Normally 0 V.
5	ISET	AI		PDO output current adjustment resistor connection
6	VV_{DD}			Internal VCO power supply.
7	FR	AI		VCO frequency range adjustment
8	V_{SS}		Digital system ground. Normally 0 V.	
9	$\overline{EFMO}$	O	Slice level control	EFM signal inverted output
10	EFMO	O		EFM signal output
11	EFMIN	I		EFM signal input
12	TEST2	I	Test input. A pull-down resistor is built in.	
13	CLV^+	O	Spindle servo control output. Acceleration when CLV^+ is high, deceleration when CLV^- is high	
14	CLV^-	O	Three-value output is also possible when specified by microprocessor command.	
15	$V/\overline{P}$	O	Rough servo/phase control automatic switching monitor output. Outputs a high level during rough servo and a low level during phase control.	
16	FOCS	O	Focus servo on/off output. Focus servo is on when the output is low.	
17	FST	O	Focus start pulse output. This is an open-drain output.	
18	$\overline{FZD}$	I	Focus error zero cross signal input. (Must be tied low if unused.)	
19	HFL	I	Track detection signal input. This is a Schmitt input.	
20	TES	I	Tracking error signal input. This is a Schmitt input.	
21	PCK	O	EFM data playback clock monitor. Outputs 4.3218 MHz when the phase is locked.	
22	FSEQ	O	Synchronization signal detection output. Outputs a high level when the synchronization signal detected from the EFM signal and the internally generated synchronization signal agree.	
23	TOFF	O	Tracking off output	
24	TGL	O	Tracking gain switching output. Increase the gain when low.	
25	THLD	O	Tracking hold output	
26	TEST3	I	Test input. A pull-down resistor is built in.	
27	V_{DD}		Digital system power supply.	
28	JP^+	O	Track jump output. A high level output from JP^+ indicates acceleration during an outward jump or deceleration during an inward jump. A high level output from JP^- indicates acceleration during an inward jump or deceleration during an outward jump. Three-value output is also possible when specified by microprocessor command.	
29	JP^-	O		
30	DEMO	I	Sound output function input used for end product adjustment manufacturing steps. A pull-down resistor is built in.	
31	TEST4	I	Test input. A pull-down resistor is built in.	
32	EMPH	O	De-emphasis monitor pin. A high level indicates playback of a de-emphasis disk.	
33	LRCKO	O	Digital filter outputs	Word clock output
34	DFORO	O		Right channel data output
35	DFOLO	O		Left channel data output
36	DACKO	O		Bit clock output
37	TST10	O	Test output. Leave open. (Normally outputs a low level.)	
38	ASDACK	I	Anti-shock system inputs (Must be tied low if unused.)	Bit clock input
39	ASDFIN	I		Left/right channel data input
40	ASDFIR	I		Test input. (Should be tied low for normal operation.)
41	ASLRCK	I		Word clock input

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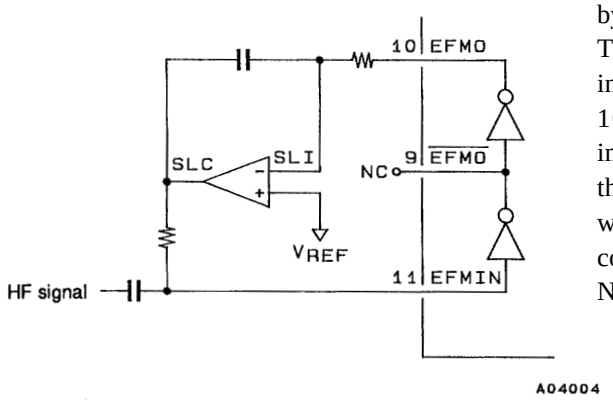
Pin No.	Symbol	I/O	Function		
42	LRSY	O	ROMXA application output signals	Left/right clock output	
43	CK2	O		Bit clock output (after reset)	Inverted polarity clock output (during CK2CON mode)
44	ROMXA	O		Interpolation data output (after reset)	ROM data output (During ROMXA mode)
45	C2F	O		C2 flag output	
46	MUTEL	O	One-bit D/A converter	Left channel mute output	
47	LV_{DD}			Left channel power supply.	
48	LCHP	O		Left channel P output	
49	LCHN	O		Left channel N output	
50	LV_{SS}			Left channel ground. Normally 0 V.	
51	RV_{SS}			Right channel ground. Normally 0 V.	
52	RCHN	O		Right channel N output	
53	RCHP	O		Right channel P output	
54	RV_{DD}			Right channel power supply.	
55	MUTER	O		Right channel mute output	
56	DOUT	O	Digital output		
57	SBSY	O	Subcode block synchronization signal		
58	EFLG	O	C1, C2, single and double error correction monitor pin		
59	PW	O	Subcode P, Q, R, S, T, U, V and W output		
60	SFSY	O	Subcode frame synchronization signal output. This signal falls when the subcodes are in the standby state.		
61	SBCK	I	Subcode readout clock input. This is a Schmitt input. (Must be tied low when unused.)		
62	FSX	O	Output for the 7.35 kHz synchronization signal divided from the crystal oscillator		
63	WRQ	O	Subcode Q output standby output		
64	RWC	I	Read/write control input. This is a Schmitt input.		
65	SQOUT	O	Subcode Q output		
66	COIN	I	Command input from the control microprocessor		
67	$\overline{CQCK}$	I	Input for both the command input acquisition clock and the SQOUT pin subcode readout clock input. This is a Schmitt input.		
68	$\overline{RES}$	I	Chip reset input. This pin must be set low briefly after power is first applied.		
69	TST11	O	Test output. Leave open. (Normally outputs a low level.)		
70	$\overline{LASER}$	O	Laser on/off output. Controlled by serial data commands from the control microprocessor.		
71	16M	O	16.9344 MHz output.		
72	4.2M	O	4.2336 MHz output		
73	CONT	O	Supplementary control output. Controlled by serial data commands from the control microprocessor.		
74	TEST5	I	Test input. A pull-down resistor is built in.		
75	$\overline{CS}$	I	Chip select input. A pull-down resistor is built in.		
76	XV_{SS}		Crystal oscillator ground. Normally 0 V.		
77	X_{IN}	I	Connections for a 16.9344 MHz crystal oscillator.		
78	X_{OUT}	O			
79	XV_{DD}		Crystal oscillator power supply.		
80	TEST1	I	Test input. A pull-down resistor is built in.		

CD System Block Diagrams



Pin Applications

1. HF Signal Input Circuit; Pin 11: EFMIN, pin 10: EFMO, pin 9: $\overline{\text{EFMO}}$, pin 1: DEFI, pin 13: CLV^+

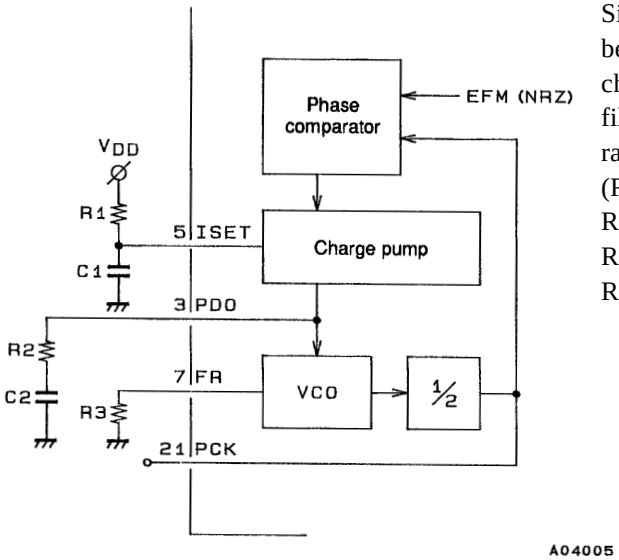


An EFM signal (NRZ) sliced at an optimal level can be acquired by inputting the HF signal to EFMIN.

The LC78621E handles defects as follows. When a high level is input to the DEFI pin (pin 1), the $\overline{\text{EFMO}}$ (pin 9) and EFMO (pin 10) pins (the slice level control outputs) go to the high-impedance state, and the slice level is held. However, note that this function is only valid in CLV phase control mode, that is, when the V/$\overline{\text{P}}$ pin (pin 15) is low. This function can be used in combination with the LA9230M and LA9231M DEF pins.

Note: If the EFMIN and CLV^+ signal lines are too close to each other, unwanted radiation can result in error rate degradation. We recommend laying a ground or V_{DD} shield line between these two lines.

2. PLL Clock Generation Circuit; Pin 3: PDO, pin 5: ISET, pin 7: FR, pin 21: PCK



Since the LC78621E includes a VCO circuit, a PLL circuit can be formed by connecting an external RC circuit. ISET is the charge pump reference current, PDO is the VCO circuit loop filter, and FR is a resistor that determines the VCO frequency range.

(Reference values)

R1 = 68 kΩ, C1 = 0.1 µF

R2 = 680 kΩ, C2 = 0.1 µF

R3 = 1.2 kΩ

3. VCO Monitor; Pin 21: PCK

PCK is a monitor pin that outputs an average frequency of 4.3218 MHz, which is divided from the VCO frequency.

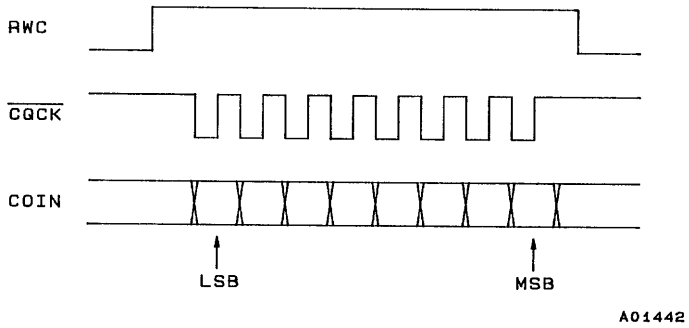
4. Synchronization Detection Monitor; Pin 22: FSEQ

Pin 22 goes high when the frame synchronization (a positive polarity synchronization signal) from the EFM signal read in by PCK and the timing generated by the counter (the interpolation synchronization signal) agree. This pin is thus a synchronization detection monitor. (It is held high for a single frame.)

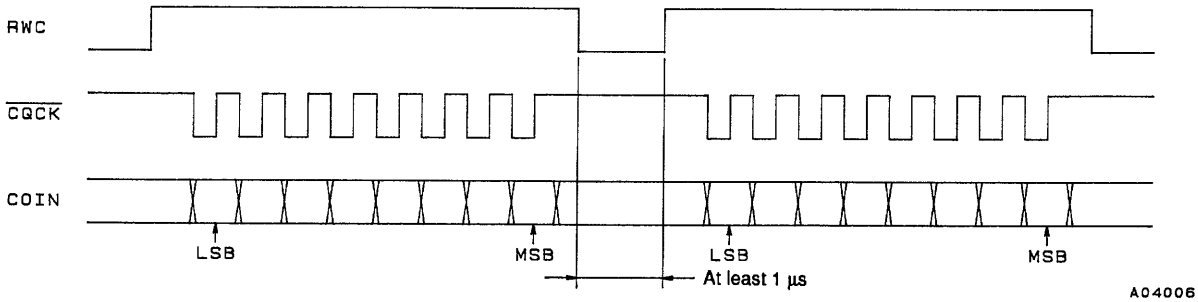
5. Servo command function; Pin 64: RWC, pin 66: COIN, pin 67: $\overline{\text{CQCK}}$
Commands can be executed by setting RWC high and inputting commands to the COIN pin in synchronization with the $\overline{\text{CQCK}}$ clock. Note that commands are executed on the falling edge of RWC.

Focus start Track jump Muting control Disk motor control Miscellaneous control	One-byte commands
Track check	Two-byte command (RWC set twice)
Digital attenuator	Two-byte command (RWC set once)

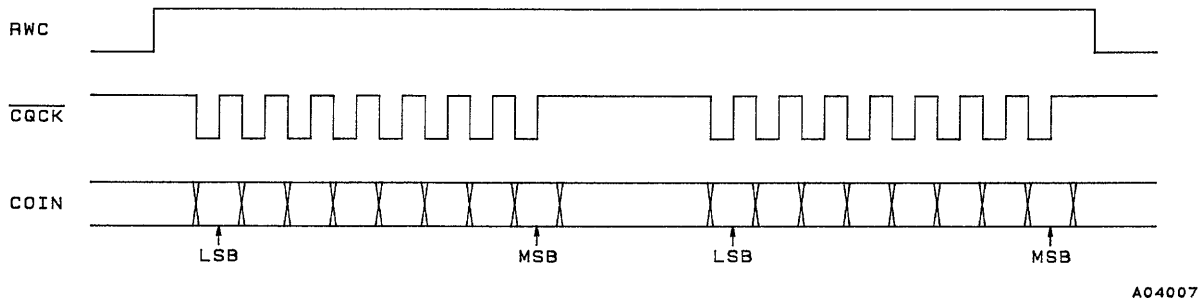
• One-byte commands



• Two-byte commands (RWC set twice)



• Two-byte commands (RWC set once)



- Command noise rejection

MSB LSB	Command	$\overline{\text{RES}}$ = low
1 1 1 0 1 1 1 1	COMMAND INPUT NOISE REDUCTION MODE	
1 1 1 0 1 1 1 0	RESET NOISE EXCLUSION MODE	○

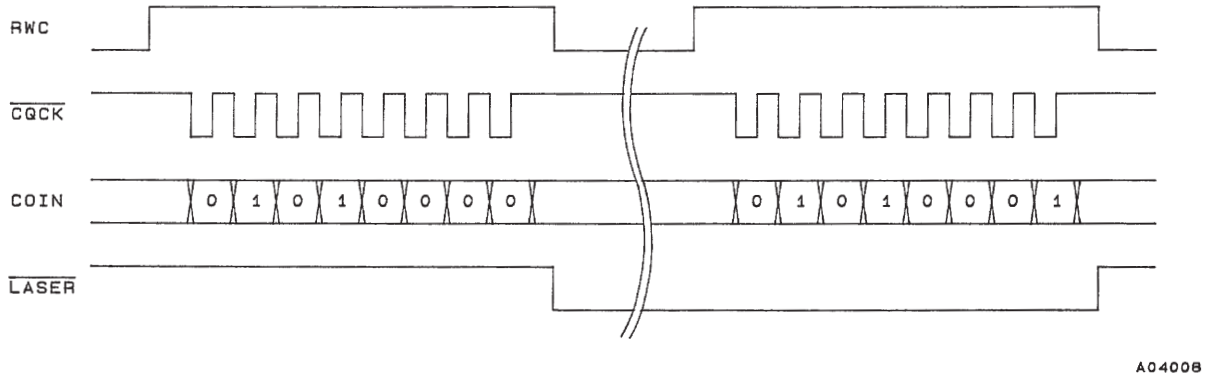
This command reduces the noise on the $\overline{\text{CQCK}}$ clock signal. While this is effective for noise pulses shorter than 500 ns, the $\overline{\text{CQCK}}$ timings $T_{W\emptyset L}$, $T_{W\emptyset H}$, and t_{setup} (see page 4 and 5, figure 1 and 2), must be set for at least 1 µs.

6. Focus Servo Circuit; Pin 16: FOCS, pin 17: FST, pin 18: $\overline{\text{FZD}}$, pin 70: $\overline{\text{LASER}}$

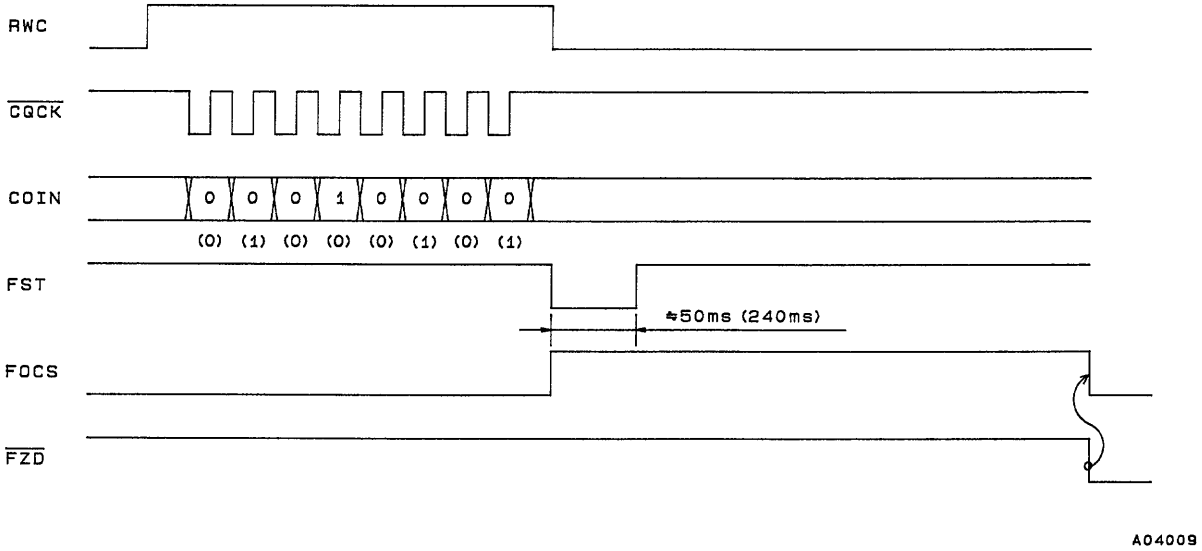
MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 0	FOCUS START #1	
1 0 1 0 0 0 1 0	FOCUS START #2	
0 0 0 0 1 0 1 0	LASER ON	
1 0 0 0 1 0 1 0	LASER OFF	○
1 1 1 1 1 1 1 0	NOTHING	

The FOCS, FST, and $\overline{\text{FZD}}$ pins are not required when the LC78621E is used in combination with the LA9230M or the LA9231M. $\overline{\text{FZD}}$ should be tied low when these pins are not used. The LA9230M and LA9231M focus start command is identical to the LC78621E FOCUS START #1 command.

- NOTHING
  This command can be used to initialize the LC78621E by inputting FE (hexadecimal). Note that 00 (hexadecimal) is the reset command for the LA9230M and the LA9231M, and should be used with care since it clears the result of the automatic adjustment process and returns these chips to their initial states.
- Laser control
  The $\overline{\text{LASER}}$ pin can be use as an extended output port.

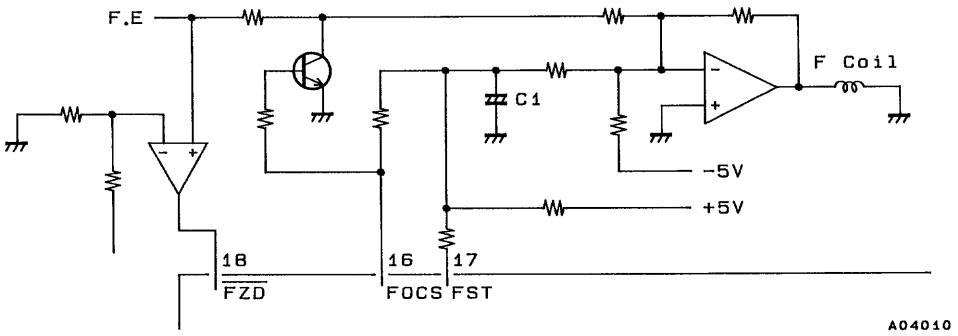


- Focus start
  When the LC78621E is used in combination with the LA9230M or the LA9231M, the focus start operation is executed completely on the servo side by commands form the control microprocessor. The following section describes this operation when the LC78621E is used in combination with the LA9230M or the LA9231M.
  When a focus start instruction (either FOCUS START #1 or FOCUS START #2) is input as a servo command, first the charge on capacitor C1 is discharged by FST and the objective lens is lowered. Next, the capacitor is charged by FOCS, and the lens is slowly raised. $\overline{\text{FZD}}$ falls when the lens reaches the focus point. When this signal is received, FOCS is reset and the focus servo turns on. After sending the command, the microprocessor should check the in-focus detection signal (the LA9210 DRF signal) to confirm focus before proceeding to the next part of the program. If focus is not achieved by the time C1 is fully charged, the microprocessor should issue another focus command and iterate the focus servo operation.



Values in parentheses are for the LASER START #2 command. The only difference is in the FST low period.

Note: 1. An $\overline{\text{FZD}}$ falling edge will not be accepted during the period that FST is low.
2. After issuing a focus start command, initialization will be performed if RWC is set high. Therefore, do not issue the next command during focus start until the focus coil drive S curve has completed.
3. When focus cannot be achieved (i.e., when $\overline{\text{FZD}}$ does not go low) the FOCS signal will remain in the high state and the lens will remain raised, so the microprocessor should initialize the system by issuing a NOTHING command.
4. When the RESET pin is set low, the $\overline{\text{LASER}}$ pin is set high directly.
5. Focus start using the DEMO pin executes a mode #1 focus start.

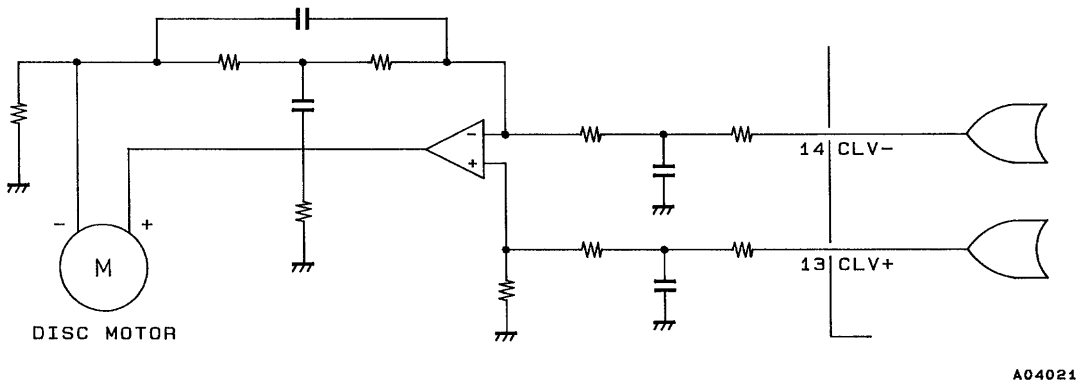


7. CLV servo circuit; Pin 13: CLV^+, pin 14: CLV^-, pin 15: $V/\overline{P}$

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 0 1 0 0	DISC MOTOR START (accelerate)	
0 0 0 0 0 1 0 1	DISC MOTOR CLV (CLV)	
0 0 0 0 0 1 1 0	DISC MOTOR BRAKE (decelerate)	
0 0 0 0 0 1 1 1	DISC MOTOR STOP (stop)	○

The CLV^+ pin provides the signal that accelerates the disk in the forward direction and the CLV^- pin provides the signal that decelerates the disk. Commands from the control microprocessor select one of four modes; accelerate, decelerate, CLV and stop. The table below lists the CLV^+ and CLV^- outputs in each of these modes.

Mode	CLV^+	CLV^-
Accelerate	High	Low
Decelerate	Low	High
CLV	*	*
Stop	Low	Low



Note: CLV servo control commands can set the TOFF pin low only in CLV mode. That pin will be at the high level at all other times. Control of the TOFF pin by microprocessor command is only valid in CLV mode.

- CLV mode

  In CLV mode the LC78621E detects the disk speed from the HF signal and provides proper linear speed using several different control schemes by switching the DSP internal modes. The PWM reference period corresponds to a frequency of 7.35 kHz. The V/$\overline{P}$ pin outputs a high level during rough servo and a low level during phase control.

Internal mode	CLV+	CLV−	V/$\overline{P}$
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PCK locked)	PWM	PWM	Low

- Rough servo gain switching

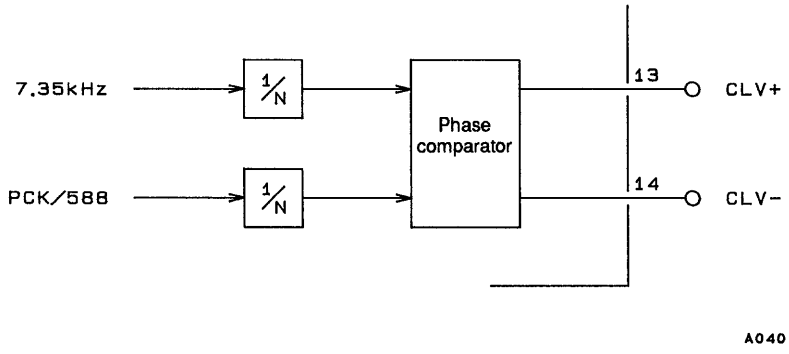
MSB LSB	Command	$\overline{RES}$ = low
1 0 1 0 1 0 0 0	DISC 8 SET	
1 0 1 0 1 0 0 1	DISC 12 SET	○

For 8 cm disks, the rough servo mode CLV control gain can be set about 8.5 dB lower than the gain used for 12 cm disks.

- Phase control gain switching

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 0 0 1	CLV PHASE COMPARATOR DIVISOR: 1/2	
1 0 1 1 0 0 1 0	CLV PHASE COMPARATOR DIVISOR: 1/4	
1 0 1 1 0 0 1 1	CLV PHASE COMPARATOR DIVISOR: 1/8	
1 0 1 1 0 0 0 0	NO CLV PHASE COMPARATOR DIVISOR USED	○

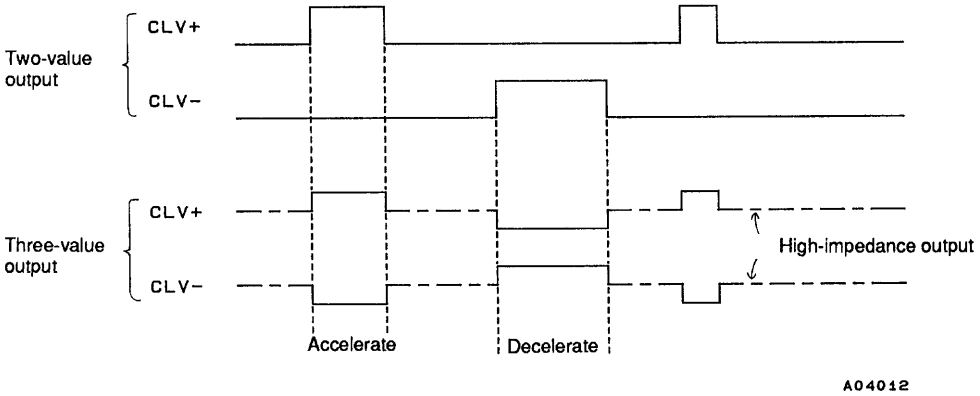
The phase control gain can be changed by changing the divisor used by the dividers in the stage immediately preceding the phase comparator.



• CLV three value output

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 1 0 0	CLV THREE VALUE OUTPUT	
1 0 1 1 0 1 0 1	CLV TWO VALUE OUTPUT (the scheme used by previous products)	○

The CLV three value output command allows the CLV to be controlled by a single pin.



• Internal brake modes

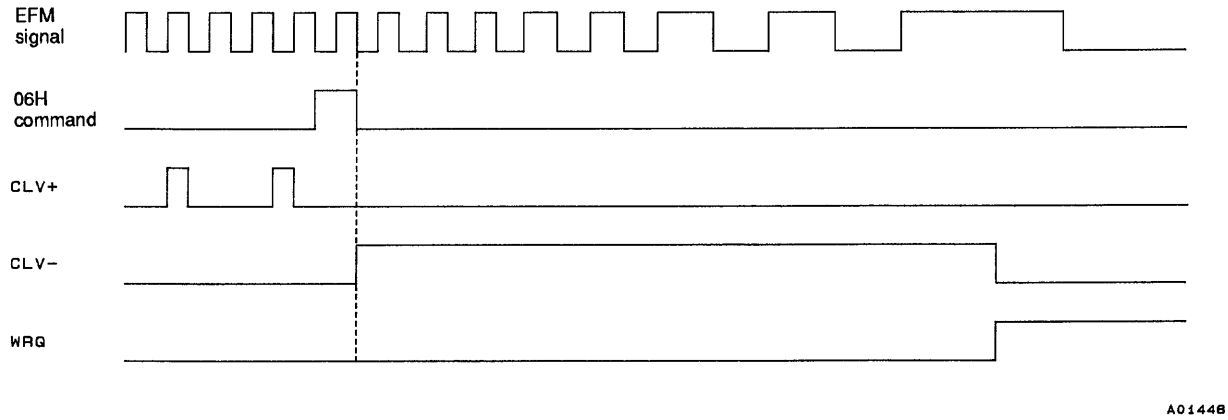
MSB LSB	Command	$\overline{RES}$ = low
1 1 0 0 0 1 0 1	INTERNAL BRAKE ON	
1 1 0 0 0 1 0 0	INTERNAL BRAKE OFF	○
1 0 1 0 0 0 1 1	INTERNAL BRAKE CONT	
1 1 0 0 1 0 1 1	INTERNAL BRAKE CONTINUOUS MODE	
1 1 0 0 1 0 1 0	RESET CONTINUOUS MODE	○
1 1 0 0 1 1 0 1	TON MODE DURING INTERNAL BRAKING	
1 1 0 0 1 1 0 0	RESET TON MODE	○

— Issuing the internal brake-on (C5H) command sets the LC78621E to internal brake mode. In this mode, the disk deceleration state can be monitored from the WRQ pin when a brake command (06H) is executed.

— In this mode the disk deceleration state is determined by counting the EFM signal density in a single frame, and when the EFM signal count falls under four, the CLV^- pin is dropped to low. At the same time the WRQ signal, which functions as a brake completion monitor, goes high. When the microprocessor detects a high level on the WRQ signal, it should issue a STOP command to fully stop the disk. In internal brake continuous mode, the CLV^- pin high-level output braking operation continues even after the WRQ brake completion monitor goes high.

Note that if errors occur in deceleration state determination due to noise in the EFM signal, the problem can be rectified by changing the EFM signal count from four to eight with the internal brake control command (A3H).

— In internal braking TON mode, the TOFF pin is held low during internal brake operations. We recommend using this feature, since it is effective at preventing incorrect detection at the disk mirror surface.



Note: 1. If focus is lost during the execution of an internal brake command, the pickup must first be refocussed and then the internal brake command must be reissued.
2. Since incorrect deceleration state determination is possible depending on the EFM signal playback state (e.g., disk defects, access in progress), we recommend using these functions in combination with a microprocessor.

8. Track Jump Circuit; Pin 19: HFL, pin 20: TES, pin 23: TOFF, pin 24: TGL, pin 25: THLD, pin 28: JP^+, pin 29: JP^-

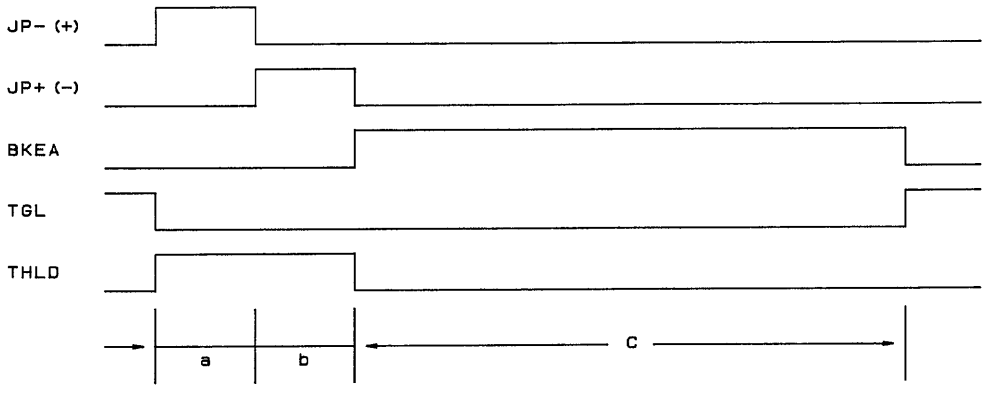
- The LC78621E supports the two track count modes listed below.

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 0 0 1 0	NEW TRACK COUNT (using the TES/HFL combination)	○
0 0 1 0 0 0 1 1	STANDARD TRACK COUNT (directly counts the TES signal)	

The earlier track count function uses the TES signal directly as the internal track counter clock.
To reduce counting errors resulting from noise on the rising and falling edges of the TES signal, the new track count function prevents noise induced errors by using the combination of the TES and HFL signals, and implements a more reliable track count function. However, dirt and scratches on the disk can result in HFL signal dropouts that may result in missing track count pulses. Thus care is required when using this function.

• TJ commands

MSB	LSB	Command	$\overline{RES}$ = low
1 0 1 0 0 0 0 0		STANDARD TRACK JUMP	○
1 0 1 0 0 0 0 1		NEW TRACK JUMP	
0 0 0 1 0 0 0 1		1 TRACK JUMP IN #1	
0 0 0 1 0 0 1 0		1 TRACK JUMP IN #2	
0 0 1 1 0 0 0 1		1 TRACK JUMP IN #3	
0 1 0 1 0 0 1 0		1 TRACK JUMP IN #4	
0 0 0 1 0 0 0 0		2 TRACK JUMP IN	
0 0 0 1 0 0 1 1		4 TRACK JUMP IN	
0 0 0 1 0 1 0 0		16 TRACK JUMP IN	
0 0 1 1 0 0 0 0		32 TRACK JUMP IN	
0 0 0 1 0 1 0 1		64 TRACK JUMP IN	
0 0 0 1 0 1 1 1		128 TRACK JUMP IN	
0 0 0 1 1 0 0 1		1 TRACK JUMP OUT #1	
0 0 0 1 1 0 1 0		1 TRACK JUMP OUT #2	
0 0 1 1 1 0 0 1		1 TRACK JUMP OUT #3	
0 1 0 1 1 0 1 0		1 TRACK JUMP OUT #4	
0 0 0 1 1 0 0 0		2 TRACK JUMP OUT	
0 0 0 1 1 0 1 1		4 TRACK JUMP OUT	
0 0 0 1 1 1 0 0		16 TRACK JUMP OUT	
0 0 1 1 1 0 0 0		32 TRACK JUMP OUT	
0 0 0 1 1 1 0 1		64 TRACK JUMP OUT	
0 0 0 1 1 1 1 1		128 TRACK JUMP OUT	
0 0 0 1 0 1 1 0		256 TRACK CHECK	
0 0 0 0 1 1 1 1		TOFF	
1 0 0 0 1 1 1 1		TON	○
1 0 0 0 1 1 0 0		TRACK JUMP BRAKE	
0 0 1 0 0 0 0 1		THLD PERIOD TOFF OUTPUT MODE	
0 0 1 0 0 0 0 0		RESET THLD PERIOD TOFF OUTPUT MODE	○



When the LC78621E receives a track jump instruction as a servo command, it first generates accelerating pulses (period a) and next generates deceleration pulses (period b). The passage of the braking period (period c) completes the specified jump. During the braking period, the LC78621E detects the beam slip direction from the TES and HFL inputs. TOFF is used to cut the components in the TE signal that aggravate slip. The jump destination track is captured by increasing the servo gain with TGL. In THLD period TOFF output mode the TOFF signal is held high during the period when THLD is high.

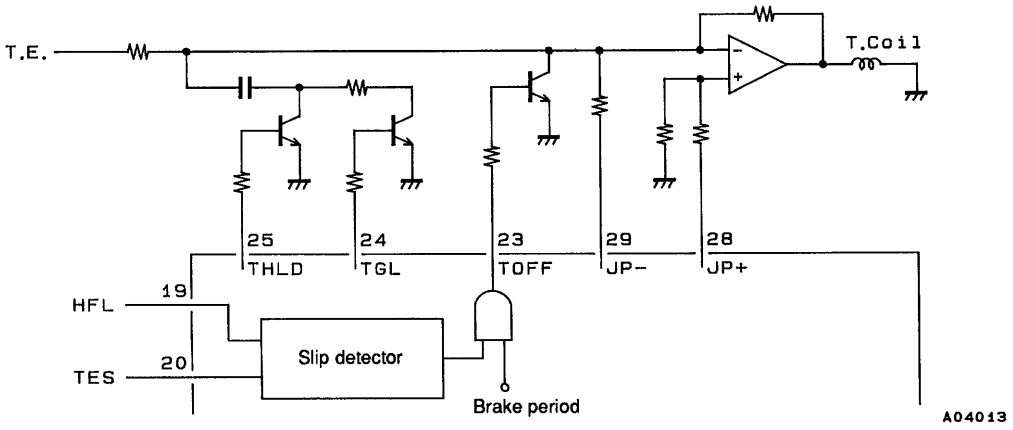
Note: Of the modes related to disk motor control, the TOFF pin only goes low in CLV mode, and will be high during start, stop, and brake operations. Note that the TOFF pin can be turned on and off independently by microprocessor issued commands. However, this function is only valid when disk motor control is in CLV mode.

• Track jump modes

The table lists the relationships between acceleration pulses, deceleration pulses, and the braking period.

Command	Standard track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	60 ms	233 µs	233 µs	60 ms
1 TRACK JUMP IN (OUT) #2	0.5 track jump period	233 µs	60 ms	0.5 track jump period	0.5 track jump period	60 ms
1 TRACK JUMP IN (OUT) #3	0.5 track jump period	233 µs	This period does not exist.	0.5 track jump period	0.5 track jump period	This period does not exist.
1 TRACK JUMP IN (OUT) #4	0.5 track jump period	233 µs	60 ms; TOFF is low during the C period.	0.5 track jump period	0.5 track jump period	60 ms; TOFF is low during the C period.
2 TRACK JUMP IN (OUT)	None	None	None	1 track jump period	1 track jump period	This period does not exist.
4 TRACK JUMP IN (OUT)	2 track jump period	466 µs	60 ms	2 track jump period	2 track jump period	60 ms
16 TRACK JUMP IN (OUT)	9 track jump period	7 track jump period	60 ms	9 track jump period	9 track jump period	60 ms
32 TRACK JUMP IN (OUT)	18 track jump period	14 track jump period	60 ms	18 track jump period	14 track jump period	60 ms
64 TRACK JUMP IN (OUT)	36 track jump period	28 track jump period	60 ms	36 track jump period	28 track jump period	60 ms
128 TRACK JUMP IN (OUT)	72 track jump period	56 track jump period	60 ms	72 track jump period	56 track jump period	60 ms
256 TRACK CHECK	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms
TRACK JUMP BRAKE	There are no a or b periods.		60ms	There are no a and b periods.		60 ms

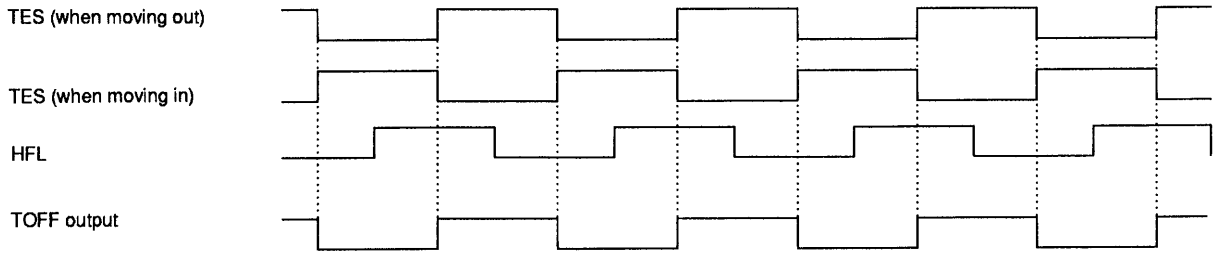
Note: 1. As indicated in the table, actuator signals are not output during the 256 TRACK CHECK function. This is a mode in which the TES signal is counted in the tracking loop off state. Therefore, feed motor forwarding is required.
2. The servo command register is automatically reset after one cycle of the track jump sequence (a, b, c) completes.
3. If another track jump command is issued during a track jump operation, the content of that new command will be executed starting immediately.
4. The 1 TRACK JUMP #3 and 2 TRACK JUMP modes do not have a braking period (the C period). Since brake mode must be generated by an external circuit, care is required when using this mode.



When the LC78621E is used in combination with the LA9230M or the LA9231M, since the THLD signal is generated by the LA9230M or the LA9231M, the THLD pin (pin 25) will be unused, i.e., have no connection.

5. Tracking brake

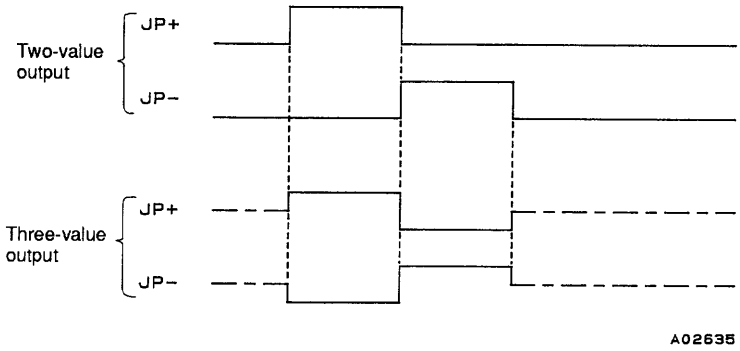
The chart shows the relationships between the TES, HFL, and TOFF signals during the track jump C period. The TOFF signal is extracted from the HFL signal by TES signal edges. When the HFL signal is high, the pickup is over the mirror surface, and when low, the pickup is over data bits. Thus braking is applied based on the TOFF signal being high when the pickup is moving from a mirror region to a data region and being low when the pickup is moving from a data region to a mirror region.



• JP three-value output

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 1 0 1 1 0	JP THREE VALUE OUTPUT	
1 0 1 1 0 1 1 1	JP TWO VALUE OUTPUT (earlier scheme)	○

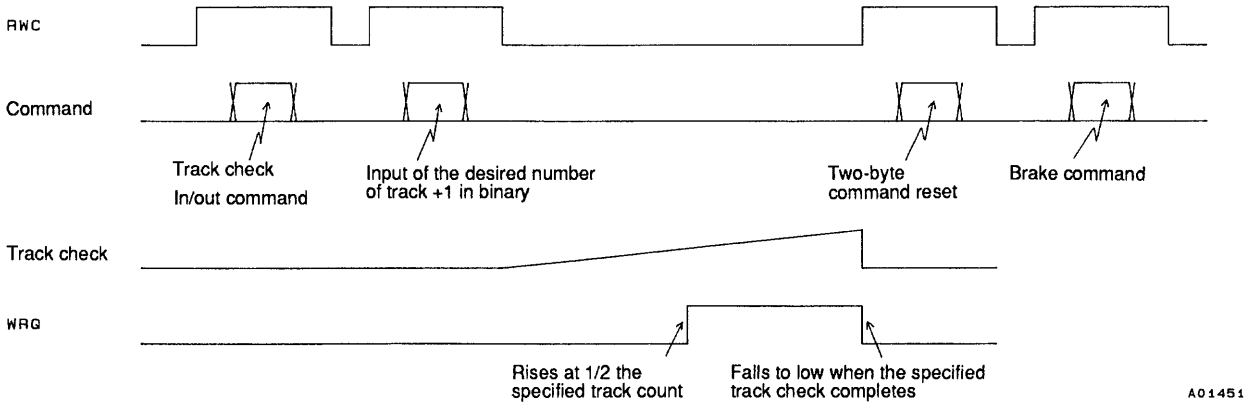
The JP three-value output command allows the track jump operation to be controlled from a single pin.



• Track check mode

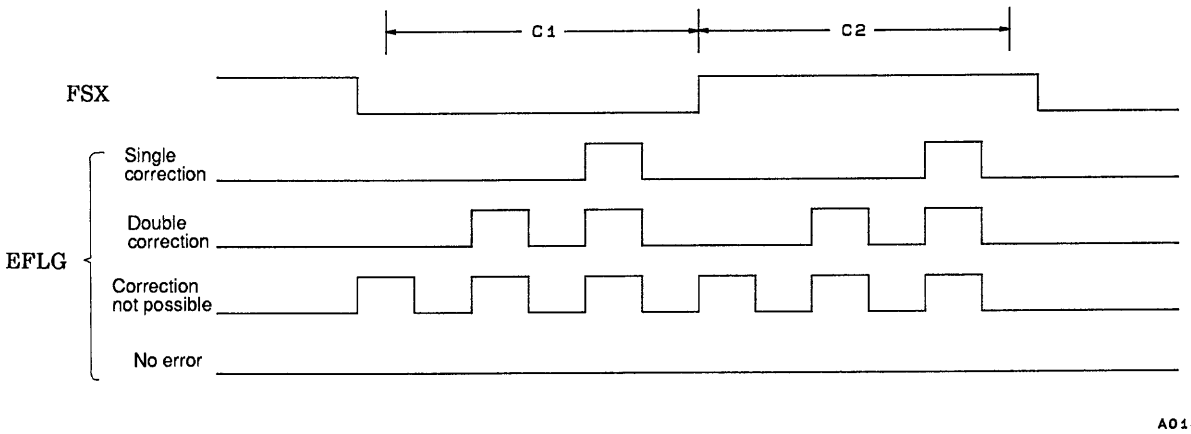
MSB LSB	Command	$\overline{RES}$ = low
1 1 1 1 0 0 0 0	TRACK CHECK IN	
1 1 1 1 1 0 0 0	TRACK CHECK OUT	
1 1 1 1 1 1 1 1	TWO BYTE COMMAND RESET	○

The LC78621E will count the specified number of tracks minus one when the microprocessor sends an arbitrary binary value in the range 8 to 254 after issuing either a track check in or a track check out command.



Note: 1. When the desired track count has been input in binary, the track check operation is started by the fall of RWC.
2. During a track check operation the TOFF pin goes high and the tracking loop is turned off. Therefore, feed motor forwarding is required.
3. When a track check in/out command is issued the function of the WRQ signal switches from the normal mode subcode Q standby monitor function to the track check monitor function. This signal goes high when the track check is half completed, and goes low when the check finishes. The control microprocessor should monitor this signal for a low level to determine when the track check completes.
4. If a two-byte reset command is not issued, the track check operation will repeat. That is, to skip over 20,000 tracks, issue a track check 201 command once, and then count the WRQ signal 100 times. This will check 20,000 tracks.
5. After performing a track check operation, use the brake command to have the pickup lock onto the track.

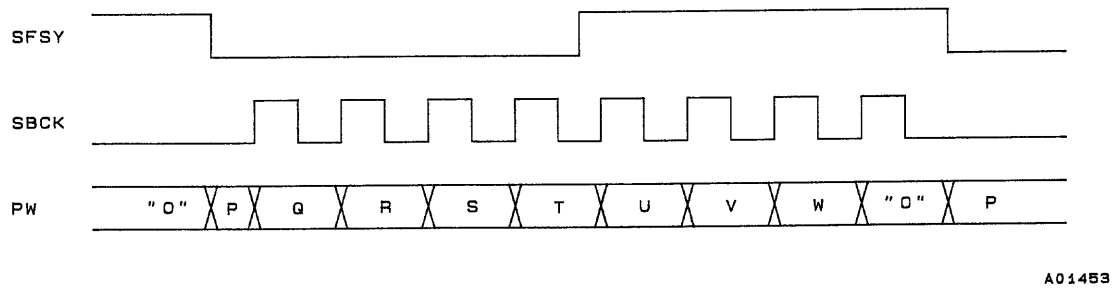
9. Error Flag Output; Pin 58: EFLG, pin 62: FSX



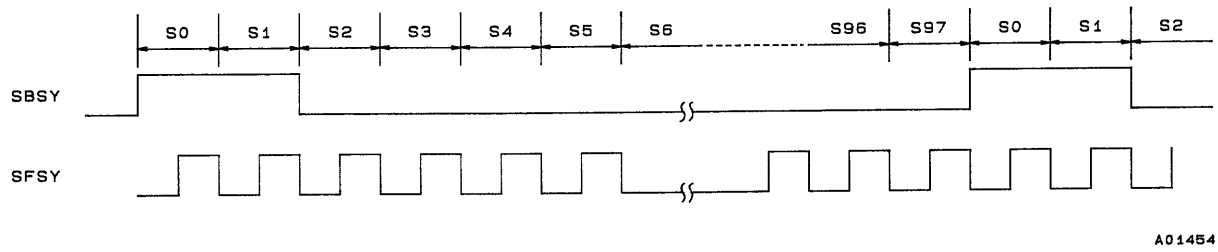
The FSX signal is generated by dividing the crystal oscillator clock, and is a 7.35 kHz frame synchronization signal. The error correction state for each frame is output from EFLG. The playback OK/NG state can be easily determined from the extent of the high level that appears here.

10. Subcode P, Q, and R to W Output Circuit; Pin 59: PW, pin 57: SBSY, pin 60: SFSY, pin 61: SBCK

PW is the subcode signal output pin, and all the codes, P, Q, and R to W can be read out by sending eight clocks to the SBCK pin within 136 µs after the fall of SFSY. The signal that appears on the PW pin changes on the falling edge of SBCK. If a clock is not applied to SBCK, the P code will be output from PW. SFSY is a signal that is output for each subcode frame cycle, and the falling edge of this signal indicates standby for the output of the subcode symbol (P to W). Subcode data P is output on the fall of this signal.



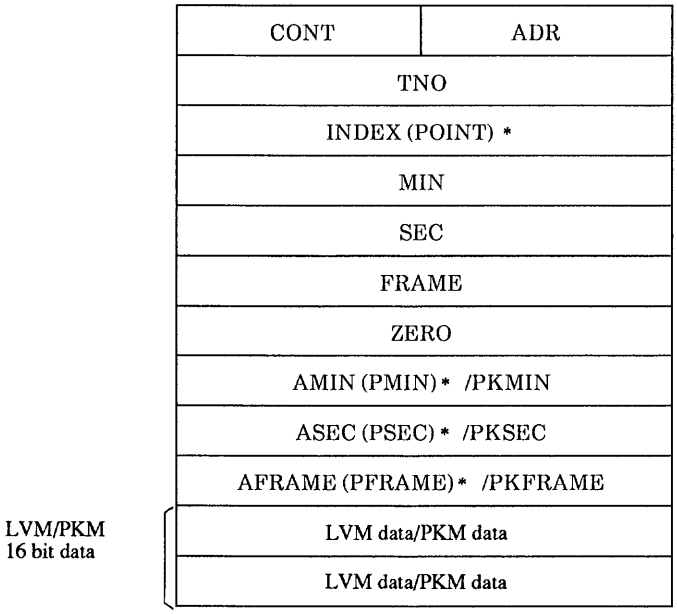
SBSY is a signal output for each subcode block. This signal goes high for the S0 and S1 synchronization signals. The fall of this signal indicates the end of the subcode synchronization signals and the start of the data in the subcode block. (EIAJ format)



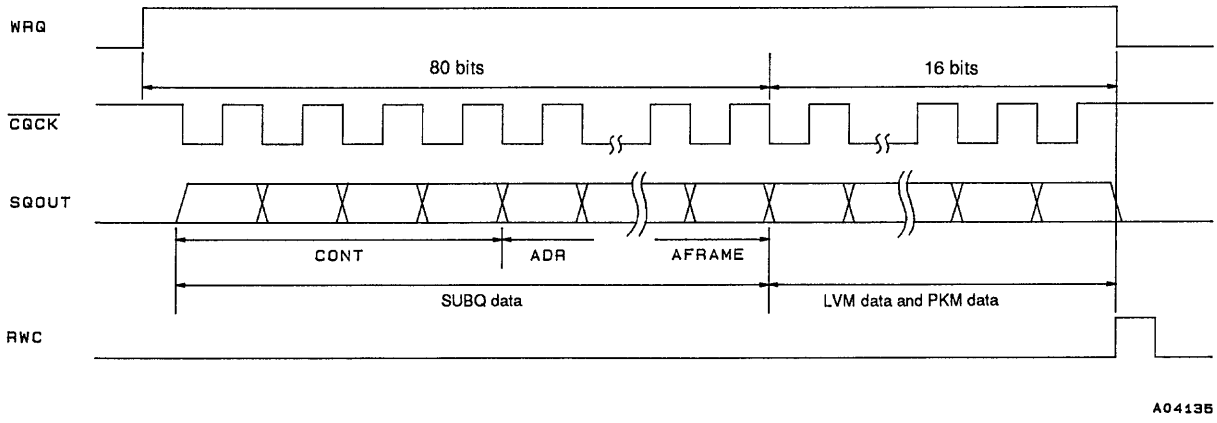
11. Subcode Q Output Circuit; Pin 63: WRQ, pin 64: RWC, pin 65: SQOUT, pin 67: $\overline{\text{CQCK}}$, pin 75: $\overline{\text{CS}}$

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 1	ADDRESS FREE	
1 0 0 0 1 0 0 1	ADDRESS 1	○

Subcode Q can be read from the SQOUT pin by applying a clock to the $\overline{\text{CQCK}}$ pin.
Of the eight bits in the subcode, the Q signal is used for song (track) access and display. The WRQ will be high only if the data passed the CRC error check and the subcode Q format internal address is 1*. The control microprocessor can read out data from SQOUT in the order shown below by detecting this high level and applying $\overline{\text{CQCK}}$. When $\overline{\text{CQCK}}$ is applied the DSP disables register update internally. The microprocessor should give update permission by setting RWC high briefly after reading has completed. WRQ will fall to low at this time. Since WRQ falls to low 11.2 ms after going high, $\overline{\text{CQCK}}$ must be applied during the high period. Note that data is read out in an LSB first format.
Note: * That state will be ignored if an address free command is input. This is provided to handle CD-ROM applications.



Note: * Items in parentheses refer to the read-in area.



Note: 1. Normally, the WRQ pin indicates the subcode Q standby state. However, it is used for a different monitoring purpose in track check mode and during internal braking. (See the items on track counting and internal braking for details.)
2. The LC78621E becomes active when the $\overline{\text{CS}}$ pin is low, and subcode Q data is output from the SQOUT pin. When the $\overline{\text{CS}}$ pin is high, the SQOUT pin goes to the high-impedance state.

12. Level Meter (LVM) Data and Peak Meter (PKM) data readout

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 1 0 1 1	PKM SET (LVM Reset)	
0 0 1 0 1 1 0 0	LVM SET (PKM Reset)	○
0 0 1 0 1 1 0 1	PKM MASK SET	
0 0 1 0 1 1 1 0	PKM MASK RESET	○

- Level meter (LVM)
  - The LVM set (2CH) command sets the LC78621E to LVM mode.
  - LVM data is a 16-bit word in which the MSB indicates the L/R polarity and the low-order 15 bits are absolute value data. A one in the MSB indicates left channel data and a zero indicates right channel data.
  - LVM data is appended after the 80 bits of SubQ data, and can be read out by applying 96 clock cycles to the $\overline{CQCK}$ pin. Each time LVM data is read out the left/right channel state is inverted. Data is held independently for both the left and right channels. In particular, the largest value that occurs between readouts for each channel is held.
- Peak meter (PKM)
  - The PKM set (2BH) command sets the LC78621E to PKM mode.
  - PKM data is a 16-bit word in which the MSB is always zero and the low-order 15 bits are absolute value data. This functions detects the maximum value that occurs in the data, whichever channel that value occurs in.
  - PKM data is read out in the same manner as LVM data. However, data is not updated as a result of the readout operation.
  - The absolute time for PKM mode SubQ data is computed by holding the absolute time (ATIME) detected after the maximum value occurred and sending that value. (Normal operation uses relative time.)
  - It is possible to set the LC78621E to ignore values larger than the already recorded value by issuing the PKM mask set command, even in PKM mode. This function is cleared by issuing a PKM mask reset command. (This is used in PK search in a memory track.)

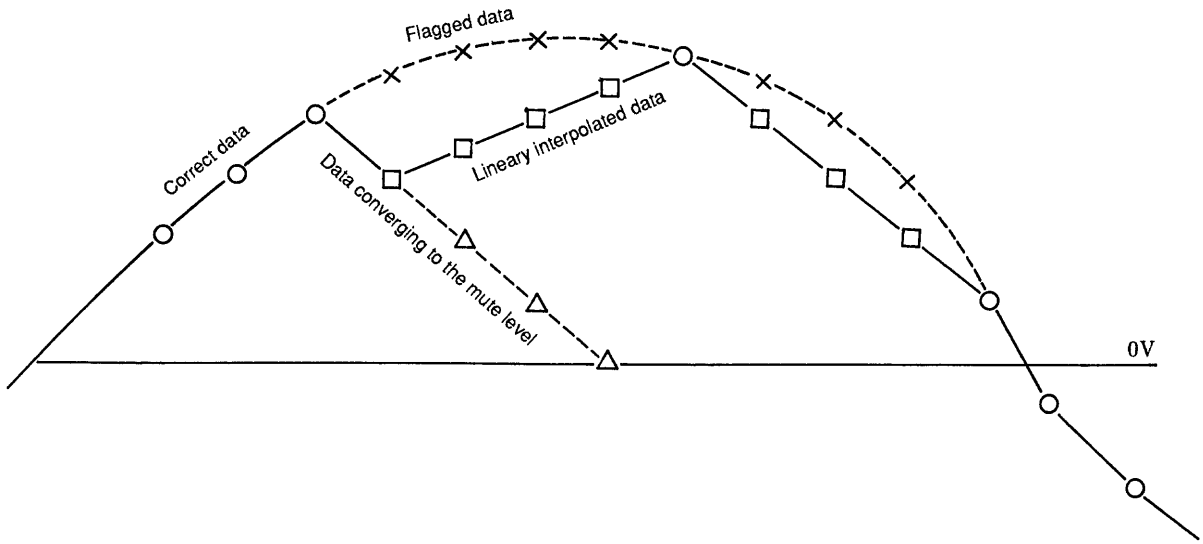
13. Mute Control Circuit

MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 0 0 1	MUTE: 0 dB	
0 0 0 0 0 0 1 0	MUTE: –12 dB	
0 0 0 0 0 0 1 1	MUTE: –∞ dB	○

An attenuation of 12 dB (MUTE –12 dB) or full muting (MUTE ∞ dB) can be applied by issuing the appropriate command from the table. Since zero cross muting is used, there is minimal noise associated with this function. Zero cross is defined for this function as the top seven bits being all ones or all zeros.

14. Interpolation Circuit

Outputting incorrect audio data that could not be corrected by the error detection and correction circuit would result in loud noises being output. To minimize this noise, the LC78621E replaces the incorrect data with linearly interpolated data based on the correct data on either side of the incorrect data. More precisely, the LC78621E uses this technique if C2 flags occurred up to three times in a row. If C2 flags occurred four or more times in a row, the LC78621E converges the output level to the muting level. However, when correct data is finally output following four or more C2 flag occurrences, the LC78621E replaces the 3 data items between the data output three items previously and the correct data with data linearly interpolated data.



15. Bilingual Function

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 1 0 1 0 0 0	STO CONT	○
0 0 1 0 1 0 0 1	Lch CONT	
0 0 1 0 1 0 1 0	Rch CONT	

- Following a reset or when a stereo (28H) command has been issued, the left and right channel data is output to the left and right channels respectively.
- When an Lch set (29H) command is issued, the left and right channels both output the left channel data.
- When an Rch set (2AH) command is issued, the left and right channels both output the right channel data.

16. De-Emphasis; Pin 32: EMPH

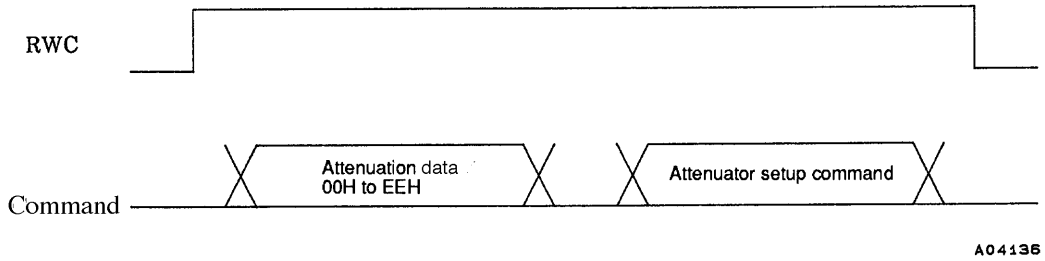
The preemphasis on/off bit in the subcode Q control information is output from the EMPH pin. When this pin is high, the LC78621E internal de-emphasis circuit operates and the digital filters and the D/A converter output de-emphasized data.

17. Digital Attenuator

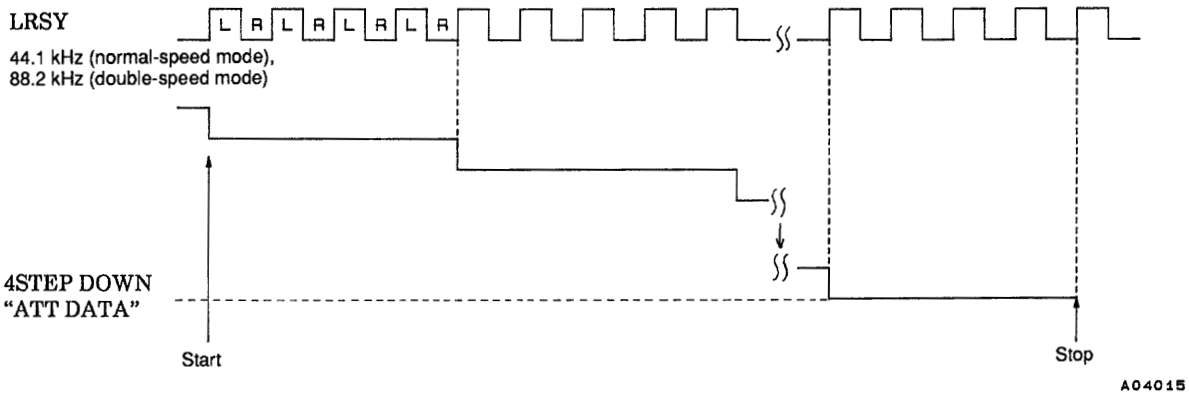
Digital attenuation can be applied to the audio data by setting the RWC pin high and inputting the corresponding two-byte command to the COIN pin in synchronization with the $\overline{\text{CQCK}}$ clock.

MSB LSB	Command	$\overline{\text{RES}}$ = low
1 0 0 0 0 0 0 0 1	ATT DATA SET ----------→	DATA 00H set (MUTE –∞ dB)
1 0 0 0 0 0 0 1 0	ATT 4 STEP UP	
1 0 0 0 0 0 0 1 1	ATT 4 STEP DOWN	
1 0 0 0 0 0 1 0 0	ATT 8 STEP UP	
1 0 0 0 0 0 1 0 1	ATT 8 STEP DOWN	
1 0 0 0 0 0 1 1 0	ATT 16 STEP UP	
1 0 0 0 0 0 1 1 1	ATT 16 STEP DOWN	

- Attenuation setup
  Since the attenuation level is set to the muted state (a muting of –∞ is specified by an attenuation coefficient of 00H) after the attenuation level is reset, the attenuation coefficient must be directly set to EEH (using the ATT DATA SET command) to output audio signals. Note that the attenuation level can be set to one of 239 values from 00H to EEH. These two-byte commands differ from the two-byte commands used for track counting in that it is only necessary to set RWC once and a two-byte command reset is not required. (See the item on two-byte commands (RWC set once) on page 10.)



After inputting the target attenuation level as a value in the range 00H to EEH, sending an attenuator step up/down command will cause the attenuation level to approach the target value in steps of 4, 8, or 16 units as specified in synchronization with rising edges on the LRSY input. However, the ATT DATA SET command sets the target value directly. If a new data value is input during the transition, the value begins to approach the new target value at that point. Note that the UP/DOWN distinction is significant here.



$$\text{Audio output level} = 20 \log \frac{\text{ATT DATA}}{100\text{H}} [\text{dB}]$$

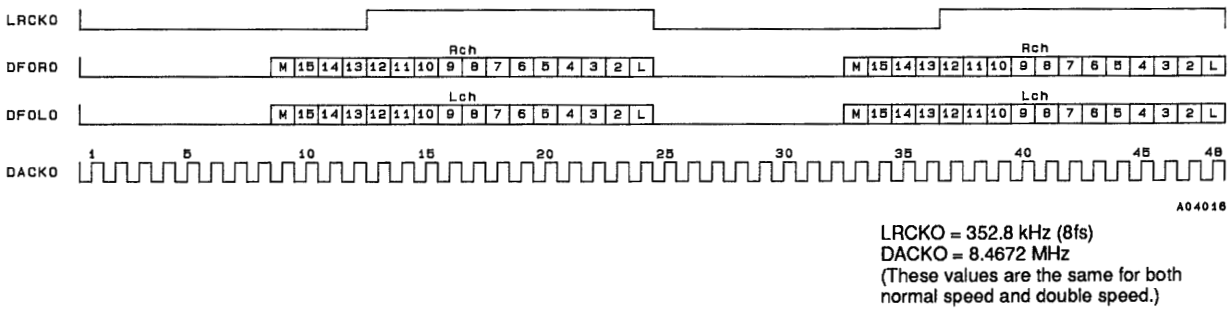
For example, the formula below calculates the time required for the attenuation level to increase from 00H to EEH when a 4STEP UP command is executed. Note that the control microprocessor must provide enough of a time margin for this operation to complete before issuing the next attenuation level set command.

$$\frac{238 \text{ level} \times 4\text{STEP UP}}{44.1 \text{ kHz (LRSY)}} \approx 21.6 \text{ ms}$$

Note: Setting the attenuation level to values of EFH or higher is disallowed to prevent overflows in one-bit D/A converter calculations from causing noise.

- Mute output; Pin 46: MUTEL, pin 55: MUTER
  These pins output a high level when the attenuator coefficient is set to 00H and the data in each channel has been zero for a certain period. If data input occurs once again, these pins go low immediately.

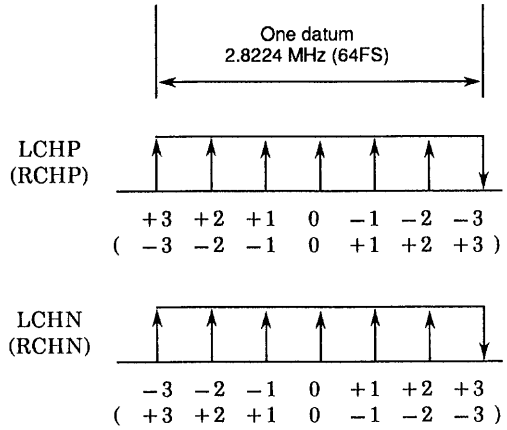
18. Digital Filter Outputs; Pin 33: LRCKO, pin 34: DFORO, pin 35: DFOLO, pin 36: DACKO
    Data for use with an external D/A converter is output MSB first from DFORO and DFOLO in synchronization with the falling edge of DACKO. These pins are provided so that an external D/A converter can be used if desired.



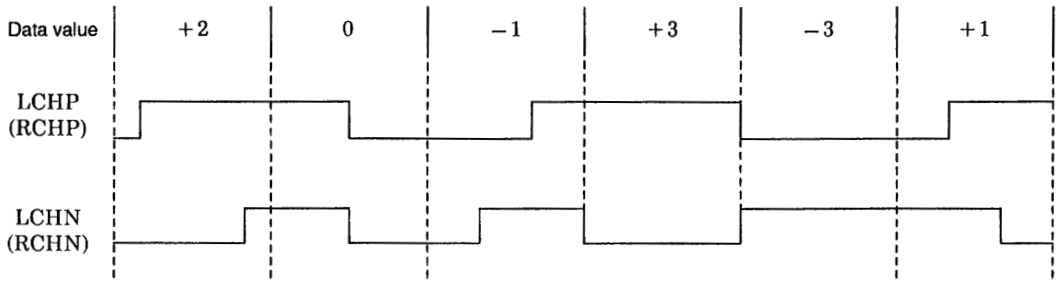
LRCKO = 352.8 kHz (8fs)
DACKO = 8.4672 MHz
(These values are the same for both normal speed and double speed.)

- Although this output is from 8× oversampling filters for normal-speed playback, 4× oversampling filters are used in double-speed playback.

19. One-bit D/A Converter
    - The LC78621E PWM block outputs a single data value in the range –3 to +3 once every 64fs period. To reduce carrier noise, this block adopts an output format in which each data switching block is adjusted so that the PWM output level does not invert. Also, the attenuator block detects 0 data and enters muting mode so that only a 0 value (a 50% duty signal) is output.
      This block outputs a positive phase signal to the LCHP (RCHP) pin and a negative phase signal to the LCHN (RCHN) pin. High-quality analog signals can be acquired by taking the differences of these two output pairs using external low-pass filters.
      The LC78621E includes built-in suppression resistors in each of the LCHP/N and RCHP/N pins.
    - PWM output format



    - PWM output example

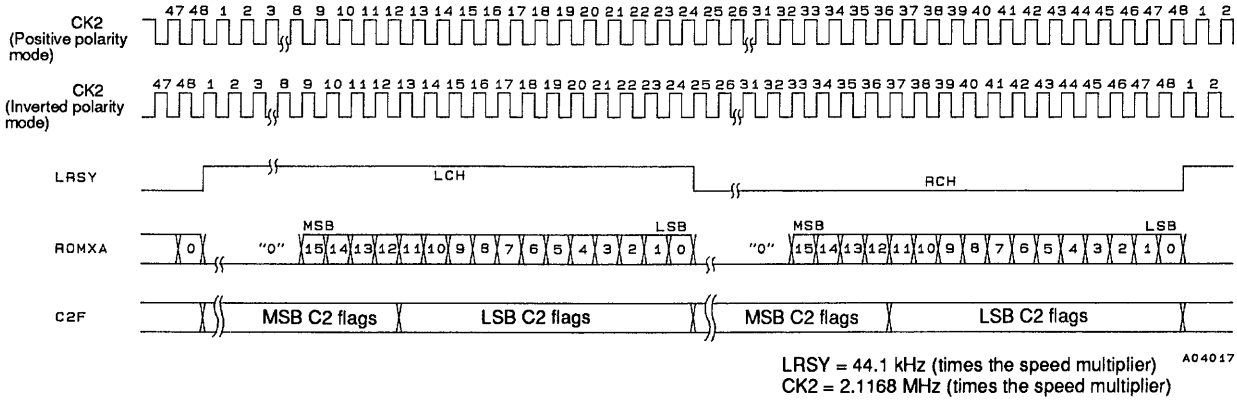


20. CD-ROM Outputs; Pin 42: LRSY, pin 43: CK2, pin 44: ROMXA, pin 45: C2F

Although the LC78621E is initially set up to output audio data from the interpolation circuit MSB first from the ROMXA pin in synchronization with the LRSY signal, the circuit can be switched to output CD-ROM data by issuing a CD-ROM XA command. Since this data has not been processed by the interpolation, muting, and other digital circuits, it is appropriate for input to a CD-ROM encoder LSI. CK2 is a 2.1168 MHz clock, and data is output on the CK2 falling edge. However, this clock polarity can be inverted by issuing a CK2 polarity inversion command. C2F is the flag information for the data in 8-bit units. Note that the CD-ROM XA reset command has the same function as the CONT pin (pin 73).

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 0 0 0	CD-ROM XA	
1 0 0 0 1 0 1 1	CONT AND CD-ROM XA RESET	○
1 1 0 0 1 0 0 1	CK2 POLARITY INVERSION	

LC78621E CD-ROM encoder LSI (LC895XX) interface



21. Digital Output Circuit; Pin 56: DOUT

This is an output pin for use with a digital audio interface. Data is output in the EIAJ format. This signal has been processed by the interpolation and muting circuits. This pin has a built-in driver circuit and can directly drive a transformer.

MSB LSB	Command	$\overline{RES}$ = low
0 1 0 0 0 0 1 0	DOUT ON	○
0 1 0 0 0 0 1 1	DOUT OFF	
0 1 0 0 0 0 0 0	UBIT ON	○
0 1 0 0 0 0 0 1	UBIT OFF	

- The DOUT pin can be locked at the low level by issuing a DOUT OFF command.
- The UBIT information in the DOUT data can be locked at zero by issuing a UBIT OFF command.
- The DOUT data can be switched to data for which interpolation and muting processing have not been performed by issuing a CD-ROM XA command.

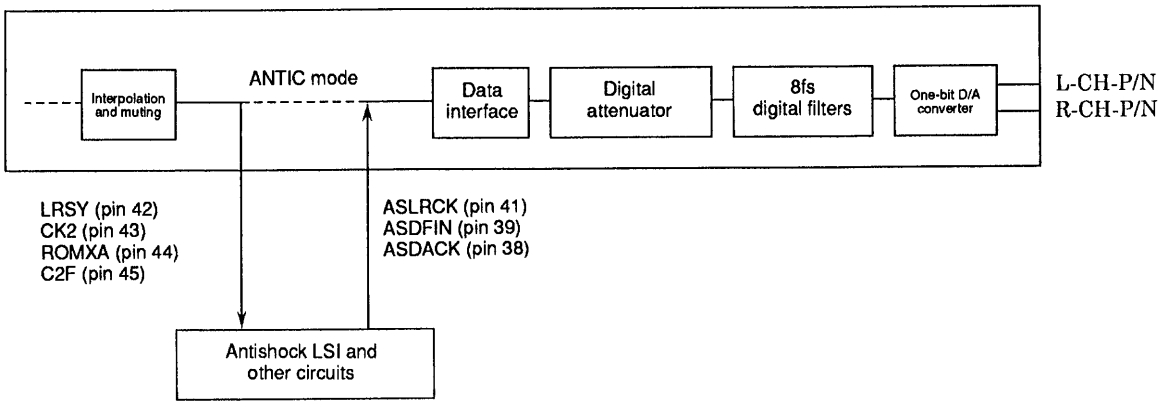
22. AntiShock Mode; Pin 38: ASDACK, pin 39: ASDFIN, pin 40: ASDFIR, pin 41: ASLRCK, pin 42: LRSY, pin 43: CK2, pin 44: ROMXA, pin 45: C2F

- Antishock mode is a mode in which antishock processing is applied to data that has been output once. That data is returned and output once again as an audio playback signal. It is also possible to use only the audio playback block (the attenuator, 8× oversampling digital filter, and one-bit D/A converter circuits) and thus share the audio playback block with other systems by synchronizing the other system with this LSI's clock.
  Note that de-emphasis on/off switching is controlled by the LC78621E subcode Q playback state.

- The ASDACK (pin 38), ASDFIN (pin 39), ASDFIR (pin 40), and ASLRCK (pin 41) pins must be held low if this mode is not used.

MSB LSB	Command	$\overline{RES}$ = low
0 1 1 0 1 1 0 0	ANTIC ON	
0 1 1 0 1 0 1 1	ANTIC OFF	○
0 1 1 0 1 1 1 1	DF NORMAL SPEED ON (only in antishock mode)	
0 1 1 0 1 1 1 0	DF NORMAL SPEED OFF (only in antishock mode)	○

- It is possible to input the signals from the ROMXA (pin 44), C2F (pin 45), LRSY (pin 42), and CK2 (pin 43) pins to an antishock LSI (the Sanyo LC89151) and re-input the signals output by the antishock LSI to the ASDFIN (pin 39), ASLRCK (pin 41), and ASDACK (pin 38) pins. These signals are then processed by the attenuator, 8× oversampling digital filter, and one-bit D/A converter circuits and output as audio signals.
- In antishock systems, the signal-processing block must operate in double-speed playback mode for data output to the antishock LSI, and the audio playback block (the attenuator, 8× oversampling digital filter, and one-bit D/A converter circuits) must operate at normal speed. This means that the control microprocessor must issue both the ANTIC on command (6CH) as well as the DF normal speed on command (6FH).
- The ANTIC off command (6BH) clears antishock mode.



23. CONT Pin; Pin 73: CONT

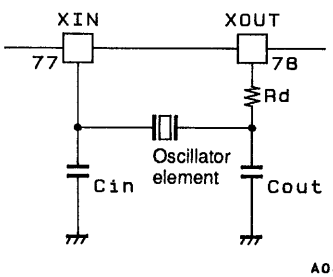
MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 1 1 1 0	CONT SET	Low
1 0 0 0 1 0 1 1	CONT AND CD-ROM XA RESET	○

The CONT pin goes high when a CONT SET command is issued.

24. Clock Oscillator; Pin 77: X_{IN}, pin 78: X_{OUT}

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 1 1 0	OSC ON	○
1 0 0 0 1 1 0 1	OSC OFF	
1 1 0 0 0 0 1 0	NORMAL-SPEED PLAYBACK	○
1 1 0 0 0 0 0 1	DOUBLE-SPEED PLAYBACK	

The clock that is used as the time base is generated by connecting a 16.9344 MHz oscillator element between these pins. The OSC OFF command turns off both the VCO and crystal oscillators. Double-speed playback can be specified by microprocessor command.



• Recommended crystal and ceramic oscillator elements

Manufacturer	Product No.	Load capacitance C1/C2 (C1 = C2)	Damping resistor Rd
Citizen Watch Co., Ltd. (crystal oscillator elements)	CSA-309 (16.9344 MHz)	6 pF to 10 pF (±10%)	0 Ω
TDK, Ltd. (ceramic oscillator elements)	FCR 16.93M2G (16.93 MHz)	15 pF (±10%)	100 Ω (±10%)
	FCR 16.93MCG (16.93 MHz)	30 pF (Includes built-in capacitors)	47 Ω (±10%)

Since the conditions for the load capacitors C_{in} and C_{out} used varies with the printed circuit board, this circuit must be tested on the printed circuit board actually used.

25. 16M and 4.2M Pins; Pin 71: 16M, pin 72: 4.2M

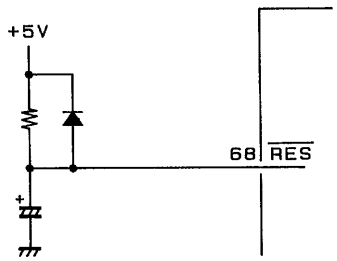
In normal- and double-speed playback modes, the 16M pin buffer outputs the 16.9344 MHz external crystal oscillator 16.9344 MHz signal. The 4.2M pin supplies the LA9231M or LA9231M system clock, normally outputting a 4.2336 MHz signal. When the oscillator is turned off both these pins will be fixed at either high or low.

26. Reset Circuit; Pin 68: $\overline{\text{RES}}$

When power is first applied, this pin should be briefly set low and then set high. This will set the muting to –∞ dB and stop the disk motor.

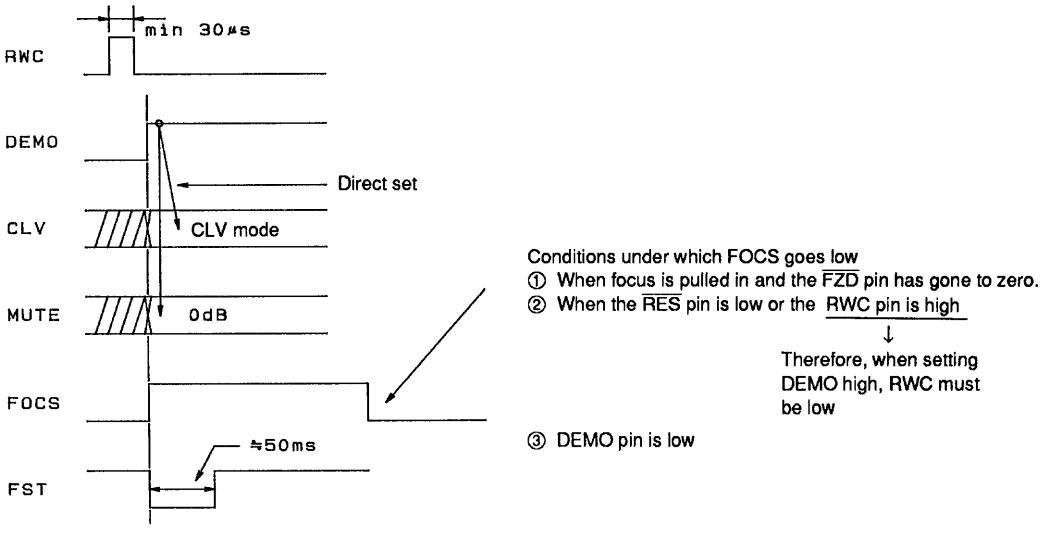
Constant linear velocity servo	START	[STOP]	BRAKE	CLV
Muting control	0 dB	–12 db	[–∞]	
Q subcode address conditions	[Address 1]	Address free		
Laser control	ON (low)	[OFF] (high)		
CONT	High	[Low]		
Track jump mode	[Standard]	New		
Track count mode	Standard	[New]		
Digital attenuator	[DATA 0]	DATA 00H to EEH		
OSC	[ON]	OFF		
Playback speed	[Normal speed]	Double speed		
Anti-shock mode	ON	[OFF]		
Digital filter normal speed	ON	[OFF]		

Setting the $\overline{\text{RES}}$ pin low sets the LC78621E to the settings enclosed in boxes in the table.



A04137

27. Adjustment Process Sound Output Function; Pin 30: DEMO



A04019

The DEMO pin can be used when the LC78621E is used in combination with an LA9210M or LA9211M.
By setting this pin high, muting can be set to 0 dB, the disk motor can be set to CLV, and a focus start operation can be performed, even without issuing any commands from the control microprocessor. Also, since the $\overline{\text{LASER}}$ pin becomes active, if the mechanism and servo systems are complete, an EFM signal can be acquired with only this equipment, and an audio signal can be produced without the presence of a microprocessor. However, since the digital attenuation is set to 100H, this technique is not appropriate for evaluating audio quality.

28. Other Pins; Pin 2:TAI, pin 80: TEST1, pin 12: TEST2, pin 26: TEST3, pin 31: TEST4, pin 74: TEST5, pin 40: ASDFIR
    These pins are used for testing the LSI's internal circuits. Since the pins TAI and TEST1 to TEST5 have built-in pull-down resistors, they can be left open in normal operation. ASDFIR must be connected to ground in normal operation.

29. Circuit Block Operating Descriptions
    • RAM address control
    The LC78621E incorporates an 8-bit × 2k-word RAM on chip. This RAM has an EFM demodulated data jitter handling capacity of ±4 frames implemented using address control. The LC78621E continuously checks the remaining buffer capacity and controls the data write address to fall in the center of the buffer capacity by making fine adjustments to the frequency divisor in the PCK side of the CLV servo circuit. If the ±4 frame buffer capacity is exceeded, the LC78621E forcibly sets the write address to the ±0 position. However, since the errors that occur due to this operation cannot be handled with error flag processing, the IC applies muting to the output for a 128 frame period.

Position	Division ratio or processing	
–4 or less	Force to ±0	
–3	589	Increase ratio
–2	589	
–1	589	
±0	588	Standard ratio
+1	587	Decrease ratio
+2	587	
+3	587	
+4 or more	Force to ±0	

- C1 and C2 Error Correction

  The LC78621E writes EFM demodulated data to internal RAM to compensate for jitter and then performs the following processing with uniform timing based on the crystal oscillator clock. First, the LC78621E performs C1 error checking and correction in the C1 block, determines the C1 flags, and writes the C1 flag register. Next, the LC78621E performs C2 error checking and correction in the C2 block, determines the C2 flags, and writes data to internal RAM.

C1 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Correction · Flag set
3 errors or more	Correction not possible · Flag set

C2 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Depends on C1 flags*1
3 errors or more	Depends on C1 flags*2

Note: 1. If the positions of the errors determined by the C2 check agree with those specified by the C1 flags, the correction is performed and the flags are cleared. However, if the number of C1 flags is 7 or higher, C2 correction may fail. In this case correction is not performed and the C1 flags are taken as the C2 flags without change. Error correction is not possible if one error position agrees and the other does not. Furthermore, if the number of C1 flags is 5 or under, the C1 check result can be seen as unreliable. Accordingly, the flags will be set in this case. Cases where the number of C1 flags is 6 or more are handled in the same way, and the C1 flags are taken as the C2 flags without change. When there is not even one agreement between the error positions, error correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. In other cases, the C1 flags are taken as the C2 flags without change.

2. When data is determined to have three or more errors and be uncorrectable, correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. In other cases the C1 flags are taken as the C2 flags without change

30. Command Summary Table

Blank entry: Illegal command, #: Changed or added command, *: latching commands (mode setting commands), ○: Commands shared with an ASP (LA9230M/31M or other processor), Items in parentheses are ASP commands (provided for reference purposes)

00000000	(ADJ.reset)	00100000	* TOFF low in TJ mode	01000000	* UBIT ON	01100000	
00000001	* MUTE 0 dB	00100001	* TOFF high in TJ mode	01000001	* UBIT OFF	01100001	
00000010	* MUTE –12 dB	00100010	* New TRACK COUNT	01000010	* DOUT ON	01100010	
00000011	* MUTE –∞ dB	00100011	* Old TRACK COUNT	01000011	* DOUT OFF	01100011	
00000100	* DISC MTR START	00100100		01000100		01100100	
00000101	* DISC MTR CLV	00100101		01000101		01100101	
00000110	* DISC MTR BRAKE	00100110		01000110		01100110	
00000111	* DISC MTR STOP	00100111		01000111		01100111	
00001000	○ FOCUS START #1	00101000	* STO CONT	01001000		01101000	
00001001	* ADDRESS FREE	00101001	* LCH CONT	01001001		01101001	
00001010	* LASER ON	00101010	* RCH CONT	01001010		01101010	
00001011		00101011	* PKM SET	01001011		01101011	* #ANTIC off
00001100		00101100	* LVM SET	01001100		01101100	* #ANTIC on
00001101		00101101	* PKM MSK SET	01001101		01101101	
00001110	* CONT SET	00101110	* PKM MSK RESET	01001110		01101110	* #DF normal speed off
00001111	* TRACKING OFF	00101111		01001111		01101111	* #DF normal speed on
00010000	2TJ IN	00110000	32TJ IN	01010000		01110000	
00010001	1TJ IN #1	00110001	1TJ IN #3	01010001		01110001	
00010010	1TJ IN #2	00110010		01010010	1TJ IN #4	01110010	
00010011	4TJ IN	00110011		01010011		01110011	
00010100	16TJ IN	00110100		01010100		01110100	
00010101	64TJ IN	00110101		01010101		01110101	
00010110	256TC	00110110		01010110		01110110	
00010111	128TJ IN	00110111		01010111		01110111	
00011000	2TJ OUT	00111000	32TJ OUT	01011000		01111000	
00011001	1TJ OUT #1	00111001	1TJ OUT #3	01011001		01111001	
00011010	1TJ OUT #2	00111010		01011010	1TJ OUT #4	01111010	
00011011	4TJ OUT	00111011		01011011		01111011	
00011100	16TJ OUT	00111100		01011100		01111100	
00011101	64TJ OUT	00111101		01011101		01111101	
00011110		00111110		01011110		01111110	
00011111	128TJ OUT	00111111		01011111		01111111	

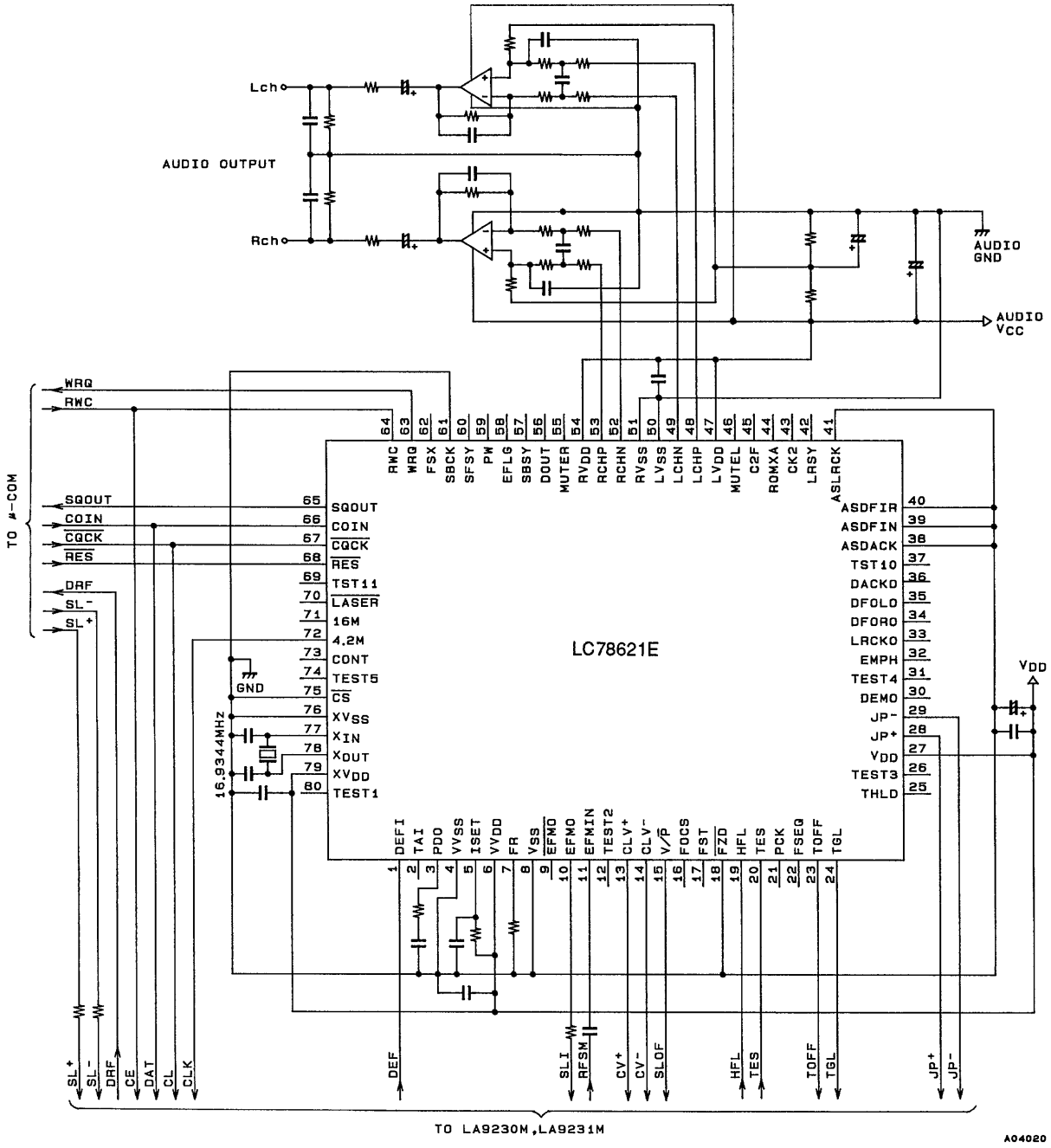
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Blank entry: Illegal command, #: Changed or added command, *: latching commands (mode setting commands), ○: Commands shared with an ASP (LA9230M/31M or other processor), Items in parentheses are ASP commands (provided for reference purposes)

10000000	* #ATT 0 dB SET	10100000	* Old TRK JMP	11000000		11100000	
10000001	* #ATT DATA SET	10100001	* New TRK JMP	11000001	* Double-speed playback	11100001	
10000010	* #ATT 4STP UP	10100010	FOCS START #2	11000010	* Normal-speed playback	11100010	
10000011	* #ATT 4STP DWN	10100011	* Internal BRKE CONT	11000011		11100011	
10000100	* #ATT 8STP UP	10100100		11000100	* Internal BRK OFF	11100100	
10000101	* #ATT 8STP DWN	10100101		11000101	* Internal BRK ON	11100101	
10000110	* #ATT 16STP UP	10100110		11000110		11100110	
10000111	* #ATT 16STP DWN	10100111		11000111		11100111	
10001000	* CDROMXA	10101000	* DISC 8 SET	11001000		11101000	
10001001	* ADDRESS 1	10101001	* DISC 12 SET	11001001	* #CK2 polarity inverted	11101001	
10001010	* LASER OFF	10101010		11001010	* Internal BRK-DMC low	11101010	
10001011	* CONT, ROMXA RST	10101011		11001011	* Internal BRK-DMC high	11101011	
10001100	TRACK JMP BRK	10101100		11001100	* TOFF during internal BRK	11101100	
10001101	* OSC OFF	10101101		11001101	* TON during internal BRK	11101101	
10001110	* OSC ON	10101110		11001110		11101110	* Command noise OFF
10001111	* TRACKING ON	10101111		11001111		11101111	* Command noise ON
10010000	(* F.OFF.ADJ.ST)	10110000	* CLV-PH 1/1 mode	11010000		11110000	* ○ TRCK CHECK IN (2BYTEDETECT)
10010001	(* F.OFF.ADJ.OFF)	10110001	* CLV-PH 1/2 mode	11010001		11110001	
10010010	(* T.OFF.ADJ.ST)	10110010	* CLV-PH 1/4 mode	11010010		11110010	
10010011	(* T.OFF.ADJ.OFF)	10110011	* CLV-PH 1/8 mode	11010011		11110011	
10010100	(* LSR.ON)	10110100	* CLV3ST output ON	11010100		11110100	
10010101	(* LSR.OF/F.SV.ON)	10110101	* CLV3ST output OFF	11010101		11110101	
10010110	(* LSR.OF/F.SV.OF)	10110110	* JP3ST output ON	11010110		11110110	
10010111	(* SP.8CM)	10110111	* JP3ST output OFF	11010111		11110111	
10011000	(* SP.12CM)	10111000		11011000		11111000	* ○ TRCK CHECK OUT (2BYTE DETECT)
10011001	(* SP.OFF)	10111001		11011001		11111001	
10011010	(* SLED.ON)	10111010		11011010		11111010	
10011011	(* SLED.OFF)	10111011		11011011		11111011	
10011100	(* EF.BAL.START)	10111100		11011100		11111100	
10011101	(* T.SERVO.OFF)	10111101		11011101		11111101	
10011110	(* T.SERVO.ON)	10111110		11011110		11111110	# ○ NOTHING
10011111		10111111		11011111		11111111	* ○ 2BYTE CMD RST

31. Sample Application Circuit



32. CD-DSP Functional Comparison

Function \ Product	LC7860KA	LC7861NE→ LC7861KE	LC7867E	LC7868E → LC7868KE	LC7869E	LC78681E → LC78681KE	LC78621E
EFM-PLL	When paired with an analog ASP	When paired with an analog ASP	When paired with an analog ASP	When paired with an analog ASP	When paired with an analog ASP	When paired with an analog ASP	Built-in VCO
16 KRAM	External	○	○	○	○	○	○
Digital output	×	○	○	○	○	○	○
Interpolation	2	4	4	4	4	4	4
Zero-cross muting	×	○	○	○	○	○	○
Level meter Peak meter	×	×	×	○	○	○	○
Bilingual	×	×	×	○	○	○	○
Digital attenuator	×	×	×	×	×	×	○
2fs	○	○	—	—	—	—	—
4fs	—	—	—	○	—	—	—
8fs	—	—	—	—	○	—	○
Digital de-emphasis	×	×	×	○	○	×	○
1 bit DAC	×	×	×	×	×	×	○

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