Precision, High Speed Operational Amplifier

DESCRIPTION

The RH118 is a precision, high speed operational amplifier which offers wide bandwidth and high slew rate. Unlike many wideband amplifiers, the RH118 is unity-gain stable and has a slew rate of 50V/µs.

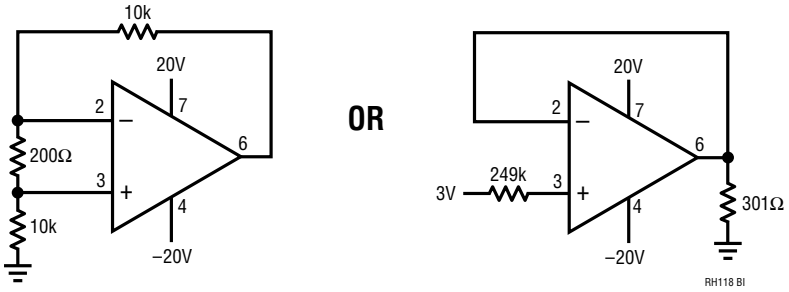
The wafer lots are processed to Linear Technology's in-house Class S flow to yield circuits usable in stringent military applications.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

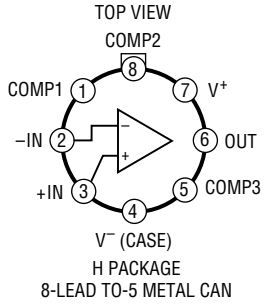
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

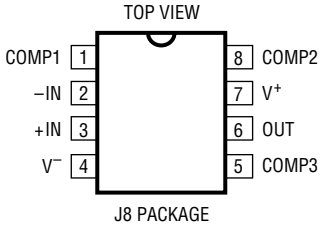
BURN-IN CIRCUIT (Each Amplifier)



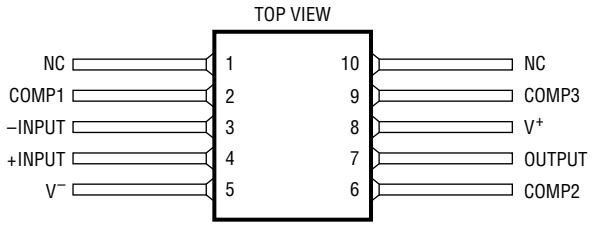
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN



J8 PACKAGE
8-LEAD CERDIP



W PACKAGE
10-LEAD CERPAC

TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−55°C T_A 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage					4	1			6	2,3	mV
I_{OS}	Input Offset Current					50	1			100	2,3	nA
I_B	Input Bias Current					250	1			500	2,3	nA
R_{IN}	Input Resistance		4	1								M
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L 2k		50			1	25			2,3	V/mV
SR	Slew Rate	V_S = ±15V, A_V = 1	5	50								V/µs
GBW	Gain Bandwidth Product	V_S = ±15V			15							MHz
	Output Voltage Swing	V_S = ±15V, R_L = 2k		±12			4	±12			5,6	V
	Input Voltage Range	V_S = ±20V		±16.5			1	±16.5			2,3	V
I_S	Supply Current					8	1					mA
		T_A = 125°C								7	2	mA
CMRR	Common Mode Rejection Ratio			80			1	80			2,3	dB
PSRR	Power Supply Rejection Ratio			70			1	70			2,3	dB

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 6)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage				4		4		4		4		10	mV
I_{OS}	Input Offset Current				50		50		50		50		100	nA
I_B	Input Bias Current				250		250		250		300		400	nA
R_{IN}	Input Resistance		4	1		1		1		0.5		0.5		M
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L 2k		50		50		50		50		25		V/mV
SR	Slew Rate	V_S = ±15V, A_V = 1	5	50		50		50		50		50		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V			15(Typ)		15(Typ)		15(Typ)		15(Typ)		15(Typ)	MHz
	Output Voltage Swing	V_S = ±15V, R_L = 2k		±12		±12		±12		±12		±12		V
	Input Voltage Range			±16.5		±16.5		±16.5		±15		±12		V
I_S	Supply Current				8		8		8		8		8	mA
CMRR	Common Mode Rejection Ratio			80		80		80		80		70		dB
PSRR	Power Supply Rejection Ratio			70		70		70		70		60		dB

ELECTRICAL CHARACTERISTICS (Continued)

Note 1: The inputs are shunted with back-to-back Zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for ±5V V_S ±20V. The power supplies must be bypassed with a 0.1µF or greater disc capacitor within four inches of the device.

Note 4: Guaranteed by design, characterization or correlation to other tested parameters.

Note 5: Slew rate is 100% tested at wafer probe testing. It is QA sample tested in finished package form.

Note 6: T_A = 25°C, V_S = ±20V, V_{CM} = 0V, unless otherwise specified. Supply bypassed per Note 3.

TOTAL DOSE BIAS CIRCUIT

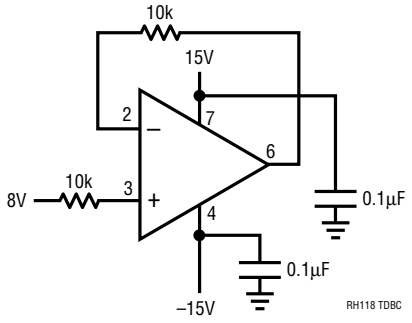


TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group C and D End Point Electrical Parameters (Method 5005)	1

* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

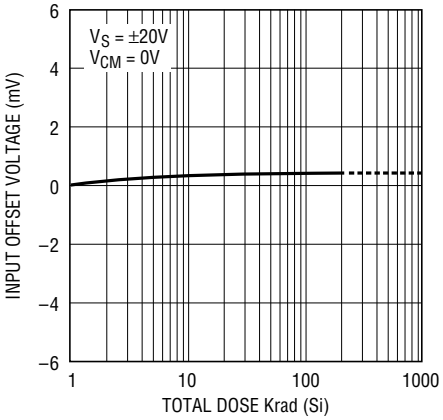
The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

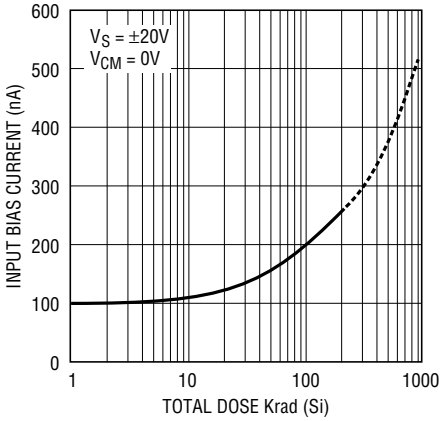
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



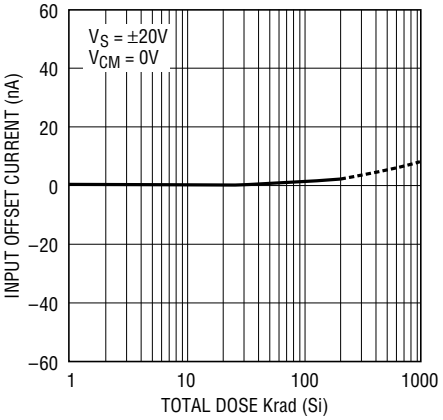
RH118 G01

Input Bias Current



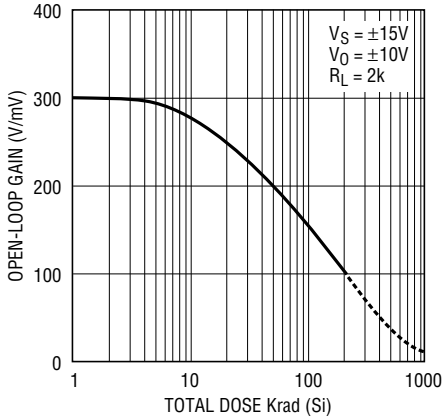
RH118 G03

Input Offset Current



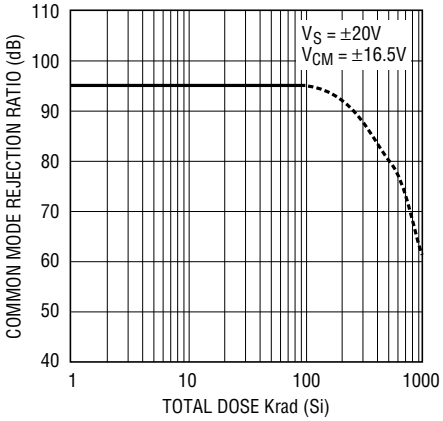
RH118 G05

Open-Loop Gain



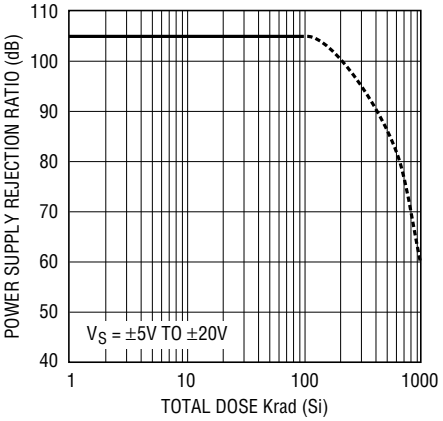
RH118 G02

Common Mode Rejection Ratio



RH118 G04

Power Supply Rejection Ratio



RH118 G06

I.D. No. 66-11-0118 Rev. A 0796

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/HP 0796 REV A 500 • PRINTED IN USA

© LINEAR TECHNOLOGY CORPORATION 1989