DRV8434A Stepper Driver With Integrated Current Sense, 1/256 Microstepping, smart tune and Stall Detection using GPIO pins

1 Features

- PWM Microstepping Stepper Motor Driver
  - Simple STEP/DIR Interface
  - Up to 1/256 Microstepping Indexer
- Integrated Current Sense Functionality
  - No Sense Resistors Required
  - ±4% Full-Scale Current Accuracy
- Smart tune ripple control decay
- Stall Detection using GPIO pins
- 4.5 to 48-V Operating Supply Voltage Range
- Low $R_{DS(ON)}$: 330 mΩ HS + LS at 24 V, 25°C
- High Current Capacity: 2.5 A Full-Scale, 1.8 A rms
- Supports 1.8 V, 3.3 V, 5.0 V Logic Inputs
- Low-Current Sleep Mode (2 µA)
- Spread spectrum clocking for low EMI
- Small Package and Footprint
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Sensorless stall detection
  - Open Load Detection (OL)
  - Thermal Shutdown (OTSD)
  - Fault Condition Output (nFAULT)

2 Applications

- Printers and Scanners
- ATM and Money Handling Machines
- Textile Machines
- Stage Lighting Equipment
- Office and Home Automation
- Factory Automation and Robotics
- Medical Applications
- 3D Printers

3 Description

The DRV8434A is a stepper motor driver for industrial and consumer applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8434A is capable of driving up to 2.5 A full-scale output current (dependent on PCB thermal design).

The DRV8434A uses an internal current sense architecture to eliminate the need for two external power sense resistors, saving PCB area and system cost. The device uses an internal PWM current regulation scheme with smart tune ripple control decay. Smart tune automatically adjusts for optimal current regulation, compensates for motor variation and aging effects and reduces audible noise from the motor.

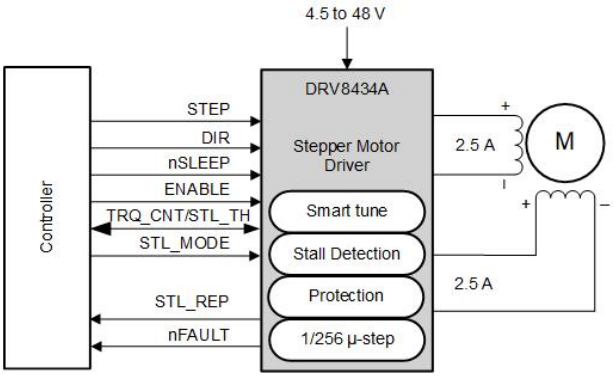
A simple STEP/DIR interface allows an external controller to manage the direction and step rate of the stepper motor. The device can be configured in full-step to 1/256 microstepping. A low-power sleep mode is provided using a dedicated nSLEEP pin.

The DRV8434A features advanced stall detection algorithm configurable by two digital IO and one analog IO pins, and does not require an SPI interface to detect stall. By detecting motor stall, system designers can identify if the motor was obstructed and take action as needed which can improve efficiency, prevent damage and reduce audible noise. Other protection features include supply undervoltage, charge pump faults, overcurrent, short circuits, open load, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
DRV8434APWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8434ARGER	VQFN (24)	4mm x 4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Pin Configuration and Functions

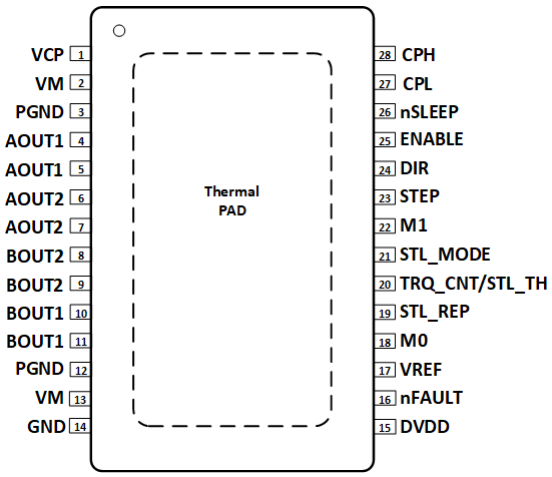


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

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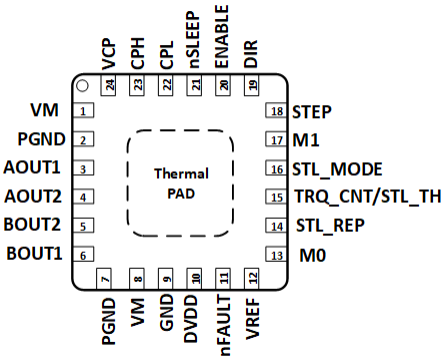


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View

5.1 Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	4, 5	3	O	Output	Winding A output. Connect to stepper motor winding.
AOUT2	6, 7	4	O	Output	Winding A output. Connect to stepper motor winding.
PGND	3, 12	2, 7	—	Power	Power ground. Connect to system ground.
BOUT2	8, 9	5	O	Output	Winding B output. Connect to stepper motor winding
BOUT1	10, 11	6	O	Output	Winding B output. Connect to stepper motor winding
CPH	28	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	22			
DIR	24	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
ENABLE	25	20	I	Input	Logic low to disable device outputs; logic high to enable device outputs; Hi-Z to enable 8x torque count scaling.
DVDD	15	10	—	Power	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	14	9	—	Power	Device ground. Connect to system ground.
VREF	17	12	I	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
M0	18	13	I	Input	Microstepping mode-setting pins. Sets the step mode.
M1	22	17			
STL_MODE	21	16	I	Input	Pin input level programs the stall detection mode: 0 = Torque count mode, torque count analog voltage is output on the TRQ_CNT/STL_TH pin. Hi-Z = Learning mode, learning result analog voltage is output on the TRQ_CNT/STL_TH pin. 1 = Stall threshold mode, stall threshold is set by an input voltage on the TRQ_CNT/STL_TH pin. Tied to ground with a 330k resistor = Stall detection disabled.
TRQ_CNT/STL_TH	20	15	I/O	Input/Output	Torque count analog output or stall threshold analog input depending on STL_MODE pin input level. A 1nF capacitor must be connected from this pin to ground.
STEP	23	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
VCP	1	24	—	Power	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.

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PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
VM	2, 13	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
STL_REP	19	14	O	Open Drain	Stall fault report output. Requires a pullup resistor. A low to high transition indicates a stall. A high to low transition indicates a successful learning. If this pin is connected to ground, stall fault reporting is disabled.
nFAULT	16	11	O	Open Drain	Fault output. Pulled logic low when a fault is detected; open-drain output. Requires a pullup resistor.
nSLEEP	26	21	I	Input	Sleep mode control. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, STL_MODE, STL_REP, TRQ_CNT/STL_TH, M0, M1)	–0.3	5.75	V
Open drain output current (nFAULT, STL_REP)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.5	V
V_{VREF}	VREF voltage	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	500(1)	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	2.5(2)	A
I_{rms}	Motor RMS current (xOUTx)	0	1.8(2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		PWP (HTSSOP) 28 PINS	RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	39.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.0	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.2	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
t_{EN}	Enable time	ENABLE = 0/1 to output transition			5	µs
V_{DVDD}	Internal regulator voltage	No external load, 6V < V_{VM} < 48V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6V < V_{VM} < 48V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
TRI-LEVEL INPUTS (M0, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUT (M1, STL_MODE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{IL}	Output pull-up current			10		µA
TORQUE COUNT INPUT/ STALL THRESHOLD OUTPUT (TRQ_CNT/STL_TH)						
V_{O1}	Output low voltage	STL_MODE = 0V	0.1			V
V_{O2}	Output High voltage	STL_MODE = 0V			2.4	V
V_{I1}	Input low voltage	STL_MODE = DVDD	0.1			V
V_{I2}	Input High voltage	STL_MODE = DVDD			2.4	V
N_{BIT}	Torque-count DAC Resolution		12			Bits
C_{LOAD}	TRQ_CNT/STL_TH pin Capacitive Load	R_{LOAD} = Infinite, Phase margin = 45°			1	nF
I_{SHORT}	TRQ_CNT/STL_TH pin short-circuit current	Full scale output shorted to GND		2		mA
t_S	DAC Output voltage settling time	99% of final target		50		µs
CONTROL OUTPUTS (nFAULT, STL_REP)						

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
V_{IL}	Input logic-low voltage	STL_REP, pulled low to disable stall reporting	0		0.6	V
V_{IH}	Input logic-high voltage	STL_REP, pulled high to enable stall reporting	1.5		5.5	V
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1 A		165	200	mΩ
		T_J = 125 °C, I_O = -1 A		250	300	mΩ
		T_J = 150 °C, I_O = -1 A		280	350	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1 A		165	200	mΩ
		T_J = 125 °C, I_O = 1 A		250	300	mΩ
		T_J = 150 °C, I_O = 1 A		280	350	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V	1.254	1.32	1.386	V/A
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			8.25	µA
ΔI_{TRIP}	Current trip accuracy	0.25 A < I_O < 0.5 A	–12		12	%
		0.5 A < I_O < 1 A	–6		6	
		1 A < I_O < 2.5 A	–4		4	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 2.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	4			A
t_{OCP}	Overcurrent deglitch time			2		µs
t_{RETRY}	Overcurrent retry time			4		ms
t_{OL}	Open load detection time				50	ms
I_{OL}	Open load current threshold			75		mA
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500(1)	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

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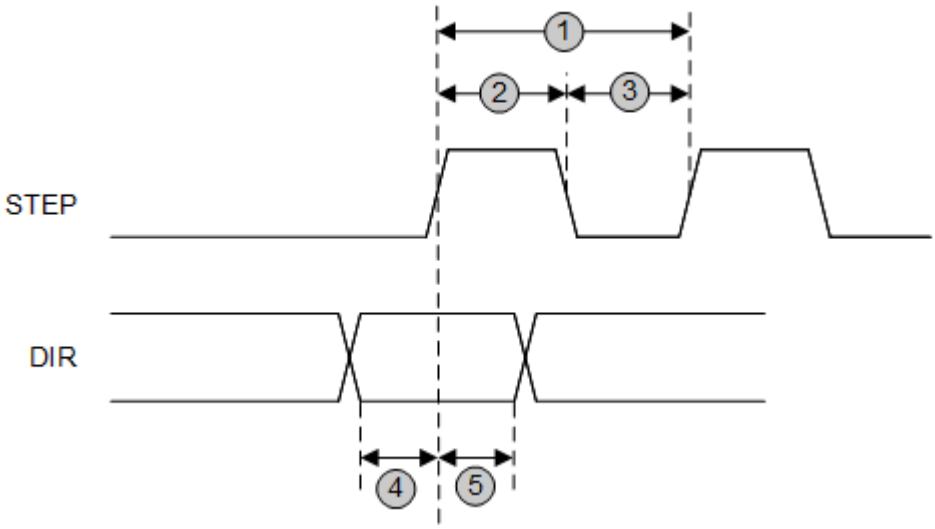


Figure 6-1. STEP and DIR Timing Diagram

6.6.1 Typical Characteristics

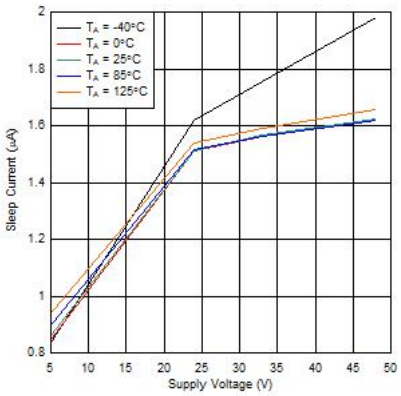


Figure 6-2. Sleep Current over Supply Voltage

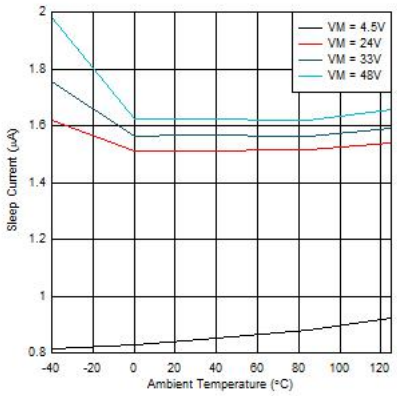


Figure 6-3. Sleep Current over Temperature

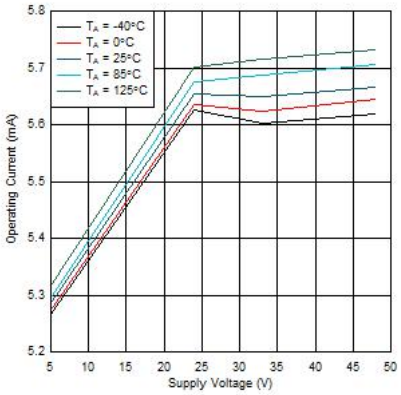


Figure 6-4. Operating Current over Supply Voltage

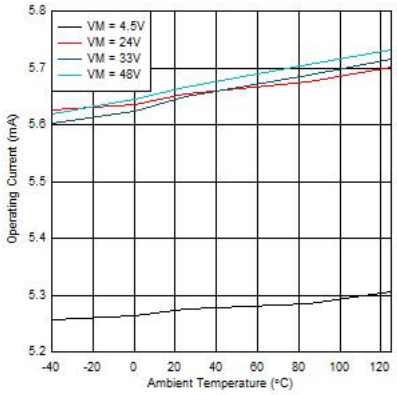


Figure 6-5. Operating Current over Temperature

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6.6.1 Typical Characteristics (continued)

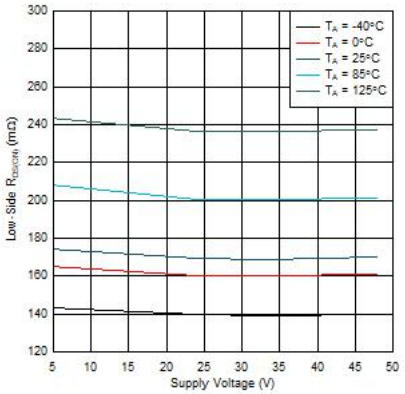


Figure 6-6. Low-Side $R_{DS(ON)}$ over Supply Voltage

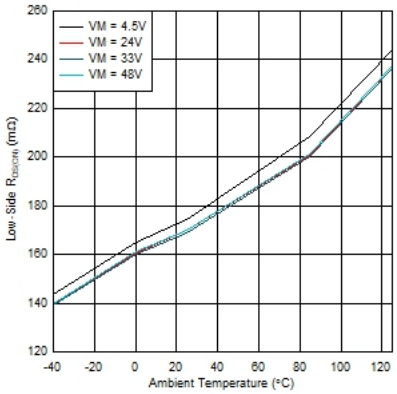


Figure 6-7. Low-Side $R_{DS(ON)}$ over Temperature

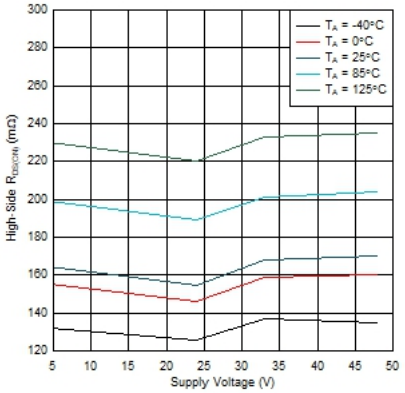


Figure 6-8. High-Side $R_{DS(ON)}$ over Supply Voltage

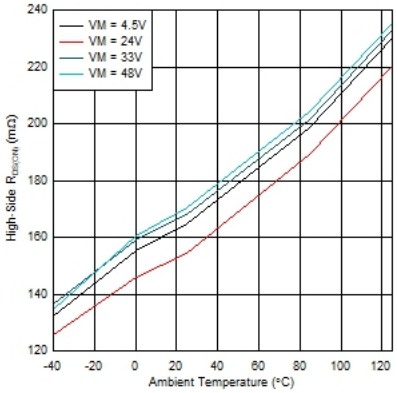


Figure 6-9. High-Side $R_{DS(ON)}$ over Temperature

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7 Detailed Description

7.1 Overview

The DRV8434A is an integrated motor-driver solution for bipolar stepper motors. The device provides maximum integration by integrating two N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and a microstepping indexer. The DRV8434A is capable of supporting a wide supply voltage of 4.5 to 48 V. DRV8434A provides an output current up to 4 A peak, 2.5 A full-scale, or 1.8 A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8434A uses an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin.

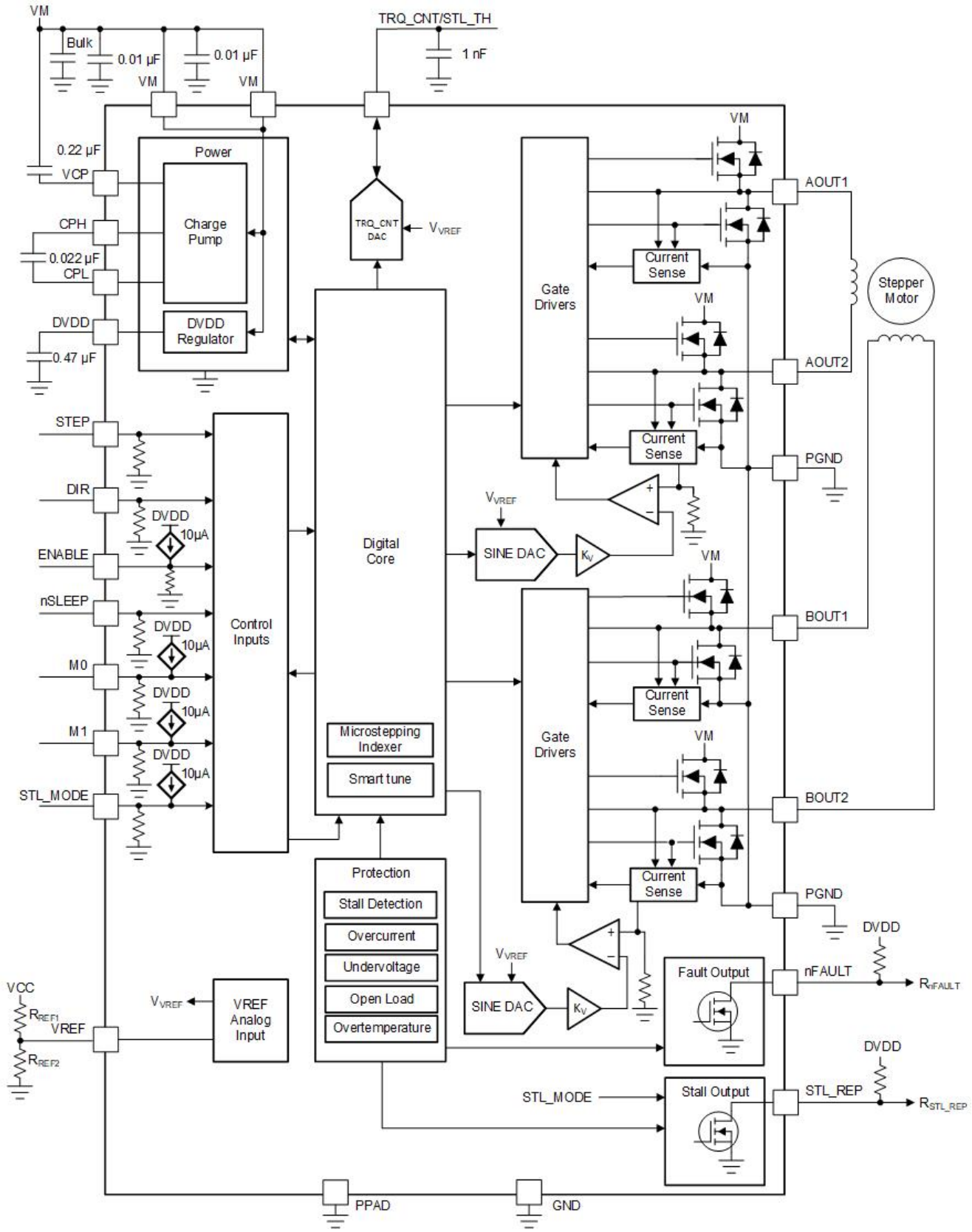
A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

The device operates with smart tune ripple control decay mode, which uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. The DRV8434A can detect a motor overload stall condition or an end-of-line travel, by detecting back-emf phase shift between rising and falling current quadrants of the motor current. Unlike conventional stall detection algorithms which require an SPI interface, the DRV8434A detects stall using two digital IO and one analog IO pins.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature minimizes the radiated emissions from the device. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

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7.2 Functional Block Diagram



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7.3 Feature Description

Table 7-1 lists the recommended external components for the DRV8434A device.

Table 7-1. DRV8434A External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
C_{TRQ_CNT}	TRQ_CNT/STL_TH	GND	X7R, 1-nF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{STL_REP}	VCC (1)	STL_REP	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. VREF pin has an internal 500 kΩ resistor to GND, therefore it is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50 kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the DRV8434A, but a VCC supply voltage pullup is required for open-drain outputs nFAULT and STL_REP; both outputs may also be pulled up to DVDD

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8434A, the peak current rating is 4 A per bridge.

7.3.1.2 RMS Current Rating

The RMS (average) current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8434A, the RMS current rating is 1.8 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

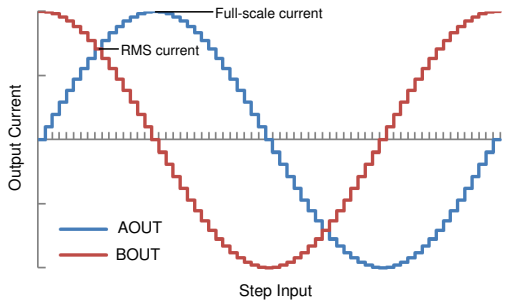


Figure 7-1. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

The DRV8434A has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-2 shows a block diagram of the circuitry.

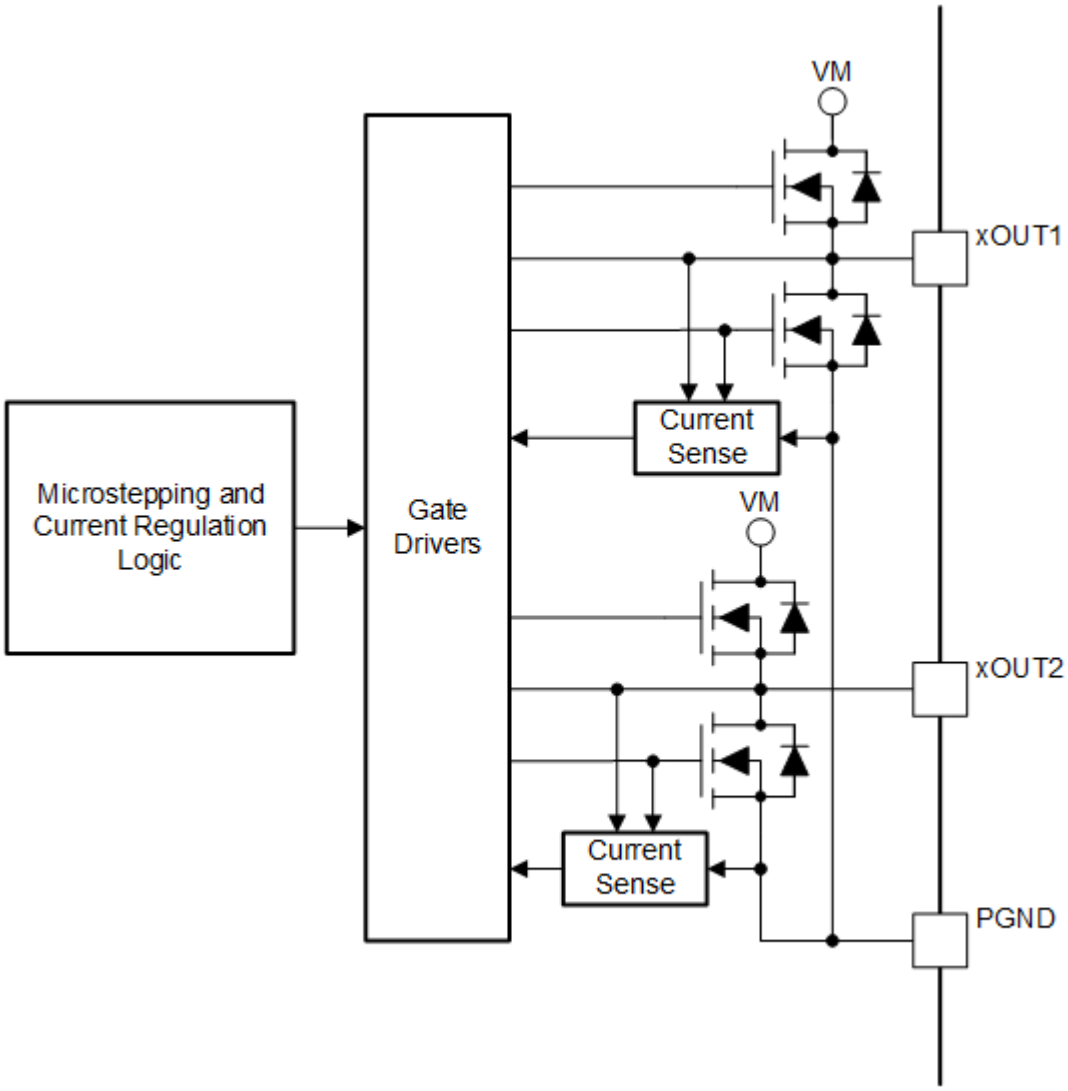


Figure 7-2. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8434A device allows a number of different step modes. The M0 and M1 pins are used to configure the step mode as shown in Table 7-2. The settings can be changed on the fly.

Table 7-2. Microstepping Indexer Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step

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Table 7-2. Microstepping Indexer Settings (continued)

M0	M1	STEP MODE
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

Table 7-3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed.

Note

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered immediately after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 7-3. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50

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Table 7-3. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	-100	100	135
3	-100	-100	225
4	100	–100	315

Table 7-5 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-5. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC must not exceed 3.3 V.

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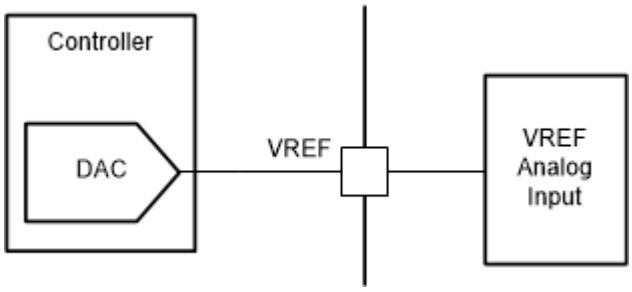


Figure 7-3. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

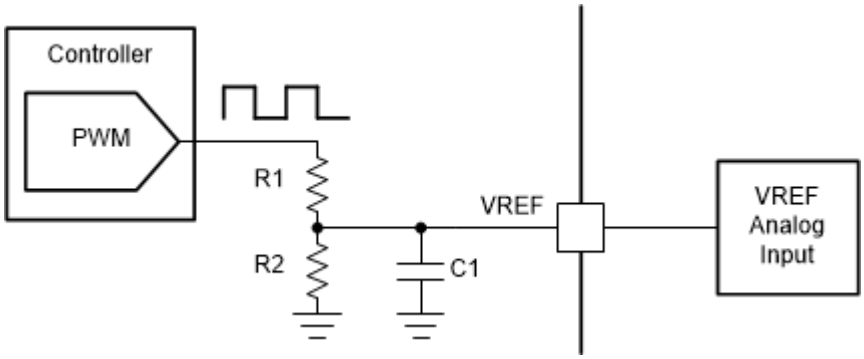


Figure 7-4. Controlling VREF With a PWM Resource

7.3.5 Current Regulation and Decay Mode

The DRV8434A operates with smart tune ripple control decay mode, which uses only slow decay during PWM current regulation. The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin.

The full-scale regulation current (I_{FS}) can be calculated as I_{FS} (A) = V_{REF} (V) / K_V (V/A) = V_{REF} (V) / 1.32 (V/A).

During PWM current chopping, the H-bridge is enabled to drive a current through the motor winding until the PWM current chopping threshold is reached. Thereafter, the winding current is re-circulated by enabling both low-side MOSFETs of the H-bridge.

7.3.5.1 Smart tune Ripple Control

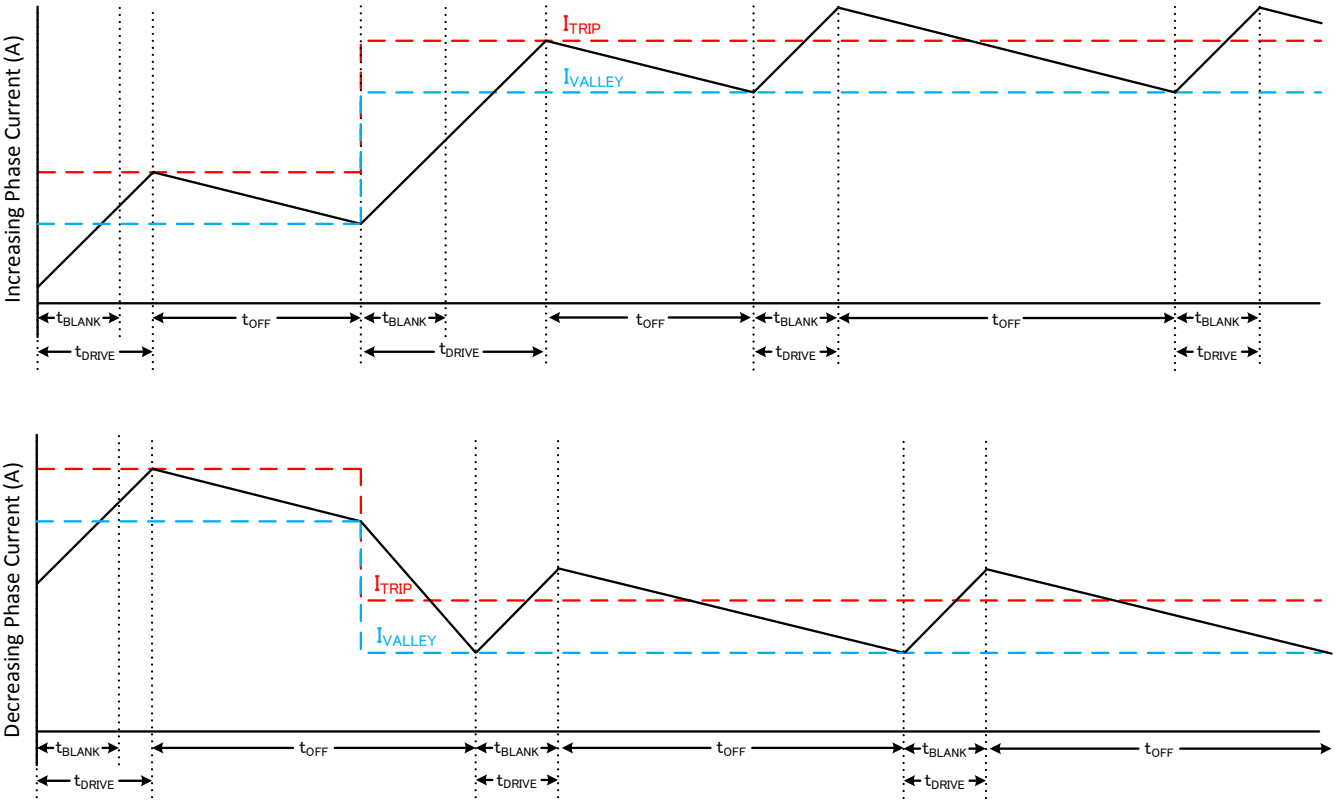


Figure 7-5. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, the driver enters slow decay until I_{VALLEY} is reached. In slow decay, both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, off-time varies depending on the current level and operating conditions.

The ripple control method allows tight regulation of the current level increasing motor efficiency and system performance.

7.3.5.2 Blanking Time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

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7.3.6 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

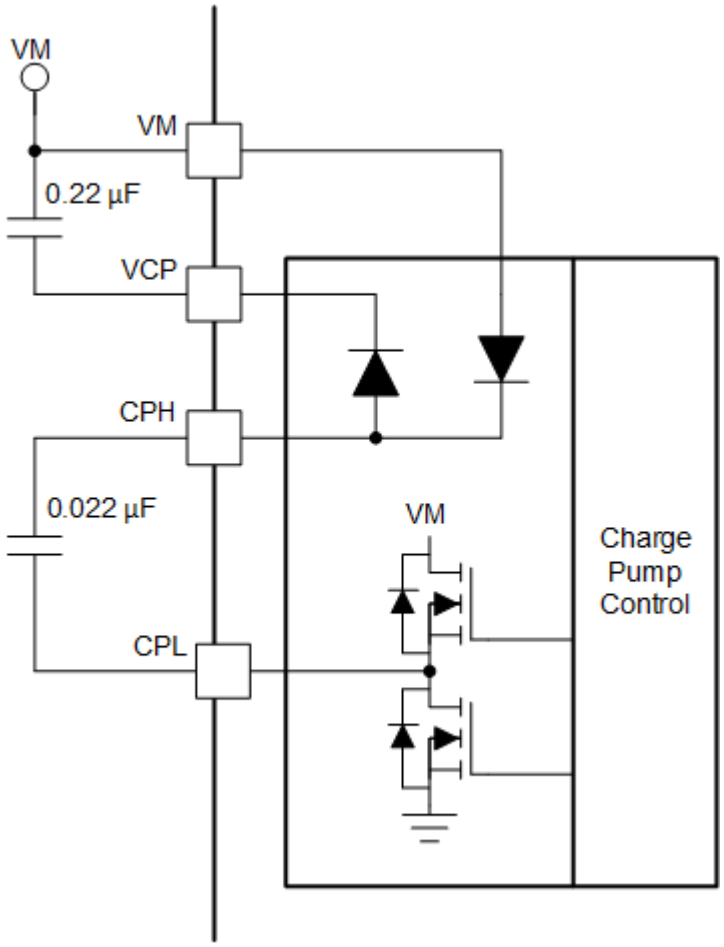


Figure 7-6. Charge Pump Block Diagram

7.3.7 Linear Voltage Regulators

A linear voltage regulator is integrated in the device for DVDD. The DVDD regulator can be used to provide VREF reference voltage. DVDD can supply a maximum of 2mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5 V. When the DVDD LDO current load exceeds 2mA, the output voltage drops significantly.

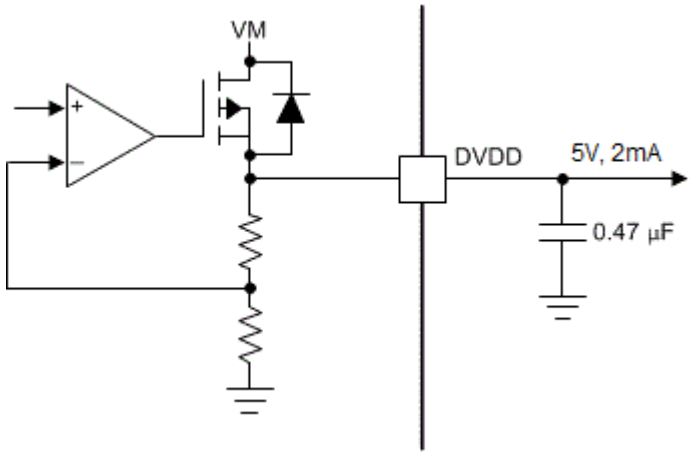


Figure 7-7. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, M0, M1 or STL_MODE), tying the input to the DVDD pin instead of an external regulator is suggested. This method saves power when the VM power is not applied or the device is in sleep mode. The DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin must not be tied to DVDD, else the device will never exit sleep mode.

7.3.8 Logic Level, tri-level and quad-level Pin Diagrams

Figure 7-8 shows the input structure for M0, STL_MODE and ENABLE pins.

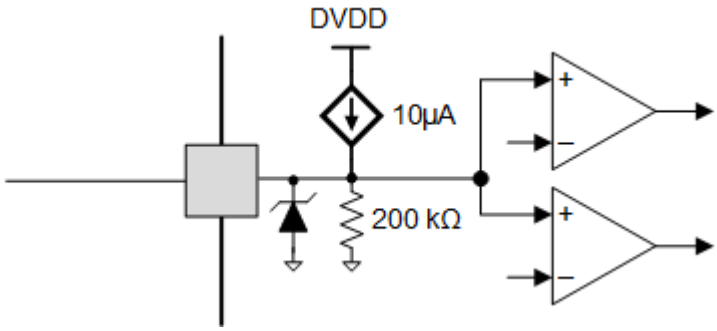


Figure 7-8. Tri-Level Input Pin Diagram

Figure 7-9 shows the input structure for M1 pin.

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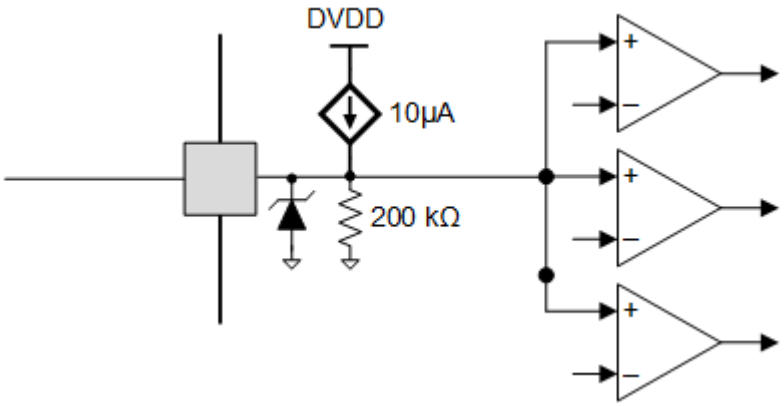


Figure 7-9. Quad-Level Input Pin Diagram

Figure 7-10 shows the input structure for STEP, DIR and nSLEEP pins.

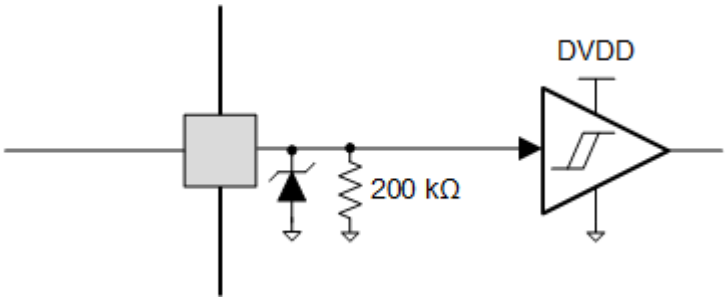


Figure 7-10. Logic-Level Input Pin Diagram

7.3.8.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5 V, 3.3 V or 1.8 V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5 V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3 V or 1.8 V pullup, an external supply must be used.

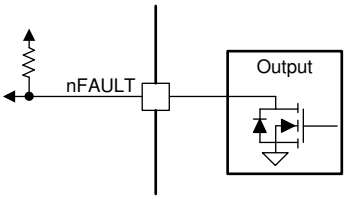


Figure 7-11. nFAULT Pin

- The STL_REP pin has open-drain output and must be pulled up to a 5 V, 3.3 V or 1.8 V supply. When a stall fault is detected, the STL_REP pin will be logic high. After a successful stall threshold learning, STL_REP pin is pulled low. The STL_REP pin can also be used as an input. When pulled low externally, stall fault reporting is disabled. For a 5 V pullup, the STL_REP pin can be tied to the DVDD pin with a resistor. For a 3.3 V or 1.8 V pullup, an external supply must be used.

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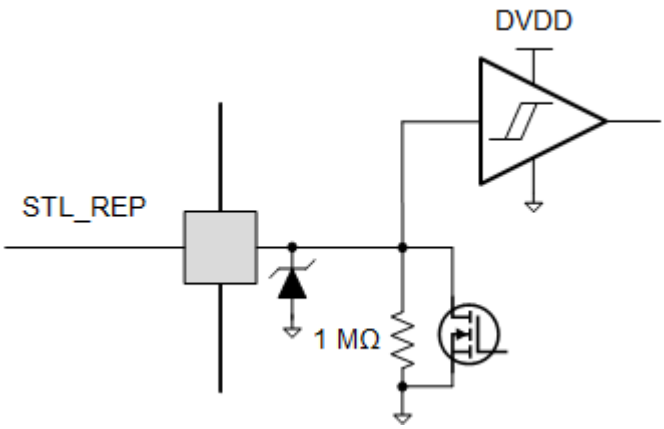


Figure 7-12. STL_REP pin

7.3.9 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events. In addition, the device is protected against stall detection in the event of overload or end-of-line movement.

7.3.9.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.9.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.9.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in both H-bridges are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.9.4 Stall Detection

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in Figure 7-13. As motor load approaches the torque capability of the motor for a given winding current, the back-EMF will move in phase with the winding current.

By detecting back-emf phase shift between rising and falling current quadrants of the motor current, the DRV8434A can detect a motor overload stall condition or an end-of-line travel. Without Stall Detection, driver will continue to drive through the obstacle, causing heating, audible noise and damage to the system.

Stall detection can replace expensive Hall sensors. Integrated sensorless stall detection results in immediate response in the event of motor stall, compared to timeout mechanism of Hall sensors.

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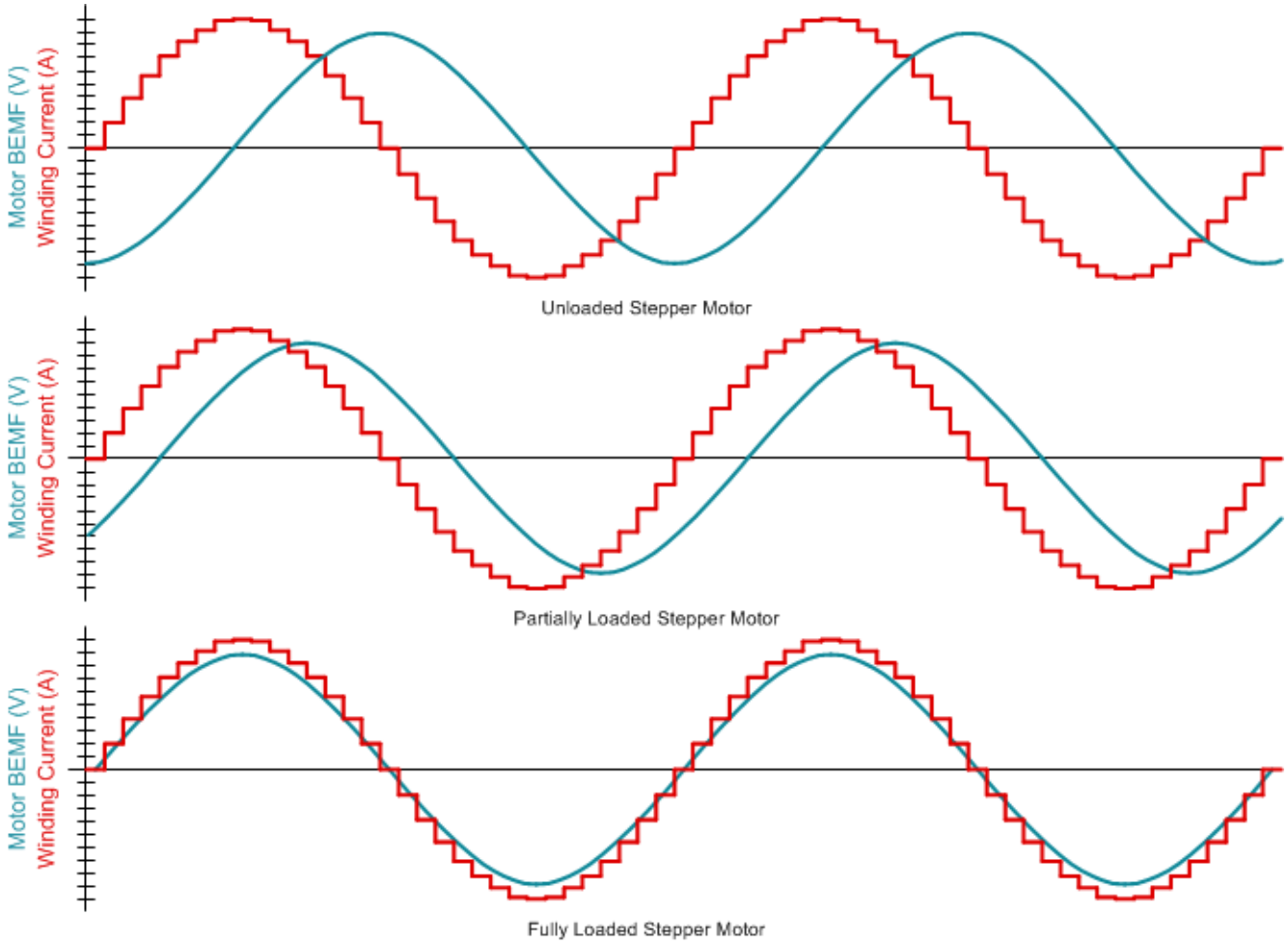


Figure 7-13. Stall Detection by Monitoring Motor Back-EMF

The stall detection algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a value represented by the torque count. The comparison is done in such a way that the torque count is practically independent of motor current, ambient temperature and supply voltage.

For a lightly loaded motor, the torque count will be a non-zero value. As the motor approaches stall condition, torque count will approach zero and can be used to detect stall condition. If anytime torque count falls below the stall threshold, the device will detect a stall. In stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed.

High motor coil resistance can result in low torque count. The ENABLE pin of the DRV8434A allows scaling up low torque count values, for ease of further processing. If the ENABLE pin is Hi-Z, the torque count and stall threshold are multiplied by a factor of 8. If the ENABLE pin is logic high, torque count and stall threshold retain the value originally calculated by the algorithm.

The stall detection algorithm of the DRV8434A is configured by two digital IO and one analog IO pins - STL_MODE, STL_REP and TRQ_CNT/STL_TH.

STL_MODE programs the stall detection mode. When this pin is logic low, stall threshold is computed by the driver or an external microcontroller (MCU). The TRQ_CNT/STL_TH pin outputs as torque count analog voltage. If the STL_MODE pin is open (Hi-Z), it enables the stall threshold learning process. If learning is successful, the TRQ_CNT/STL_TH pin outputs the stall threshold as an analog voltage. When the STL_MODE is logic high (tied to DVDD), stall threshold is set by applying a voltage on the TRQ_CNT/STL_TH pin. TRQ_CNT/STL_TH pin can act as both input or output, depending on the operating mode. An 1 nF capacitor must be connected from the

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TRQ_CNT/STL_TH pin to GND. Connecting a 330k resistor from STL_MODE pin to ground disables stall detection. Additionally, if any fault condition exists (UVLO, OCP, OL, OTSD etc.), stall detection will be disabled.

STL_REP is an open-drain output. When STL_MODE = GND or DVDD, STL_REP is pulled low by the driver if there is no stall fault; and goes high if stall is detected. If STL_MODE = GND or DVDD and the STL_REP pin is pulled low externally, then stall fault reporting is disabled and nFAULT will not go low if a stall is detected. In stall threshold learning mode (STL_MODE = Hi-Z), if STL_REP goes from high to low, it indicates successful stall threshold learning. STL_REP must be pulled up with an external pull-up resistor.

The following procedure describes the stall threshold learning operation:

- Before stall threshold learning, ensure that the motor speed has reached its target value. Do not learn stall threshold while the motor speed is ramping up or down.
- Initiate learning by making the STL_MODE pin Hi-Z.
- Run motor with no load.
- Wait for 32 electrical cycles for the driver to learn the steady count.
- Stall the motor.
- Wait for 16 electrical cycles for the driver to learn the stall count.
- STL_REP will be pulled low if learning is successful.
- Stall threshold is calculated as the average of steady count and stall count.
- At the end of a successful learning, TRQ_CNT/STL_TH pin outputs the stall threshold as an analog voltage, and also stores the value internally for use with Torque Count Mode.
- After successful learning, once device enters Torque Count mode or Stall Threshold mode by changing STL_MODE logic level, STL_REP goes high, nFAULT is pulled down and the voltage on the TRQ_CNT/STL_TH pin is reset.
- Apply nSLEEP reset pulse to pull down STL_REP and pull up nFAULT again.

Sometimes the stall learning process might not be successful due to an unstable torque count while the motor is running or stalled. For example, when the motor has high coil resistance or is running at very high or low speeds, the torque count might vary a lot over time and the difference between steady count and stall count might be small. In such cases, it is recommended not to use the stall learning method. Instead, the user should carefully study the steady count and torque count across the range of operating conditions and set the threshold midway between the minimum steady count and the maximum stall count.

When the motor is intially ramping up speed, it is recommended to configure the driver in either Torque Count Mode or Stall Threshold Mode. If the device is in Learning Mode during the initial ramp up, the learning process might result in a lower stall threshold value. Once steady state speed has been achieved, learning process can be initiated.

Table 7-6 shows all the different operating modes in which stall can be detected.

Table 7-6. Stall Detection Operating Modes

Operating Mode	STL_MODE	TRQ_CNT/STL_TH	STL_REP	nFAULT	Description
Torque Count Mode	GND	Torque count voltage as output	Output:High: Stall Fault Input:Low: Stall Reporting Disabled	If STL_REP > 1.6V, nFAULT goes low when stall is detected	This Mode supports two types of operations: 1. Standalone Stall Detection Mode: Driver takes care of stall detection and reporting (this needs to be preceded by Learning Mode). 2. MCU assisted Stall Detection Mode: MCU takes TRQ_CNT/STL_TH voltage as input, compensates it for any second order effects, and compares it with its own stall threshold value to detect a stall. Because this operating mode is external, the device stall reporting must be disabled. The MCU could also run an algorithm to control VREF based on the torque count.

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Table 7-6. Stall Detection Operating Modes (continued)

Operating Mode	STL_MODE	TRQ_CNT/ STL_TH	STL_REP	nFAULT	Description
Learning Mode	Hi-Z	Stall threshold voltage as output	Output:High: Learning Not done Low: learning Successful	Not Applicable	1. Torque count learning result is available via the TRQ_CNT/ STL_TH pin. 2. In this mode, the motor must spin with no load for at least 32 electrical cycles, then stalled for at least 16 electrical cycles for the stall detection algorithm to determine the internal stall threshold.
Stall Threshold Mode	DVDD	Stall threshold voltage as input	Output:High: Stall Fault Input:Low: Stall Reporting Disabled	If STL_REP > 1.6V, nFAULT goes low when stall is detected	Torque count is noted from Torque Count Mode or Learning Mode and a desired stall threshold voltage is applied to the TRQ_CNT/STL_TH pin. The stall threshold voltage must be less than the torque count noted from the Torque Count Mode. Stall Threshold Mode must be selected while the motor is spinning in Torque Count Mode.
Stall Detection Disabled	330k to GND		Output: Low		Motor stall will be ignored until STL_MODE = 0 or 1.

Figure 7-14 shows the flowchart of stall detection by the DRV8434A driver.

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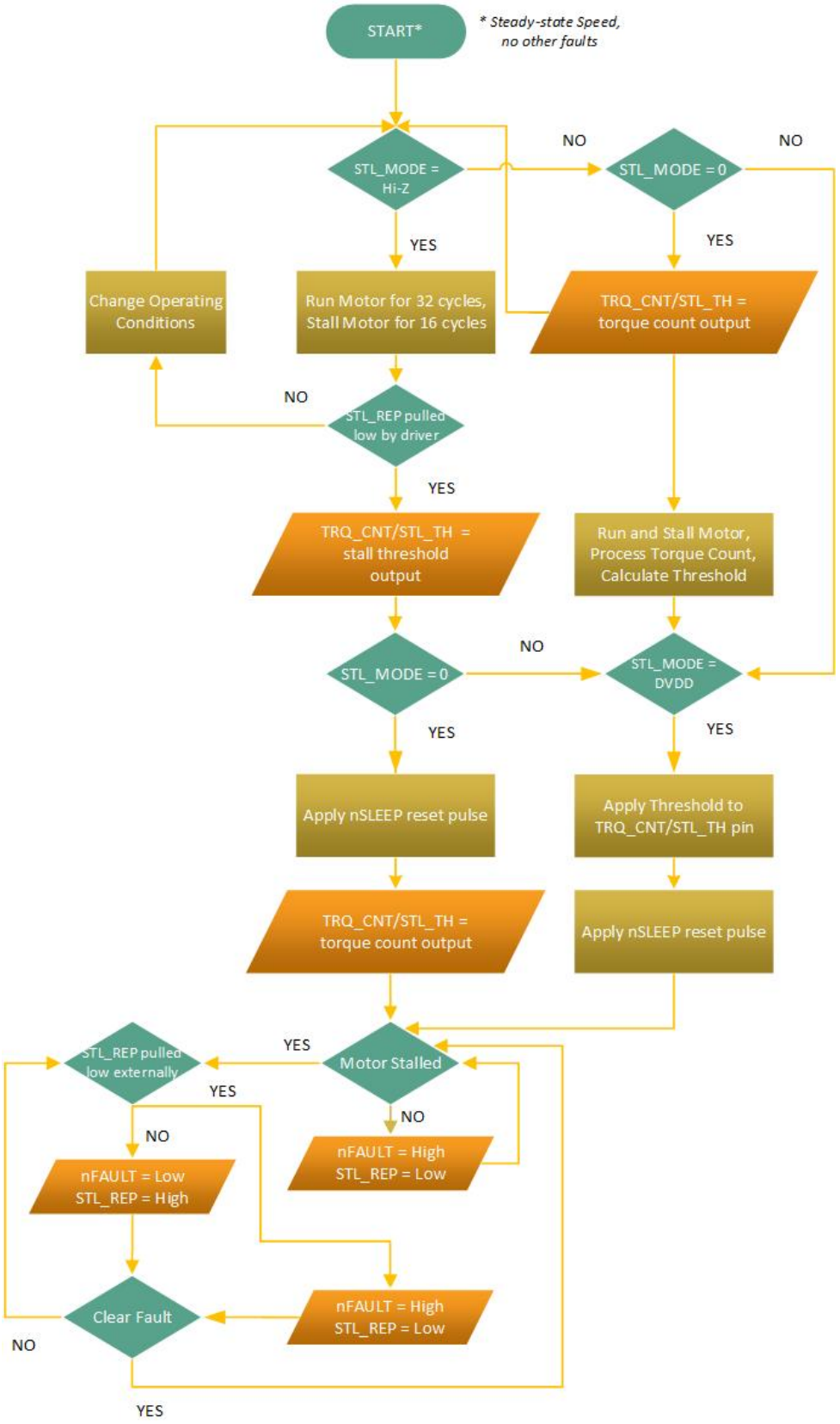


Figure 7-14. Flowchart of Stall Detection by DRV8434A

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7.3.9.5 Open-Load Detection (OL)

If the winding current in any coil drops below the open load current threshold (I_{OL}) and the I_{TRIP} level set by the indexer, and if this condition persists for more than the open load detection time (t_{OL}), an open-load condition is detected. Normal operation resumes when the open load condition is removed. The fault is cleared by an nSLEEP reset pulse or if the device is power cycled or comes out of sleep mode.

7.3.9.6 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled during this condition. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS_OTSD}).

Fault Condition Summary

Table 7-7. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT	Disabled	Operating	Operating	Operating	Automatic: VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	—	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	—	nFAULT	Operating	Operating	Operating	Operating	Report only
Stall Detection (STALL)	Stall / stuck motor	—	STL_REP, nFAULT	Operating	Operating	Operating	Operating	Report Only
Thermal Shutdown (OTSD)	T_J > T_{TSD}	—	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The DRV8434A device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the DRV8434A device enters a low-power sleep mode. In the sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The DRV8434A device is brought out of sleep automatically when the nSLEEP pin is high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the DRV8434A device. When the ENABLE pin is low, the output drivers are disabled and the output pins are in the Hi-Z state.

7.4.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.4 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7-15). This reset pulse does not affect the status of the charge pump or other functional blocks.

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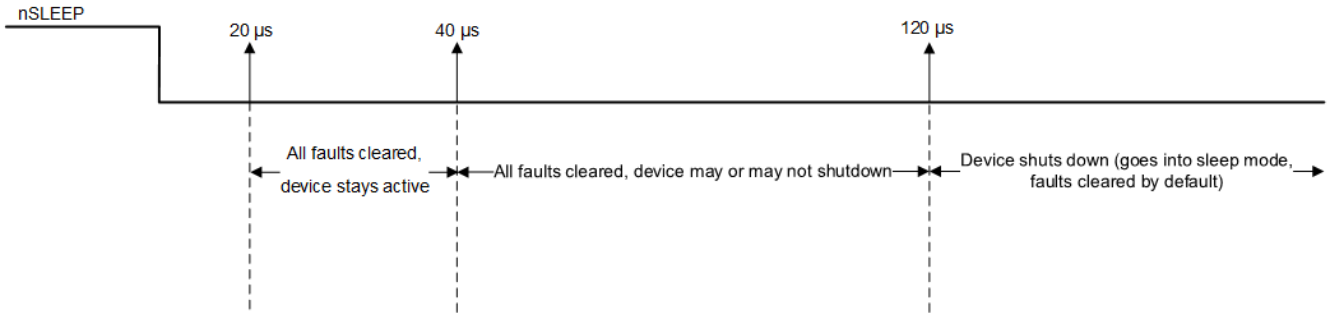


Figure 7-15. nSLEEP Reset Pulse

Functional Modes Summary

Table 7-8 lists a summary of the functional modes.

Table 7-8. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 1 or Hi-Z	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8434A is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8434A.

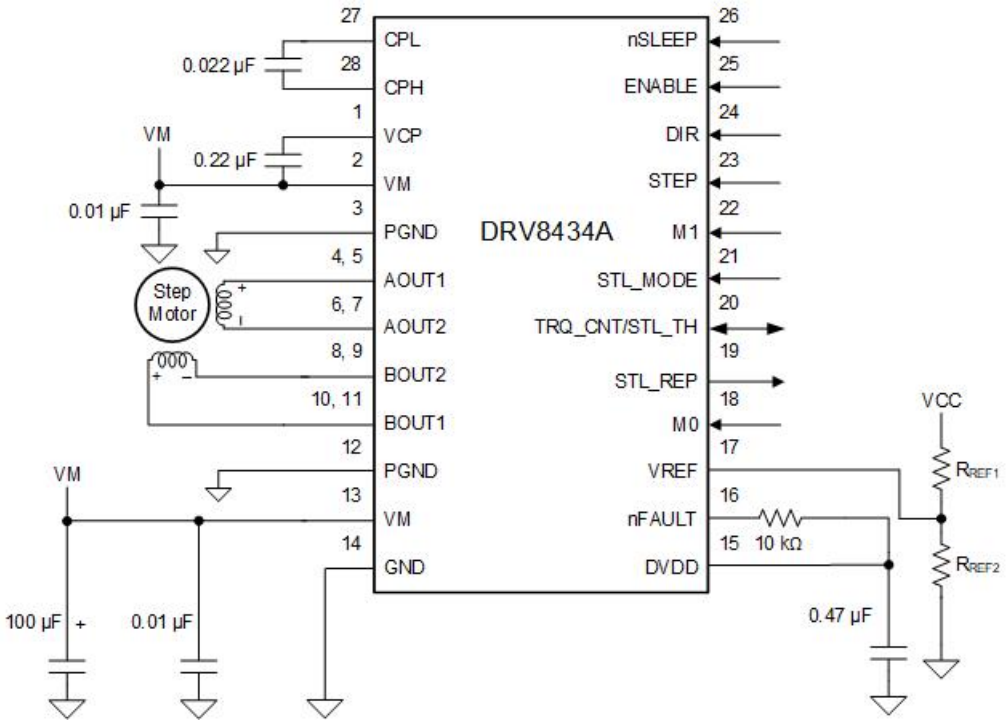


Figure 8-1. Typical Application Schematic (HTSSOP package)

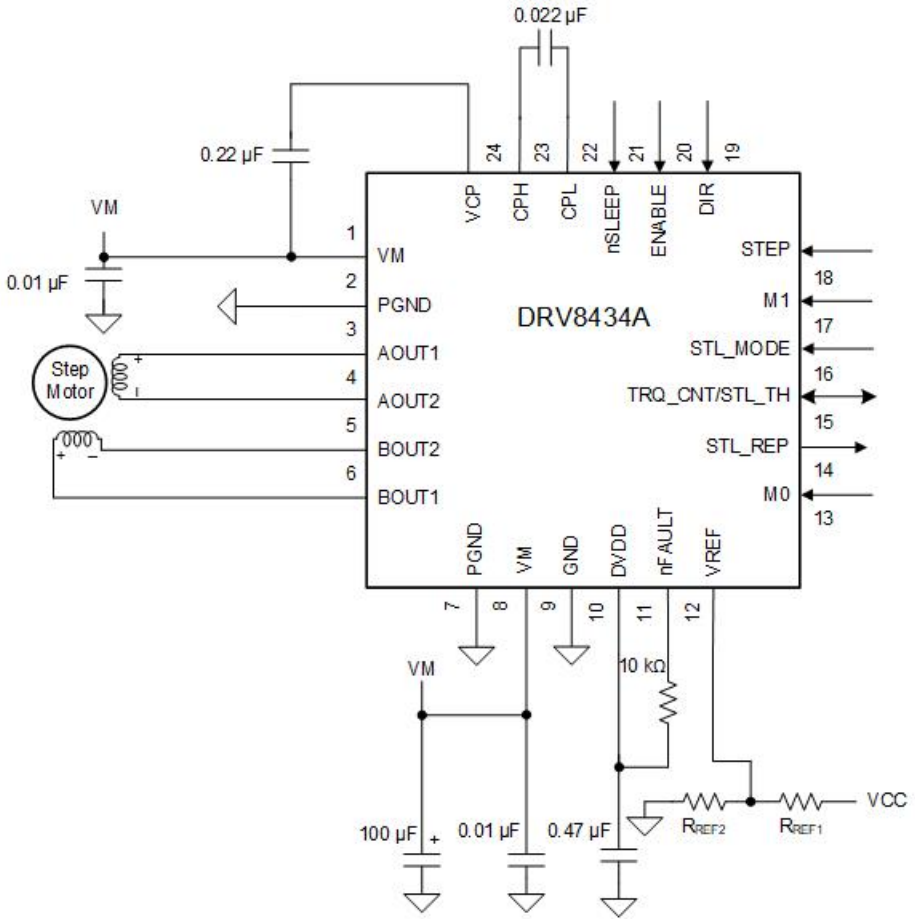


Figure 8-2. Typical Application Schematic (VQFN package)

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.9 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	18.75 rpm
Target full-scale current	I_{FS}	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8434A requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 1 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

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$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (°/rot)}{\theta_{step}\ (°/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \quad (1)$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 18.75 rpm at 1/8 microstep mode. Using Equation 1, f_{step} can be calculated as 500 Hz.

The microstepping level is set by the M0 and M1 pins and can be any of the settings listed in Table 8-2. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

Table 8-2. Microstepping Indexer Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330 kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage and the TRQ_DAC setting, as shown in Equation 2.

The maximum allowable voltage on the VREF pin is 3.3 V. DVDD can be used to provide VREF through aresistor divider.

During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V(V/A)} \times TRQ_DAC(\%) = \frac{V_{REF}(V) \times TRQ_DAC(\%)}{1.32(V/A)} \quad (2)$$

8.2.2.3 Decay Mode

The DRV8434A operates with smart tune ripple control decay mode. When a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8434A places the winding in slow decay.

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8.2.2.4 Application Curves

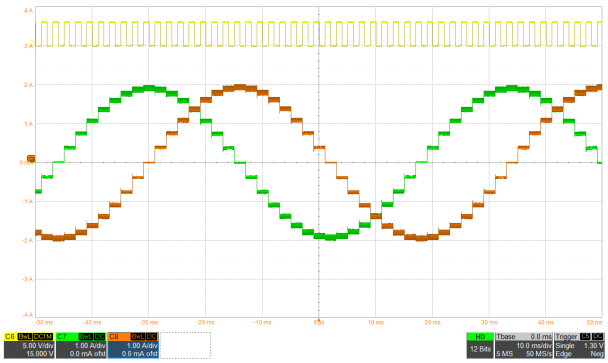


Figure 8-3. 1/8 Microstepping With smart tune Ripple Control Decay

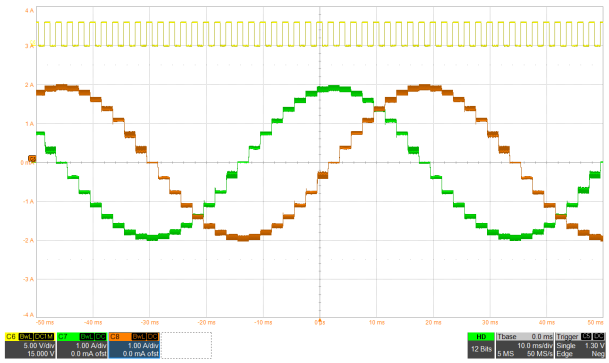


Figure 8-4. 1/8 Microstepping With smart tune Dynamic Decay

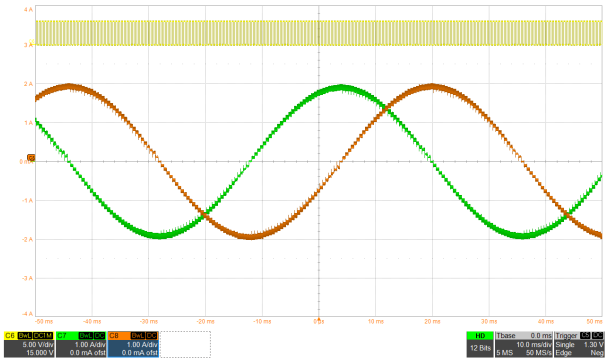


Figure 8-5. 1/32 Microstepping With smart tune Ripple Control Decay

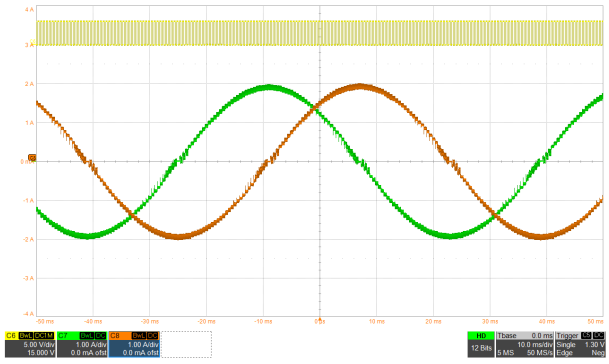


Figure 8-6. 1/32 Microstepping With smart tune Dynamic Decay

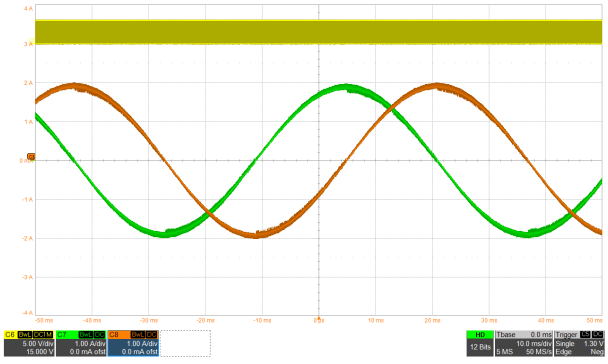


Figure 8-7. 1/256 Microstepping With smart tune Ripple Control Decay

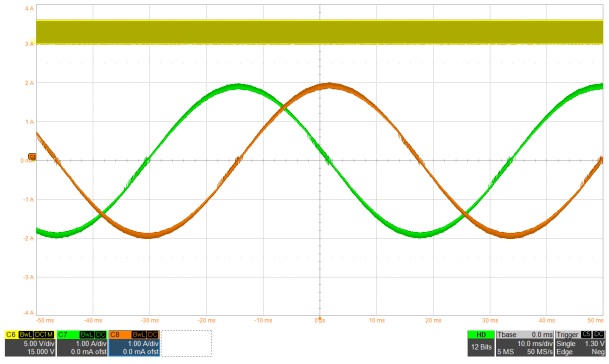


Figure 8-8. 1/256 Microstepping With smart tune Dynamic Decay

8.2.2.5 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.2.5.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

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8.2.2.5.2 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 3.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (3)$$

The conduction loss for the typical application shown in Typical Application is calculated in Equation 4.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (2\text{-A} / \sqrt{2})^2 \times (0.165\text{-}\Omega + 0.165\text{-}\Omega) = 1.32\text{-W} \quad (4)$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.2.5.3 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 5 and Equation 6.

$$P_{SW_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} \quad (5)$$

$$P_{SW_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} \quad (6)$$

Both t_{RISE_PWM} and t_{FALL_PWM} can be approximated as V_{VM} / t_{SR}. After substituting the values of various parameters, and assuming 30-kHz PWM frequency, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW_RISE} = 0.5 \times 24\text{-V} \times (2\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (7)$$

$$P_{SW_FALL} = 0.5 \times 24\text{-V} \times (1\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (8)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW_RISE} + P_{SW_FALL}) = 2 \times (0.05\text{-W} + 0.05\text{-W}) = 0.2\text{-W} \quad (9)$$

Note

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.2.5.4 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (10)$$

Substituting the values, quiescent power loss can be calculated as shown below -

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$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (11)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

8.2.2.5.5 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 12.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.32\text{-W} + 0.2\text{-W} + 0.12\text{-W} = 1.64\text{-W} \quad (12)$$

8.2.2.5.6 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 29.7 °C/W for the HTSSOP package and 39 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 29.7°C/W) = 73.71°C \quad (13)$$

The junction temperature for the VQFN package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 39°C/W) = 88.96\ °C \quad (14)$$

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

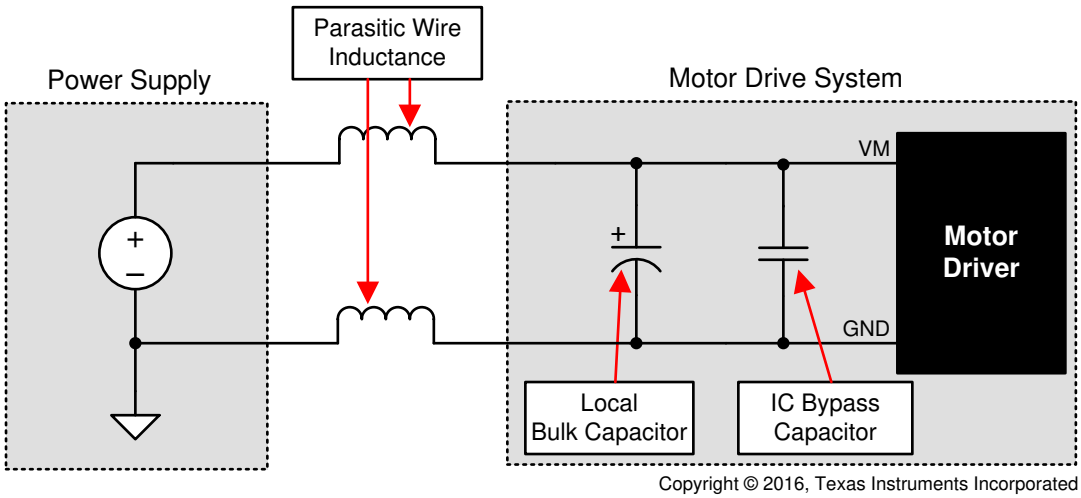


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible..

10.2 Layout Example

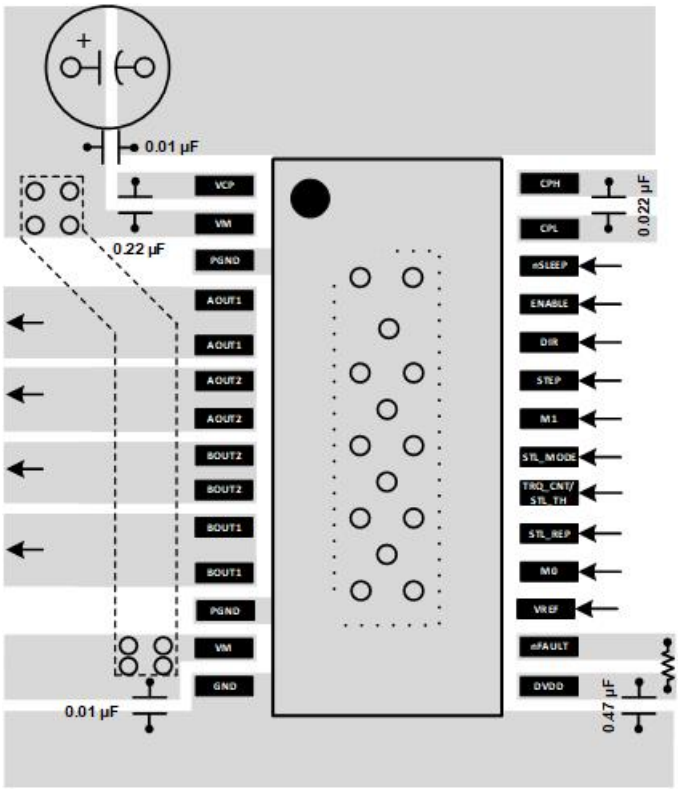


Figure 10-1. HTSSOP Layout Example

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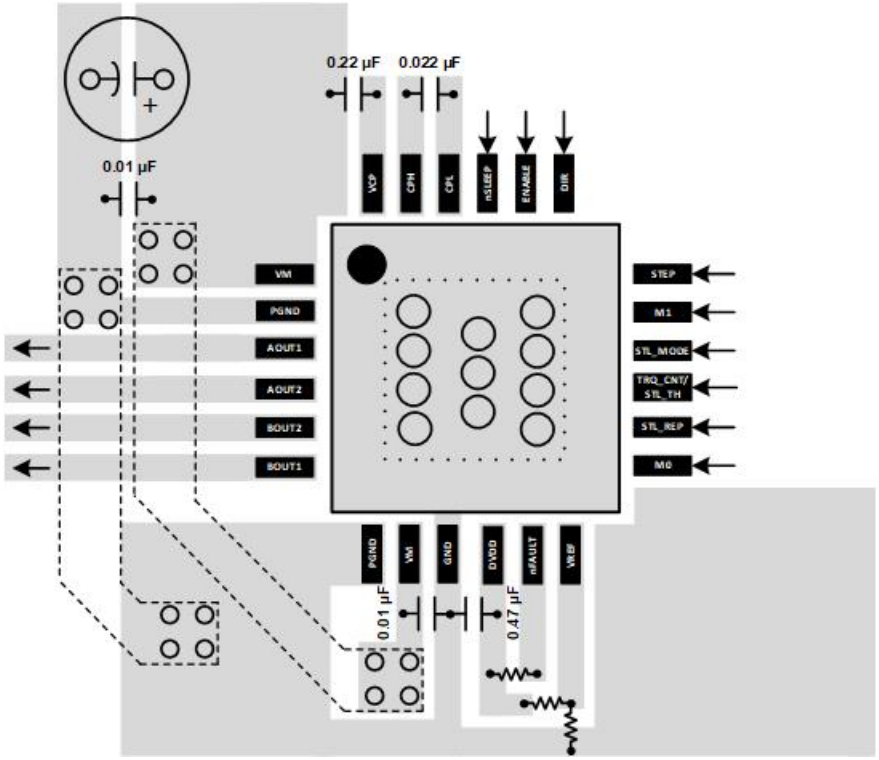


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

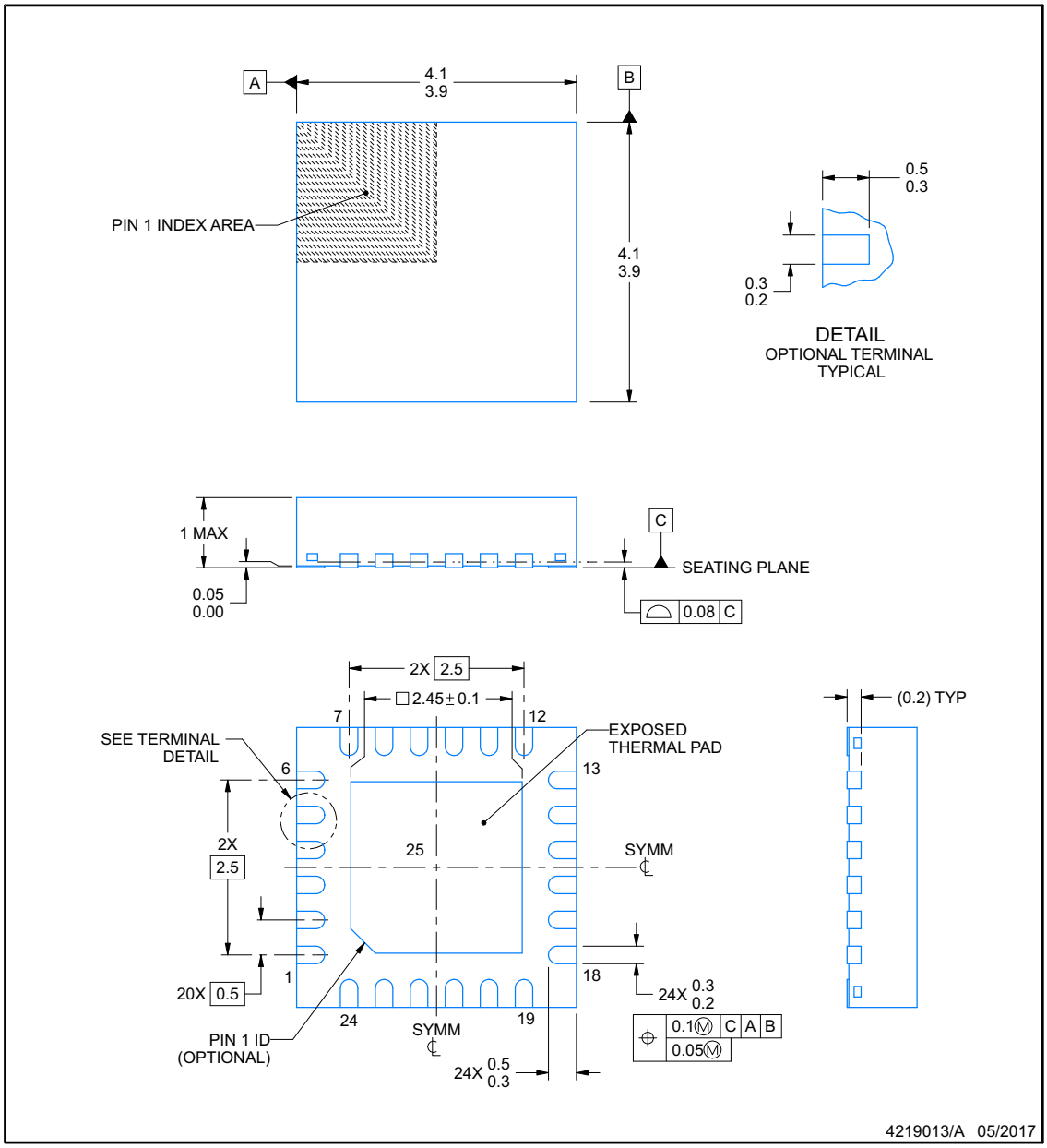
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PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

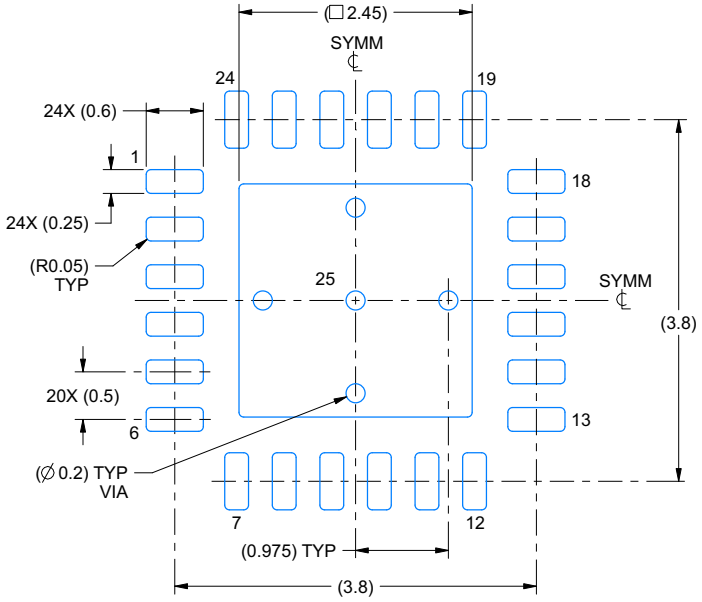
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EXAMPLE BOARD LAYOUT

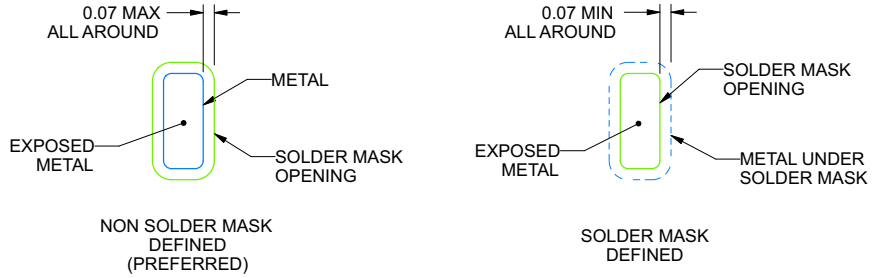
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

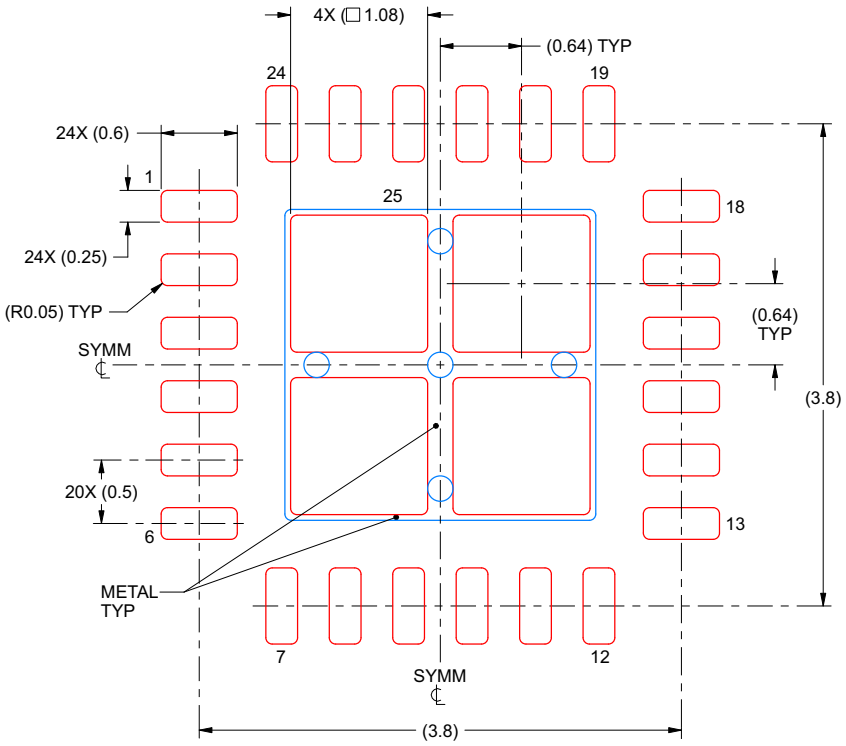
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RGE0024B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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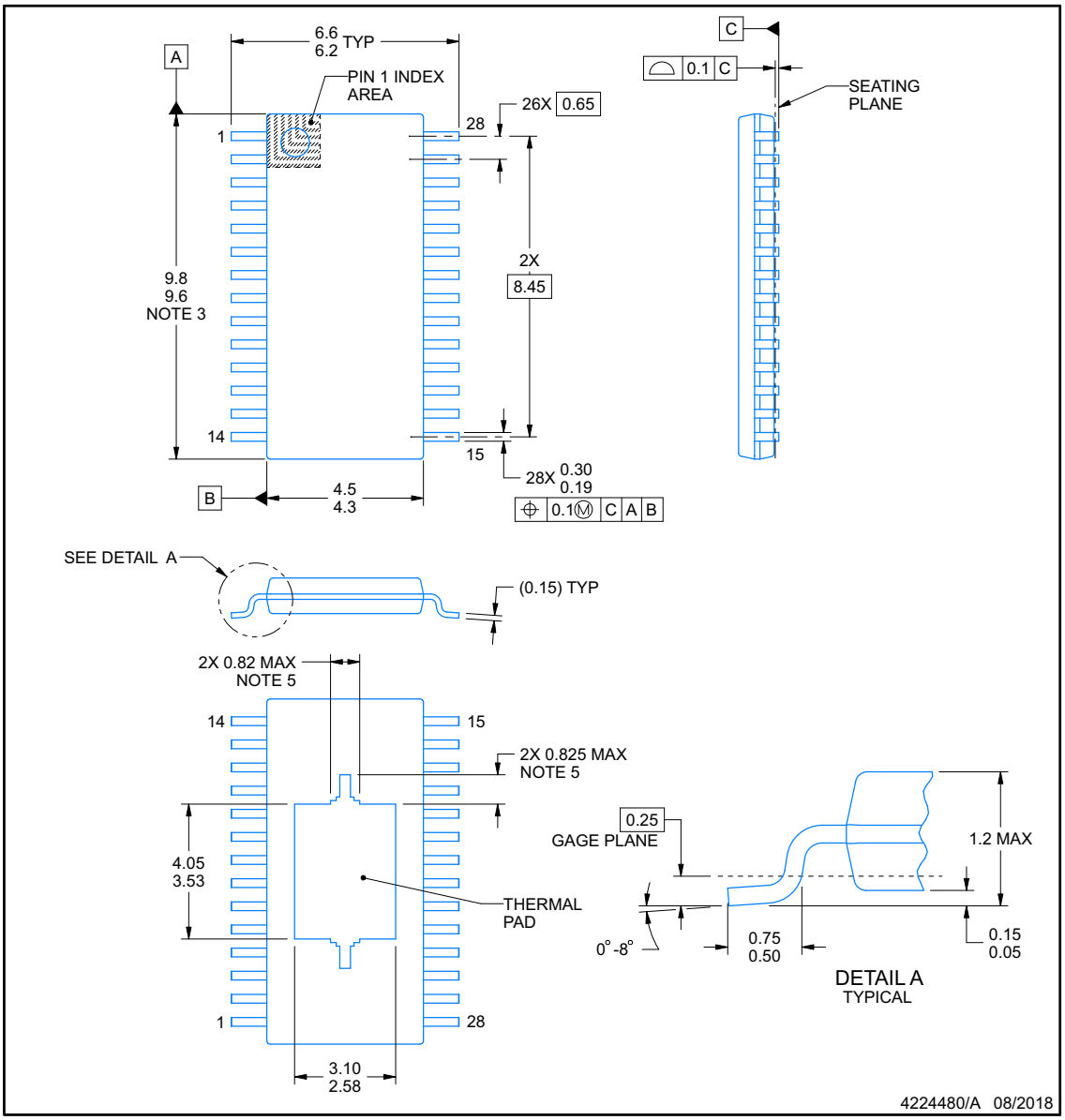
PACKAGE OUTLINE

PWP0028M



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

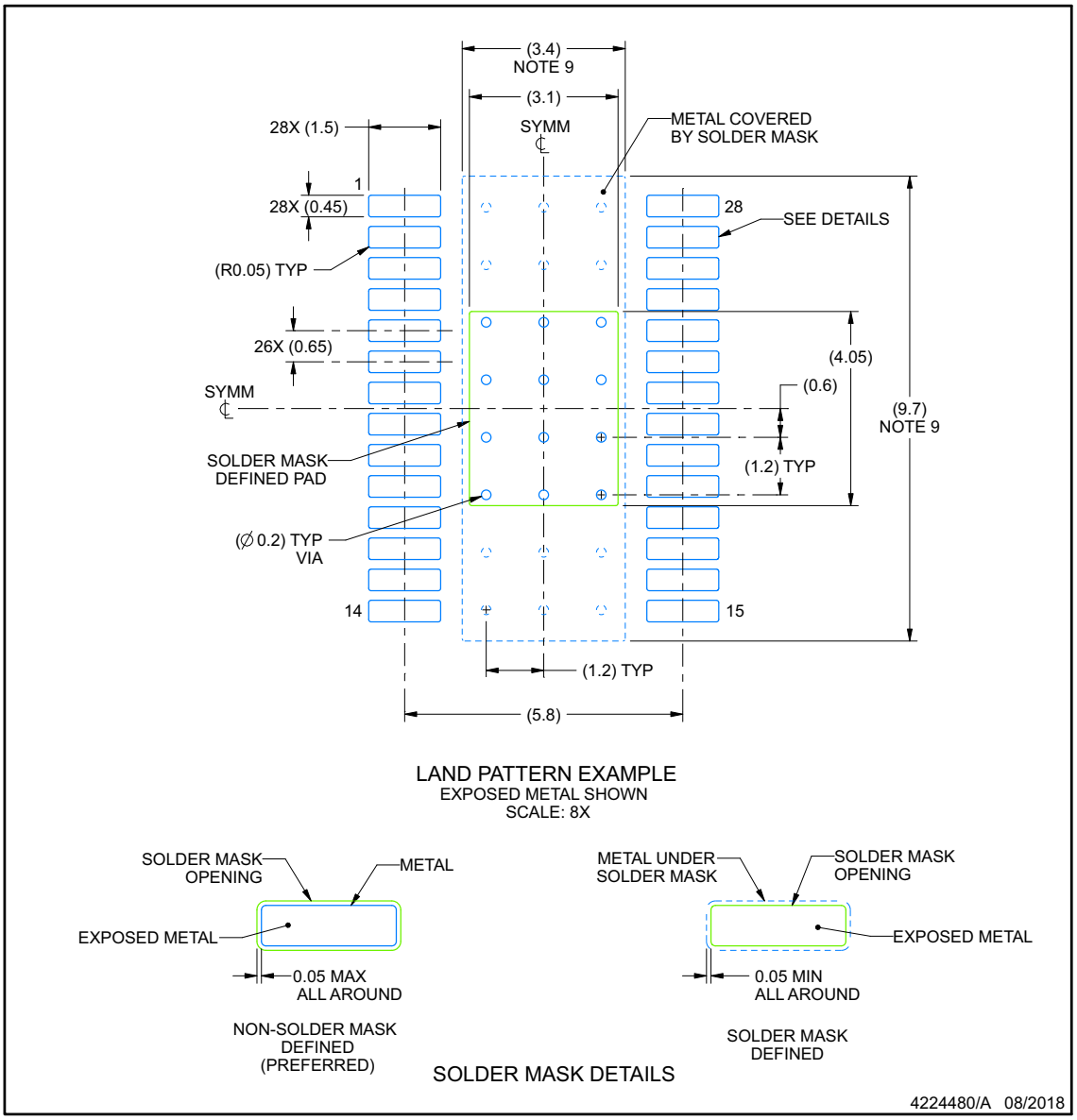
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EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

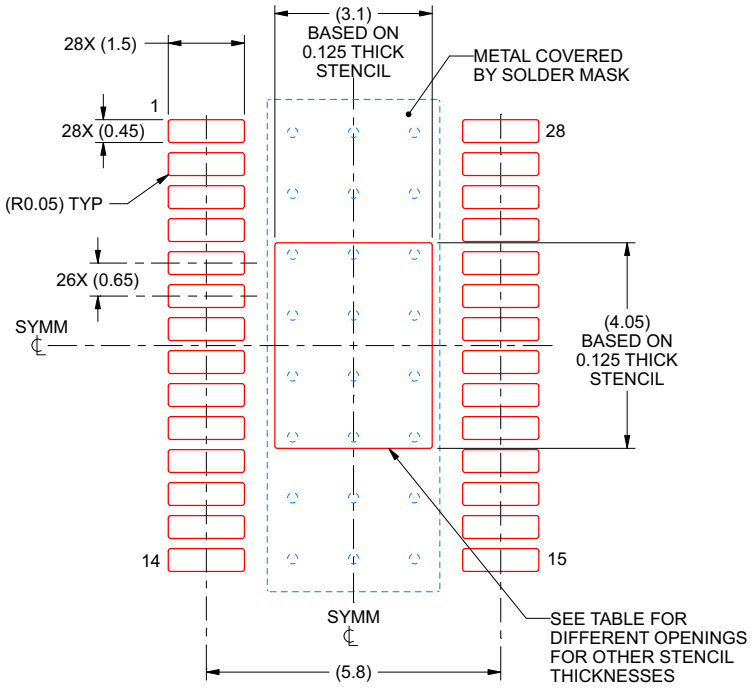
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EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8434ARGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8434A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

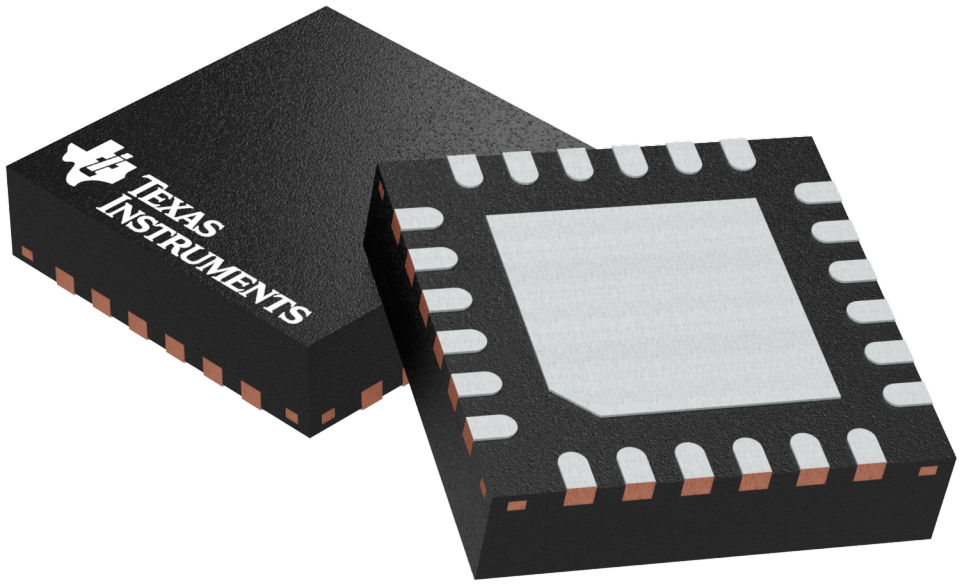
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GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

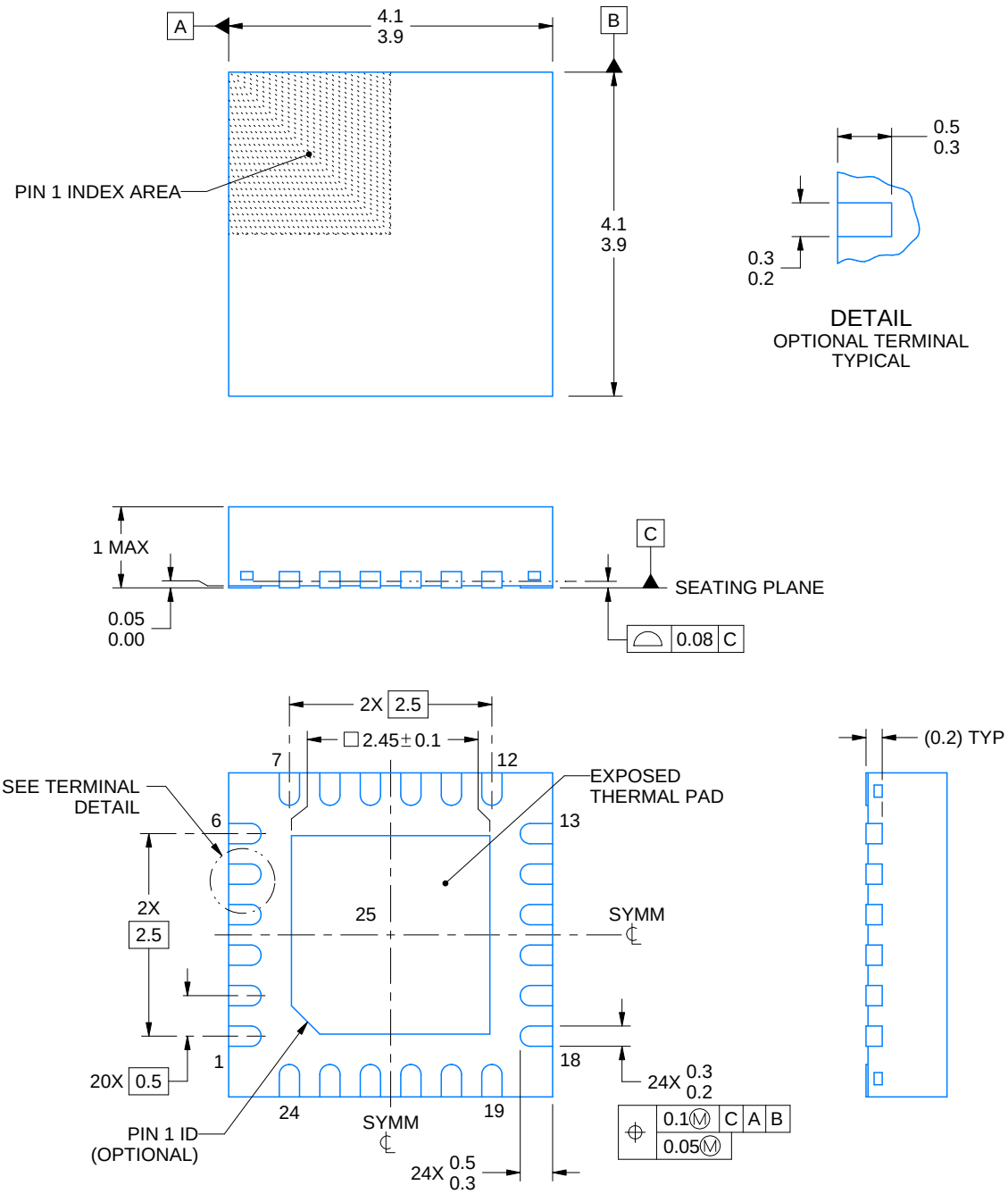
4204104/H

PACKAGE OUTLINE

RGE0024B

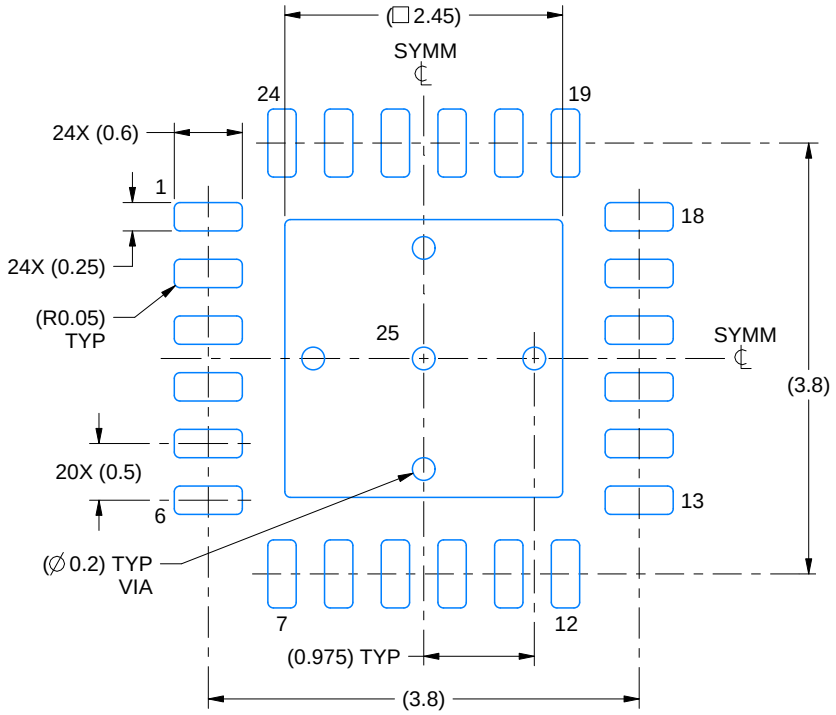
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

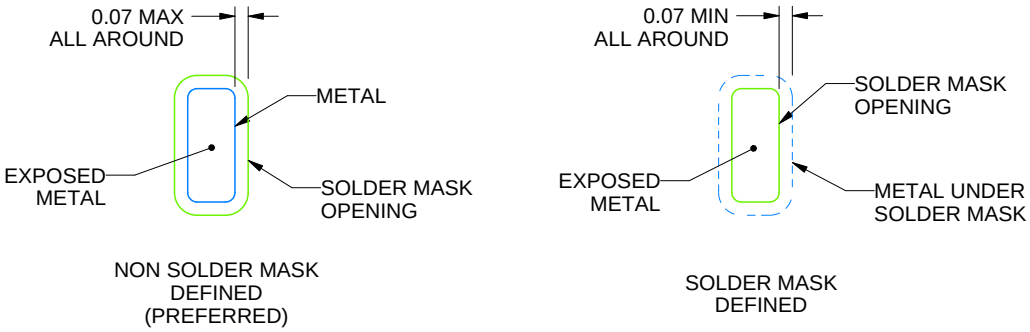


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

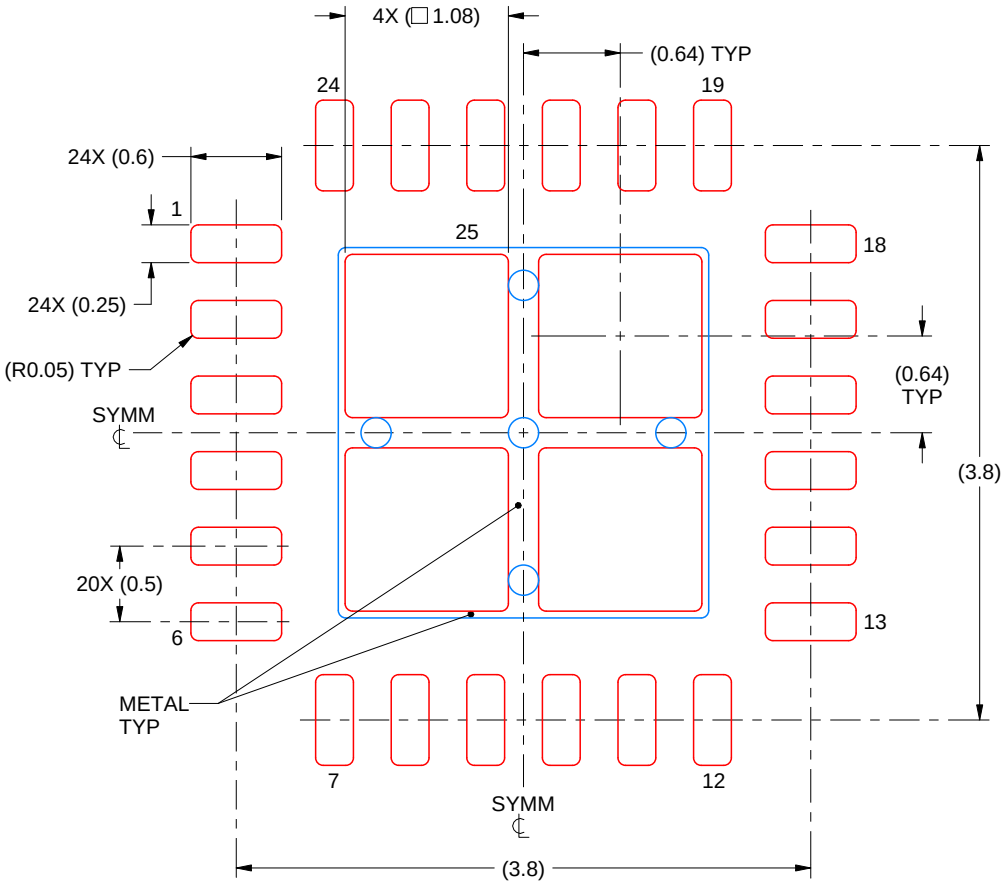


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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