ALT5020

High Efficiency
UMTS E800 (Band 20)
LTE Linear PAM

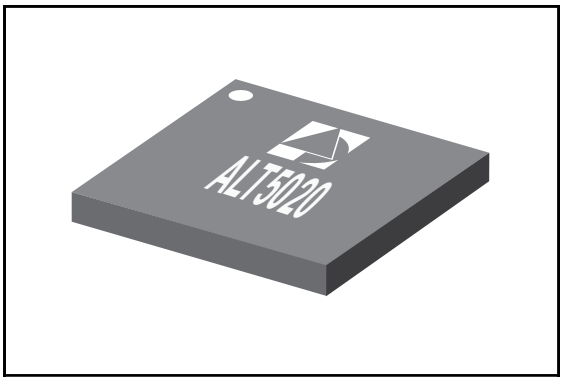
ADVANCED PRODUCT INFORMATION - Rev 0.0

FEATURES

- LTE Compliant
- High Efficiency (LTE waveform):
  - 42% @ P_{OUT} = +27.7 dBm
- Optimized for SMPS Supply
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated "daisy chainable" directional coupler with CPL_{IN} and CPL_{OUT} Ports
- Optimized for a 50 Ω System
- Internal DC blocks on IN/OUT RF ports
- 1.8 V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

APPLICATIONS

- Wireless Handsets and Data Devices for:
  - LTE (B20)



10 Pin 3 mm x 3 mm x 0.9 mm
Surface Mount Module

PRODUCT DESCRIPTION

The ALT5020 PA is designed to provide highly linear output for LTE handsets and data devices with high efficiency at high power mode. This ANADIGICS PA can be used with an external switch mode power supply (SMPS) to improve its efficiency and reduce current consumption further at high and low output powers. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. There are three selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, which increases handset talk and standby time. The self-contained 3 mm x 3 mm x 0.9 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

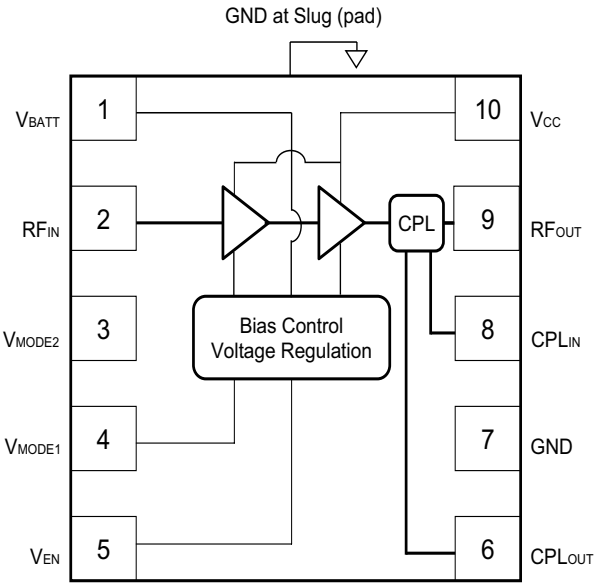


Figure 1: Block Diagram

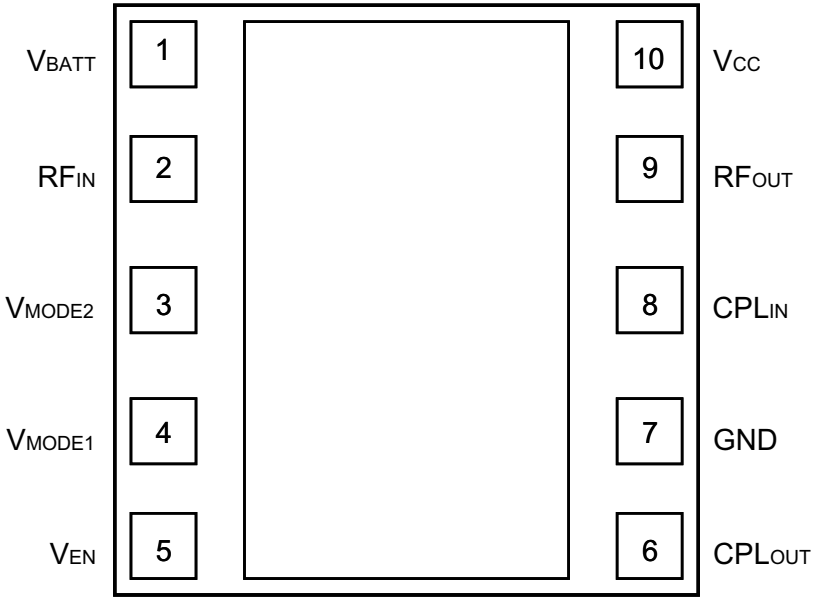


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	V_{MODE2}	Mode Control Voltage 2
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	CPL_{OUT}	Coupler Output
7	GND	Ground
8	CPL_{IN}	Coupler Input
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
RF Input (P_{IN})	-	0	10	dBm
V_{CC}	0	3.4	5	V
V_{BATT}	0	3.4	6	V
Control Voltage (V_{ENABLE}, V_{MODE})	0	1.8	3.5	V
Storage Temperature ($T_{STORAGE}$)	-40	25	150	°C

Functional operation to the specified performance is not implied under these conditions. Operation of any single parameter in excess of the absolute ratings may cause permanent damage. No damage occurs if one parameter is set at the limit while all other parameters are set within normal operating ranges.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	832	-	862	MHz	UMTS Band 20
Supply Voltage (V_{CC})	+0.6	+3.4	+4.4	V	$P_{OUT} \leq$ +27.7 dBm
Battery Voltage (V_{BATT})	+3.1	+3.4	+4.4	V	$P_{OUT} \leq$ +27.7 dBm
Enable Voltage (V_{ENABLE})	+1.35 0	+1.8 0	+3.1 +0.5	V	PA “on” PA “shut down”
Mode Control Voltage (V_{MODE1})	+1.35 0	+1.8 0	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT}) (1, 2, 3) LTE, HPM LTE, LPM	 26.9 -	 27.7 16	 - -	dBm	TS 36.101 Rel 8 for LTE
Case Temperature (T_C)	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:
(1) For operation at V_{CC} = +3.1 V, P_{OUT} is derated by 0.8 dB.
(2) For operation at 105 °C, P_{OUT} is derated by 1.0 dB.
(3) LTE waveform characteristics up to 20 MHz QPSK, 18 RB's.

Table 4: Electrical Specifications - LTE Operation (RB = 12, START = 0, QPSK)
(T_C = +25 °C, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS			
					P_{OUT}	V_{CC}	V_{MODE1}	V_{MODE2}
Gain	26.5 18 14	30 22 17	33 25 21	dB	+27.7 dBm +16 dBm +7 dBm	3.4 V 1.4 V 0.7 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR E-UTRA (1) at ± 10 MHz offset	- - -	-38 -38 -40	-34 -34 -34	dBc	+27.7 dBm +16 dBm +7 dBm	3.4 V 1.4 V 0.7 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 UTRA (1) at ± 7.5 MHz offset	- - -	-39 -39 -40	-36 -36 -36	dBc	+27.7 dBm +16 dBm +7 dBm	3.4 V 1.4 V 0.7 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 UTRA (1) at ± 12.5 MHz offset	- - -	<-60 <-60 <-60	-40 -40 -40	dBc	+27.7 dBm +16 dBm +7 dBm	3.4 V 1.4 V 0.7 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Efficiency (1)	33 - -	38 22 13	- - -	%	+27.7 dBm +16 dBm +7 dBm	3.4 V 1.4 V 0.7 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (Icq) Low Bias Mode	-	25	-	mA	through V_{CC} pin, $V_{MODE1,2}$ = +1.8 V			
Mode Control Current	-	0.05	0.1	mA	through V_{MODE} pin, V_{MODE1} = 1.8 V			
Enable Current	-	0.05	0.1	mA	through V_{ENABLE} pin			
BATT Current	-	3	5.5	mA	through V_{BATT} pin, V_{MODE1} = +1.8 V			
Leakage Current	-	<5	10	µA	V_{BATT} = +4.4 V, V_{CC} = +4.4 V V_{ENABLE} = 0 V, V_{MODE1} = 0 V			
Noise in Receive Band (2)	-	TBD	-	dBm/Hz	791 - 821 MHz			
Harmonics 2f_O 3f_O, 4f_O	- -	TBD TBD	- -	dBc	P_{OUT} ≤ +27.7 dBm			
Input Impedance	-	-	2:1	VSWR				
Coupling Factor	-	20	-	dB				
Directivity	-	20	-	dB				
Coupler IN-OUT Daisy Chain Insertion Loss	-	<0.25	-	dB	698 to 2620 MHz Pin 8 to 6 Shutdown Mode			
Spurious Output Level (all suprious outputs)	-	-	<-65	dBc	P_{OUT} ≤ +27.7 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions			
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range			

Notes:
(1) ACLR and Efficiency measured at 847 MHz.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode
The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE} voltages.

Bias Modes
The power amplifier may be placed in either a Low, Medium or High Bias mode by applying the appropriate logic level (see Operating Ranges table) to $V_{MODE1,2}$. The Bias Control table lists the recommended modes of operation for various applications.

Three operating modes are available to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels $\geq$ 15 dBm. At around 16 dBm output power, the PA should be “Mode Switched” to Medium power mode for lowest quiescent current consumption. The PA should be switched to Low Bias/ Low Power mode at ~<7 dbm.

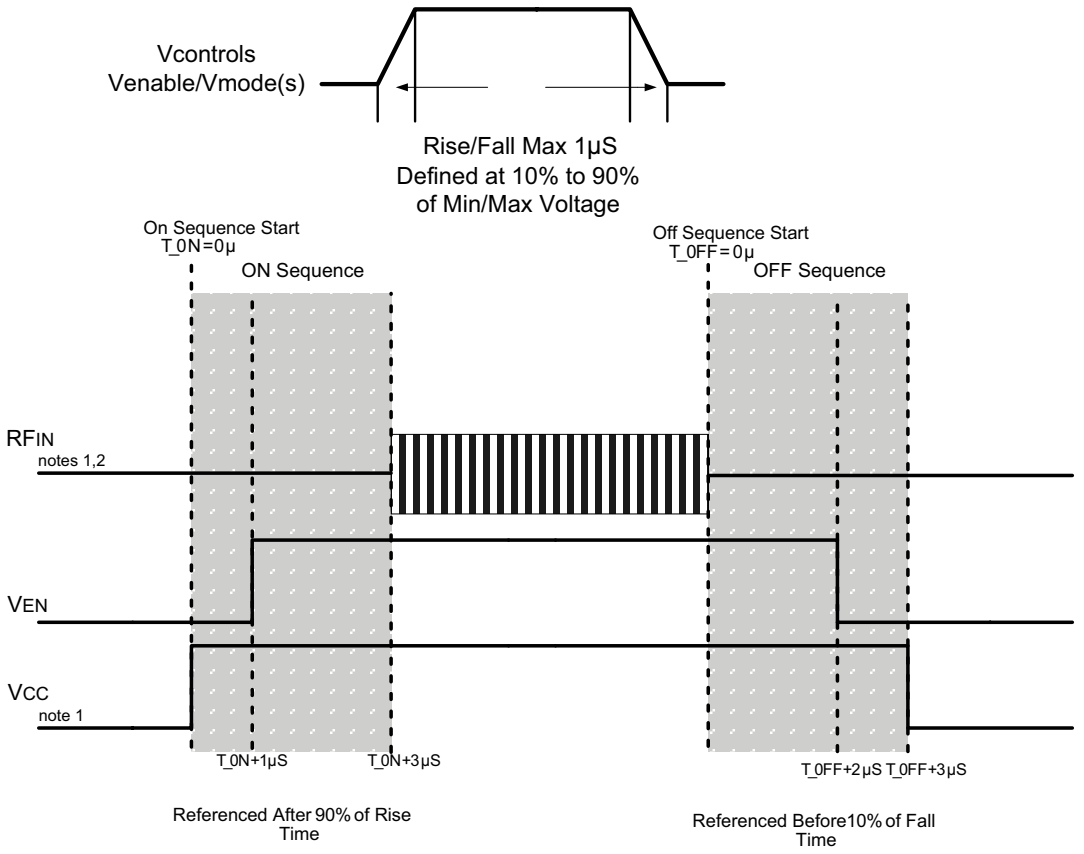


Figure 3: Recommended ON/OFF Timing Sequence

Notes:
(1) Level might be changed after RF is ON.
(2) RF OFF defined as $P_{IN} \leq$ -30 dBm.
(3) Switching simultaneously between V_{MODE} and V_{EN} is not recommended.

Table 5: Bias Control

APPLICATION	POUT LEVELS	BIAS MODE	VENABLE	VMODE1	VMODE2	VCC	VBATT
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V
Med power (Med Bias Mode)	≤ +17 dBm	Medium	+1.8 V	+1.8 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V
Low power (Low Bias Mode)	≤ +8 dBm	Low	+1.8 V	+1.8 V	+1.8 V	0.6 - 4.4 V	3.1 - 4.4 V
Shutdown	-	Shutdown	0 V	0 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V

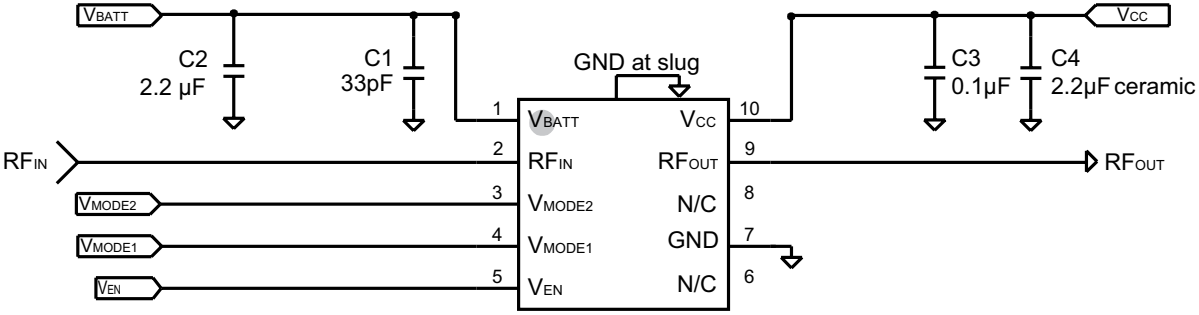
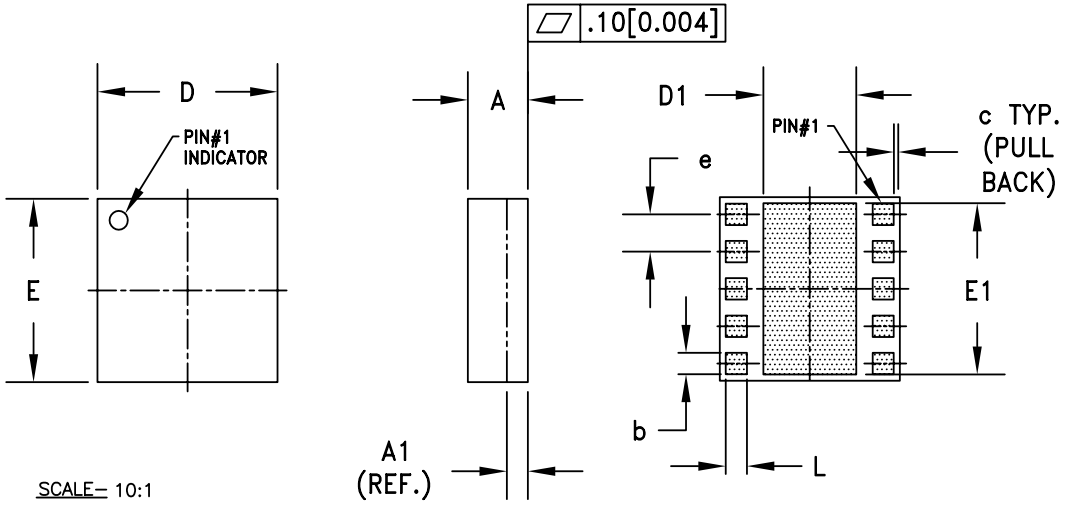


Figure 4: Evaluation Board Schematic

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.88	0.94	1.00	0.035	0.037	0.039	–
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						–
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	–
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e		0.60			0.024		3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS IN MILLIMETERS.
2. UNLESS SPECIFIED, TOLERANCE=±0.076[0.003].
3. SIGNAL PADS SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO THE PRODUCT DESIGN.
4. GROUND PADS SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL SIZE AND LOCATION ARE REFERENCE ONLY.
5. PITCH MEASUREMENTS (e) TAKE CENTERLINE TO CENTERLINE OF SOLDERMASK OPENINGS.
6. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
7. LAMINATE CONTROL DRAWING SPECIFIED BY

Figure 5: Package Outline - 10 Pin 3 mm x 3 mm x 0.94 mm Surface Mount Module

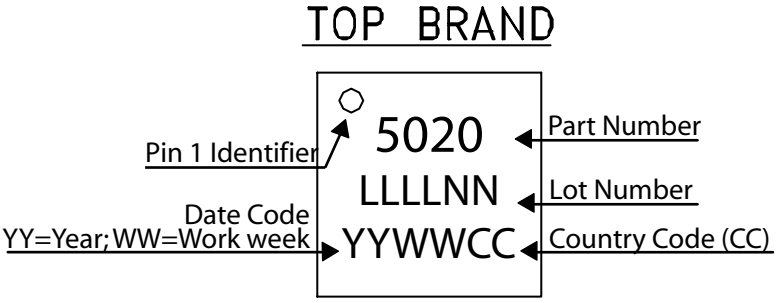
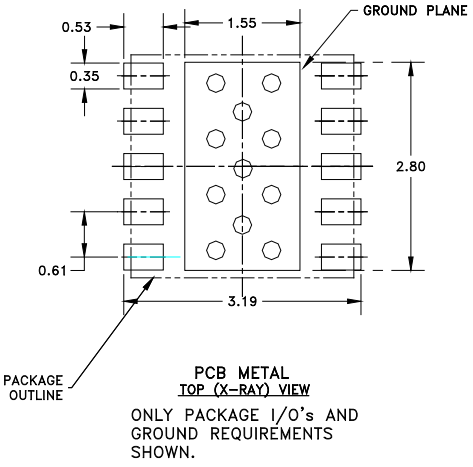


Figure 6: Branding Specification

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

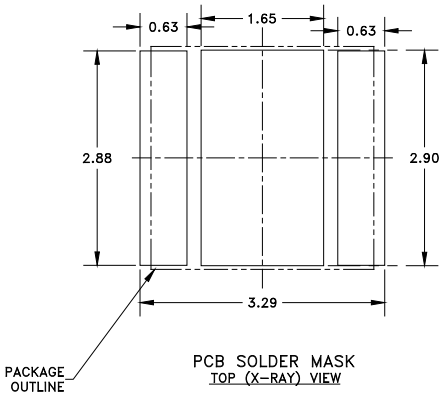
(1) OUTLINE DRAWING REFERENCE: P8002478_E

(2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

(3) DIMENSIONS IN MILLIMETERS.

(4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.

(5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)



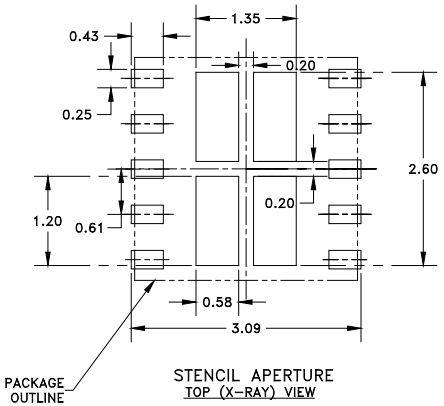
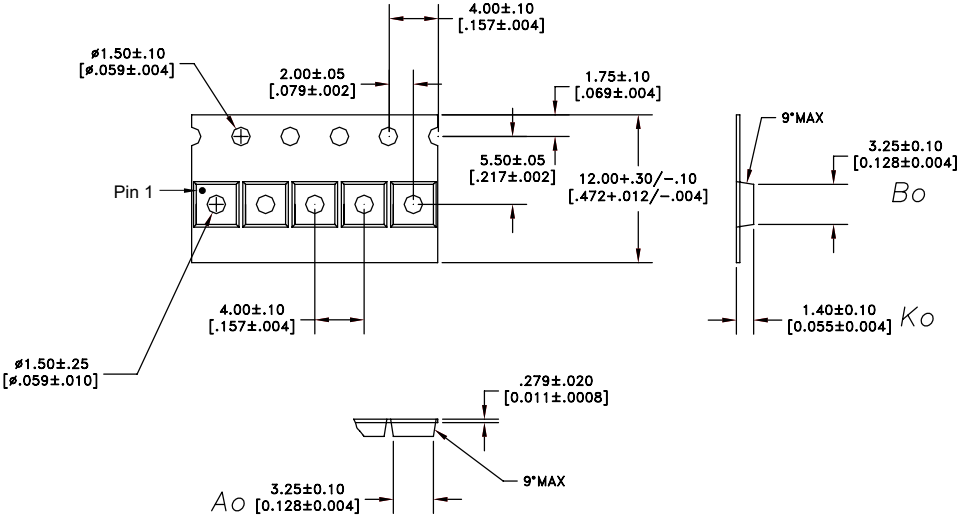


Figure 7: Recommended PCB Layout Information

COMPONENT PACKAGING



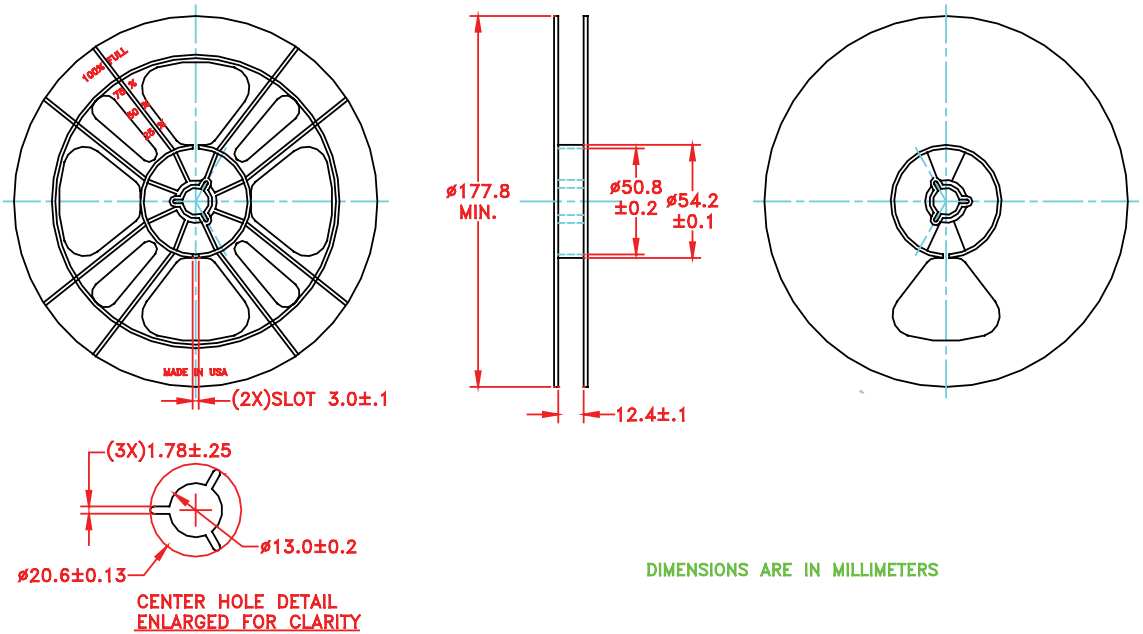
NOTES:

1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 8: Carrier Tape



DIMENSIONS ARE IN MILLIMETERS

NOTES:

1. MATERIAL: BLACK CARBON POLYSTYRENE
SURFACE RESISTIVITY: $1X10^4$ TO $1X10^8$ ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 9: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ALT5020Q7	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.94 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
ALT5020P9	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.94 mm Surface Mount Module	Partial Tape and Reel

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