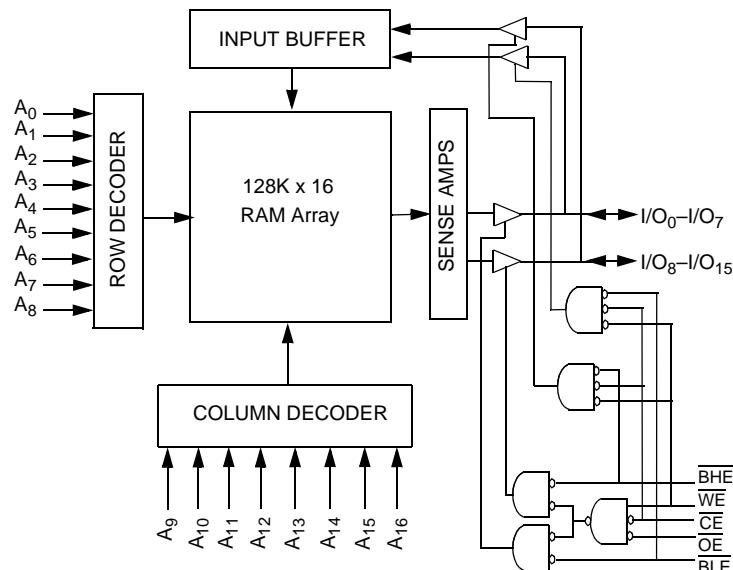


## Features

- Temperature ranges
  - Industrial: -40 °C to 85 °C
  - Automotive-A: -40 °C to 85 °C
  - Automotive-E: -40 °C to 125 °C
- Pin and function compatible with CY7C1011BV33
- High speed
  - $t_{AA} = 10$  ns (Industrial and Automotive-A)
  - $t_{AA} = 12$  ns (Automotive-E)
- Low active power
  - 360 mW (max) (Industrial and Automotive-A)
- 2.0 V data retention
- Automatic power down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) features
- Available in Pb-free 44-pin thin small outline package (TSOP) II, 44-pin thin quad flat package (TQFP), and non Pb-free 48-ball very fine ball grid array (VFBGA) packages

## Logic Block Diagram



## Functional Description

The CY7C1011CV33 is a high performance complementary metal oxide semiconductor (CMOS) static RAM organized as 131,072 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

To write to the device, take  $\overline{CE}$  and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take  $\overline{CE}$  and  $\overline{OE}$  LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If BLE is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. For more information, see the "Truth Table" on page 10 for a complete description of Read and Write modes.

The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $CE$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $CE$  LOW and  $WE$  LOW).

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

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## Pin Configuration

Figure 1. 44-Pin TSOP II<sup>[1]</sup>

|                  |    |    |                   |
|------------------|----|----|-------------------|
| A <sub>4</sub>   | 1  | 44 | A <sub>5</sub>    |
| A <sub>3</sub>   | 2  | 43 | A <sub>6</sub>    |
| A <sub>2</sub>   | 3  | 42 | A <sub>7</sub>    |
| A <sub>1</sub>   | 4  | 41 | OE                |
| A <sub>0</sub>   | 5  | 40 | BHE               |
| CE               | 6  | 39 | BLE               |
| I/O <sub>0</sub> | 7  | 38 | I/O <sub>15</sub> |
| I/O <sub>1</sub> | 8  | 37 | I/O <sub>14</sub> |
| I/O <sub>2</sub> | 9  | 36 | I/O <sub>13</sub> |
| I/O <sub>3</sub> | 10 | 35 | I/O <sub>12</sub> |
| V <sub>CC</sub>  | 11 | 34 | V <sub>SS</sub>   |
| V <sub>SS</sub>  | 12 | 33 | V <sub>CC</sub>   |
| I/O <sub>4</sub> | 13 | 32 | I/O <sub>11</sub> |
| I/O <sub>5</sub> | 14 | 31 | I/O <sub>10</sub> |
| I/O <sub>6</sub> | 15 | 30 | I/O <sub>9</sub>  |
| I/O <sub>7</sub> | 16 | 29 | I/O <sub>8</sub>  |
| WE               | 17 | 28 | NC                |
| A <sub>16</sub>  | 18 | 27 | A <sub>8</sub>    |
| A <sub>15</sub>  | 19 | 26 | A <sub>9</sub>    |
| A <sub>14</sub>  | 20 | 25 | A <sub>10</sub>   |
| A <sub>13</sub>  | 21 | 24 | A <sub>11</sub>   |
| A <sub>12</sub>  | 22 | 23 | NC                |

Figure 2. 48-Ball VFBGA Pinout<sup>[1]</sup>

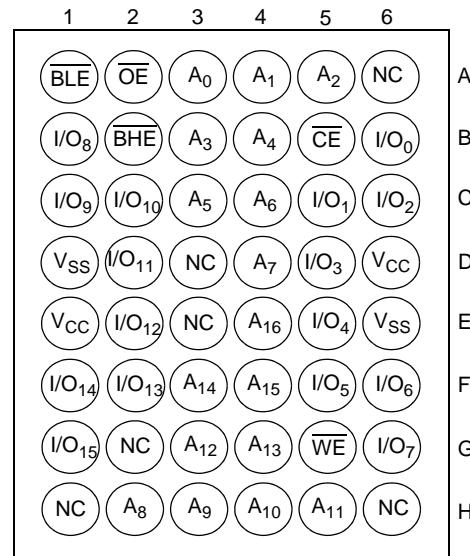
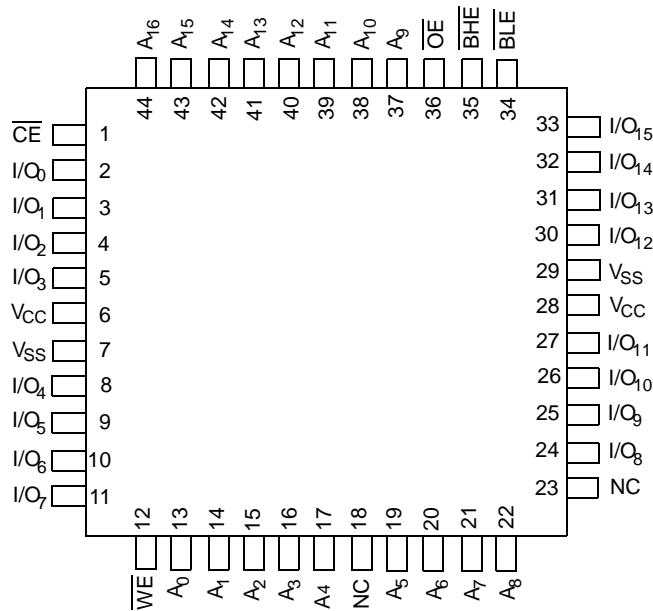


Figure 3. 44-Pin TQFP



### Note

1. NC pins are not connected on the die.

**Selection Guide**

| <b>Description</b>           |              | <b>-10</b> | <b>-12</b> | <b>Unit</b> |
|------------------------------|--------------|------------|------------|-------------|
| Maximum access time          |              | 10         | 12         | ns          |
| Maximum operating current    | Industrial   | 100        | 95         | mA          |
|                              | Automotive-A | 100        |            | mA          |
|                              | Automotive-E |            | 120        | mA          |
| Maximum CMOS standby current | Industrial   | 10         | 10         | mA          |
|                              | Automotive-A | 10         |            | mA          |
|                              | Automotive-E |            | 15         | mA          |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient temperature with

power applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply voltage on  $V_{CC}$  relative to GND<sup>[2]</sup> .....  $-0.5\text{ V}$  to  $+4.6\text{ V}$

DC voltage applied to outputs  
in High Z state<sup>[2]</sup> .....  $-0.5\text{ V}$  to  $V_{CC}+0.5\text{ V}$

DC input voltage<sup>[2]</sup> .....  $-0.5\text{ V}$  to  $V_{CC}+0.5\text{ V}$

Current into outputs (LOW) .....  $20\text{ mA}$

Static discharge voltage .....  $>2001\text{ V}$   
(MIL-STD-883, method 3015)

Latch up current .....  $>200\text{ mA}$

## Operating Range

| Range         | Ambient Temperature ( $T_A$ )                   | $V_{CC}$                |
|---------------|---|-------------------------|
| Industrial    | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  | $3.3\text{ V} \pm 10\%$ |
| Automotive-A  | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |                         |
| Automotive -E | $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |                         |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description                                      | Test Conditions   | -10           |                | -12  |                | Unit |               |
|-----------|--|---|---------------|----------------|------|----------------|------|---------------|
|           |  |   | Min           | Max            | Min  | Max            |      |               |
| $V_{OH}$  | Output HIGH voltage                              | $V_{CC} = \text{Min}$ , $I_{OH} = -4.0\text{ mA}$   | 2.4           |                | 2.4  |                | V    |               |
| $V_{OL}$  | Output LOW voltage                               | $V_{CC} = \text{Min}$ , $I_{OL} = 8.0\text{ mA}$  |               | 0.4            |      | 0.4            | V    |               |
| $V_{IH}$  | Input HIGH voltage                               |   | 2.0           | $V_{CC} + 0.3$ | 2.0  | $V_{CC} + 0.3$ | V    |               |
| $V_{IL}$  | Input LOW voltage <sup>[2]</sup>                 |   | -0.3          | 0.8            | -0.3 | 0.8            | V    |               |
| $I_{IX}$  | Input leakage current                            | $\text{GND} \leq V_I \leq V_{CC}$   | Industrial    | -1             | +1   | -1             | +1   | $\mu\text{A}$ |
|           |  |   | Automotive-A  | -1             | +1   |                |      |               |
|           |  |   | Automotive -E |                |      | -20            | +20  |               |
| $I_{OZ}$  | Output leakage current                           | $\text{GND} \leq V_I \leq V_{CC}$ ,<br>Output disabled  | Industrial    | -1             | +1   | -1             | +1   | $\mu\text{A}$ |
|           |  |   | Automotive-A  | -1             | +1   |                |      |               |
|           |  |   | Automotive -E |                |      | -20            | +20  |               |
| $I_{CC}$  | $V_{CC}$ operating supply current                | $V_{CC} = \text{Max}$ , $I_{OUT} = 0\text{ mA}$ ,<br>$f = f_{MAX} = 1/t_{RC}$   | Industrial    |                | 100  |                | 95   | mA            |
|           |  |   | Automotive-A  |                | 100  |                |      |               |
|           |  |   | Automotive -E |                |      |                | 120  |               |
| $I_{SB1}$ | Automatic CE power down<br>current — TTL Inputs  | $\text{Max } V_{CC}, CE \geq V_{IH}$<br>$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$                                      | Industrial    |                | 40   |                | 40   | mA            |
|           |  |   | Automotive-A  |                | 40   |                |      |               |
|           |  |   | Automotive -E |                |      |                | 45   |               |
| $I_{SB2}$ | Automatic CE power down<br>current — CMOS inputs | $\text{Max } V_{CC}, CE \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$ , or<br>$V_{IN} \leq 0.3\text{ V}$ , $f = 0$ | Industrial    |                | 10   |                | 10   | mA            |
|           |  |   | Automotive-A  |                | 10   |                |      |               |
|           |  |   | Automotive -E |                |      |                | 15   |               |

### Note

2.  $V_{IL}(\text{min}) = -2.0\text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

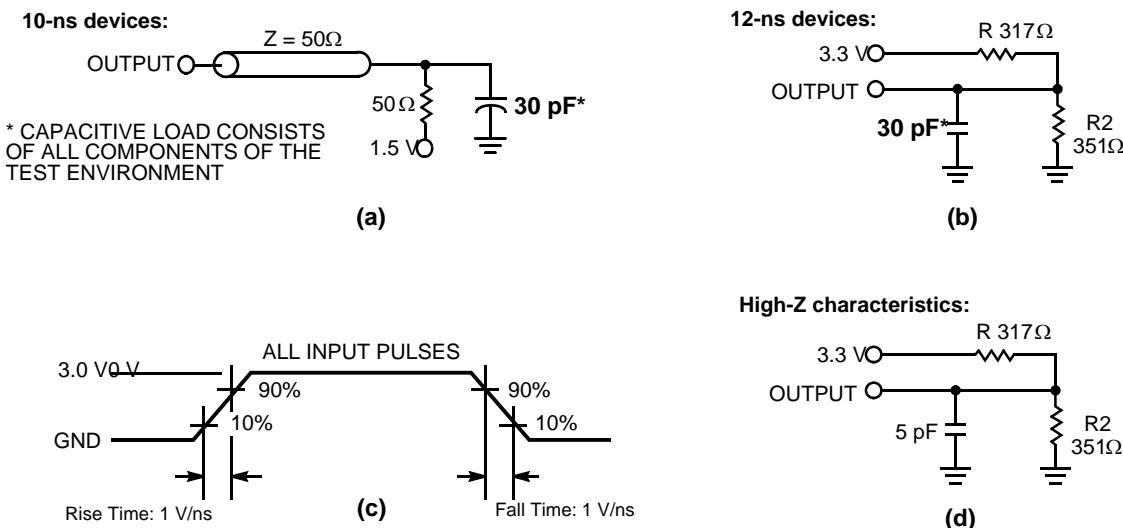
| Parameter | Description        | Test Conditions   | Max | Unit |
|-----------|--------------------|---|-----|------|
| $C_{IN}$  | Input capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3 \text{ V}$ | 8   | pF   |
| $C_{OUT}$ | Output capacitance |   | 8   | pF   |

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter     | Description                              | Test Conditions  | TSOP II | TQFP  | VFBGA | Unit                      |
|---------------|--|--|---------|-------|-------|---------------------------|
| $\Theta_{JA}$ | Thermal resistance (Junction to ambient) | Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board | 44.56   | 42.66 | 46.98 | $^\circ\text{C}/\text{W}$ |
| $\Theta_{JC}$ | Thermal resistance (Junction to case)    |  | 10.75   | 14.64 | 9.63  | $^\circ\text{C}/\text{W}$ |

Figure 4. AC Test Loads and Waveforms [3]



### Note

3. AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure 4 (a). All other speeds are tested using the Thevenin load shown in Figure 4 (b). High-Z characteristics are tested for all speeds using the test load shown in Figure 4 (d).

## Switching Characteristics

Over the Operating Range [4]

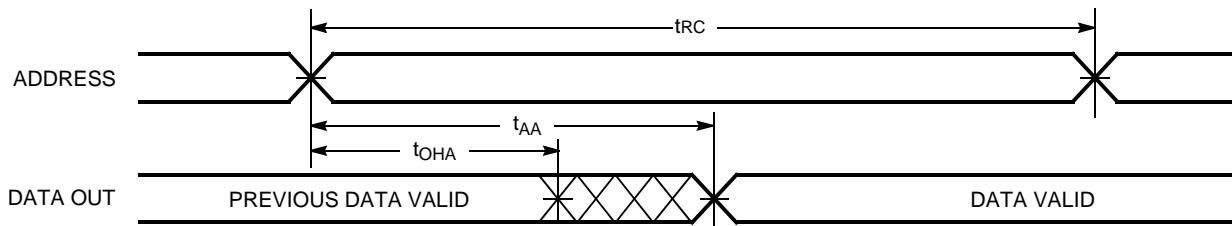
| Parameter                            | Description   | -10                     |     | -12 |     | Unit          |
|--------------------------------------|---|-------------------------|-----|-----|-----|---------------|
|                                      |   | Min                     | Max | Min | Max |               |
| <b>Read Cycle</b>                    |   |                         |     |     |     |               |
| $t_{\text{power}}^{[5]}$             | $V_{\text{CC}}$ (typical) to the first access           | 1                       |     | 1   |     | $\mu\text{s}$ |
| $t_{\text{RC}}$                      | Read cycle time   | 10                      |     | 12  |     | ns            |
| $t_{\text{AA}}$                      | Address to data valid                                   |                         | 10  |     | 12  | ns            |
| $t_{\text{OHA}}$                     | Data hold from address change                           | 3                       |     | 3   |     | ns            |
| $t_{\text{ACE}}$                     | $\overline{\text{CE}}$ LOW to data valid                |                         | 10  |     | 12  | ns            |
| $t_{\text{DOE}}$                     | $\overline{\text{OE}}$ LOW to data valid                | Industrial/Automotive-A |     | 5   | 6   | ns            |
|                                      |   | Automotive-E            |     |     | 8   |               |
| $t_{\text{LZOE}}$                    | $\overline{\text{OE}}$ LOW to Low Z <sup>[6]</sup>      | 0                       |     | 0   |     | ns            |
| $t_{\text{HZOE}}$                    | $\overline{\text{OE}}$ HIGH to High Z <sup>[6, 7]</sup> |                         | 5   |     | 6   | ns            |
| $t_{\text{LZCE}}$                    | $\overline{\text{CE}}$ LOW to Low Z <sup>[6]</sup>      | 3                       |     | 3   |     | ns            |
| $t_{\text{HZCE}}$                    | $\overline{\text{CE}}$ HIGH to High Z <sup>[6, 7]</sup> |                         | 5   |     | 6   | ns            |
| $t_{\text{PU}}$                      | $\overline{\text{CE}}$ LOW to power up                  | 0                       |     | 0   |     | ns            |
| $t_{\text{PD}}$                      | $\overline{\text{CE}}$ HIGH to power down               |                         | 10  |     | 12  | ns            |
| $t_{\text{DBE}}$                     | Byte enable to data valid                               | Industrial/Automotive-A |     | 5   | 6   | ns            |
|                                      |   | Automotive-E            |     |     | 8   |               |
| $t_{\text{LZBE}}$                    | Byte enable to Low Z                                    | 0                       |     | 0   |     | ns            |
| $t_{\text{HZBE}}$                    | Byte disable to High Z                                  |                         | 5   |     | 6   | ns            |
| <b>Write Cycle</b> <sup>[8, 9]</sup> |   |                         |     |     |     |               |
| $t_{\text{WC}}$                      | Write cycle time  | 10                      |     | 12  |     | ns            |
| $t_{\text{SCE}}$                     | $\overline{\text{CE}}$ LOW to write end                 | 7                       |     | 8   |     | ns            |
| $t_{\text{AW}}$                      | Address setup to write end                              | 7                       |     | 8   |     | ns            |
| $t_{\text{HA}}$                      | Address hold from write end                             | 0                       |     | 0   |     | ns            |
| $t_{\text{SA}}$                      | Address setup to write start                            | 0                       |     | 0   |     | ns            |
| $t_{\text{PWE}}$                     | $\overline{\text{WE}}$ pulse width                      | 7                       |     | 8   |     | ns            |
| $t_{\text{SD}}$                      | Data setup to write end                                 | 5                       |     | 6   |     | ns            |
| $t_{\text{HD}}$                      | Data hold from write end                                | 0                       |     | 0   |     | ns            |
| $t_{\text{LZWE}}$                    | $\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>     | 3                       |     | 3   |     | ns            |
| $t_{\text{HZWE}}$                    | $\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>  |                         | 5   |     | 6   | ns            |
| $t_{\text{BW}}$                      | Byte enable to end of write                             | 7                       |     | 8   |     | ns            |

### Notes

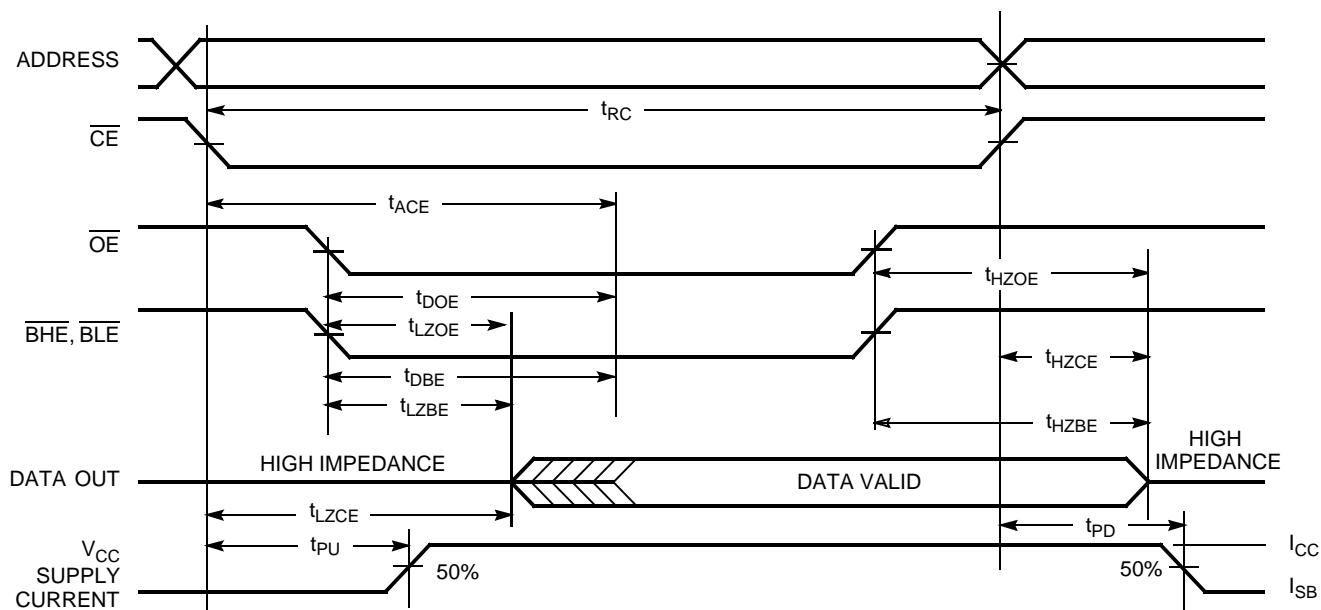
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
5.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
6. At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
7.  $t_{\text{HZOE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" [3] on page 6. Transition is measured  $\pm 500$  mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW,  $\overline{\text{WE}}$  LOW, and  $\overline{\text{BHE/BLE}}$  LOW.  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$ , and  $\overline{\text{BHE/BLE}}$  must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1 (Address Transition Controlled)<sup>[10, 11]</sup>**



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

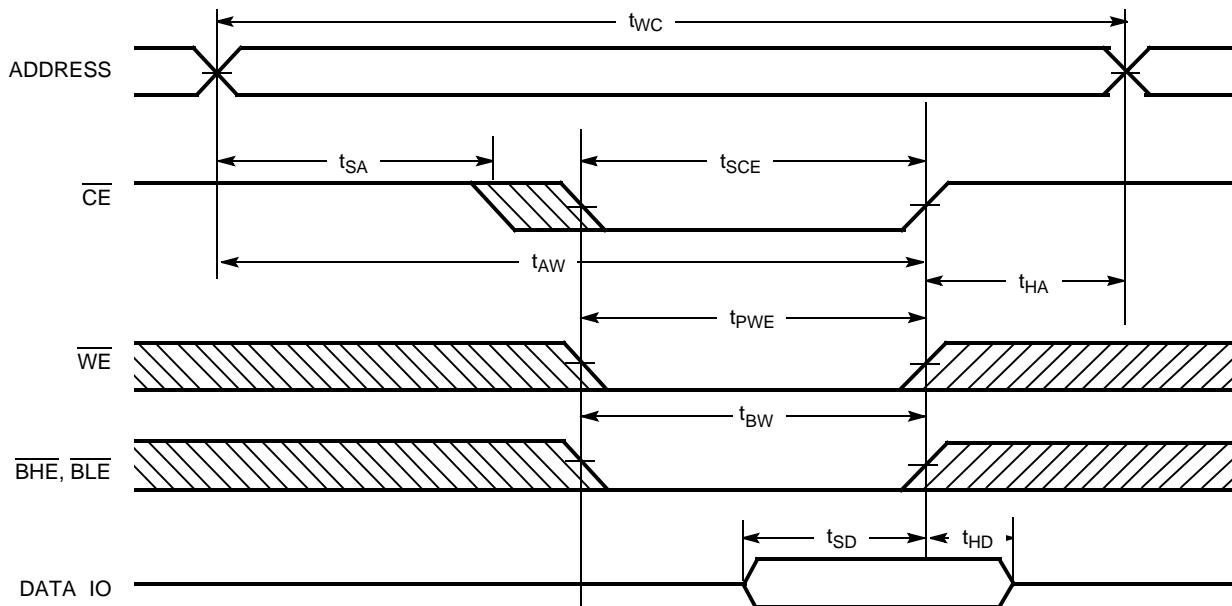


### Notes

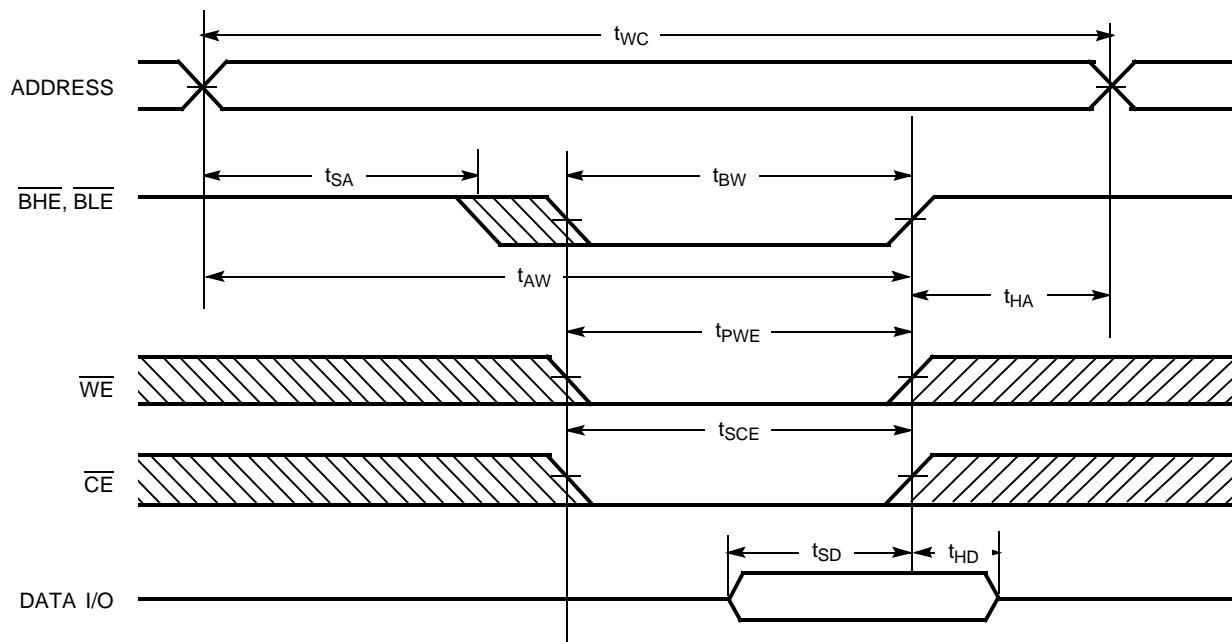
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE}$  =  $V_{IL}$ .
11. WE is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[13, 14]</sup>**



**Figure 8. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

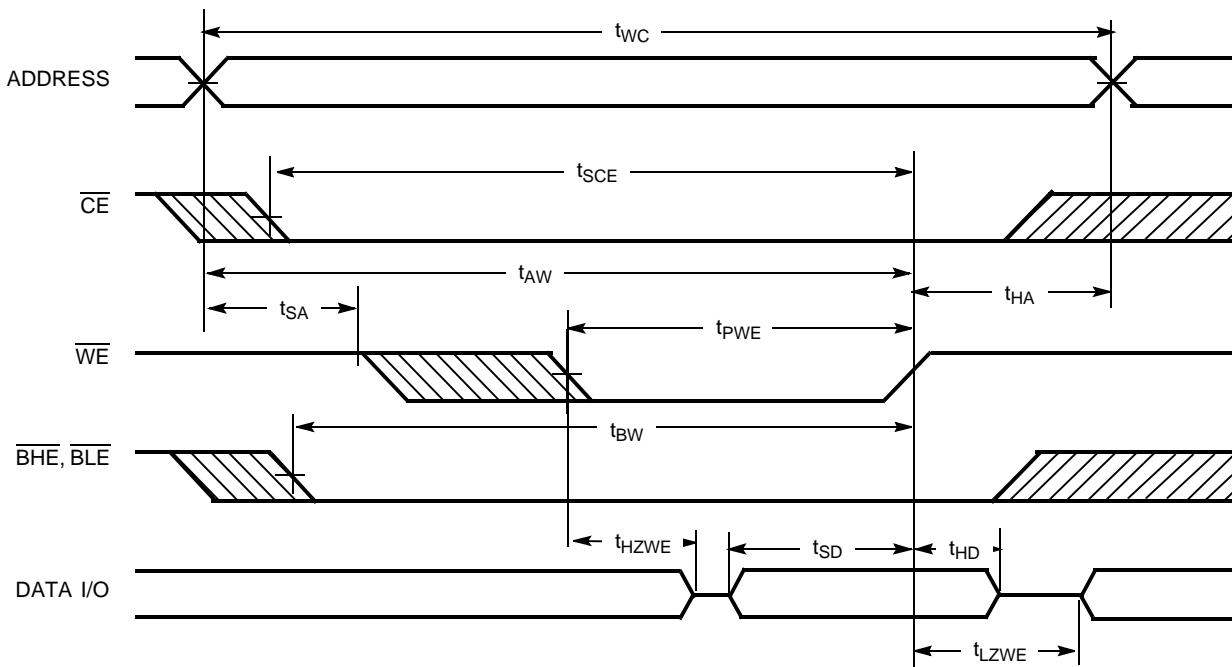


### Notes

13. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .
14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

## Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ( $\overline{WE}$  Controlled, LOW)



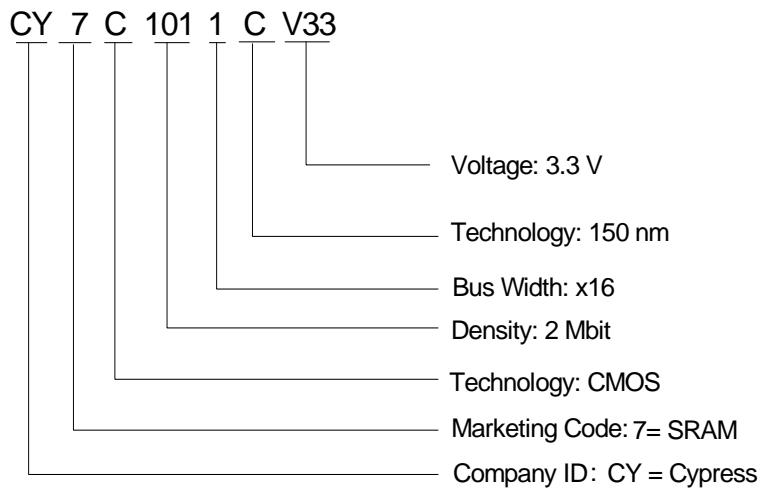
## Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $I/O_0 - I/O_7$ | $I/O_8 - I/O_{15}$ | Mode                       | Power                |
|-----------------|-----------------|-----------------|------------------|------------------|-----------------|--------------------|----------------------------|----------------------|
| H               | X               | X               | X                | X                | High Z          | High Z             | Power down                 | Standby ( $I_{SB}$ ) |
| L               | L               | H               | L                | L                | Data Out        | Data Out           | Read – all bits            | Active ( $I_{CC}$ )  |
| L               | L               | H               | L                | H                | Data Out        | High Z             | Read – lower bits only     | Active ( $I_{CC}$ )  |
| L               | L               | H               | H                | L                | High Z          | Data Out           | Read – upper bits only     | Active ( $I_{CC}$ )  |
| L               | X               | L               | L                | L                | Data In         | Data In            | Write – all bits           | Active ( $I_{CC}$ )  |
| L               | X               | L               | L                | H                | Data In         | High Z             | Write – lower bits only    | Active ( $I_{CC}$ )  |
| L               | X               | L               | H                | L                | High Z          | Data In            | Write – upper bits only    | Active ( $I_{CC}$ )  |
| L               | H               | H               | X                | X                | High Z          | High Z             | Selected, outputs disabled | Active ( $I_{CC}$ )  |

## Ordering Information

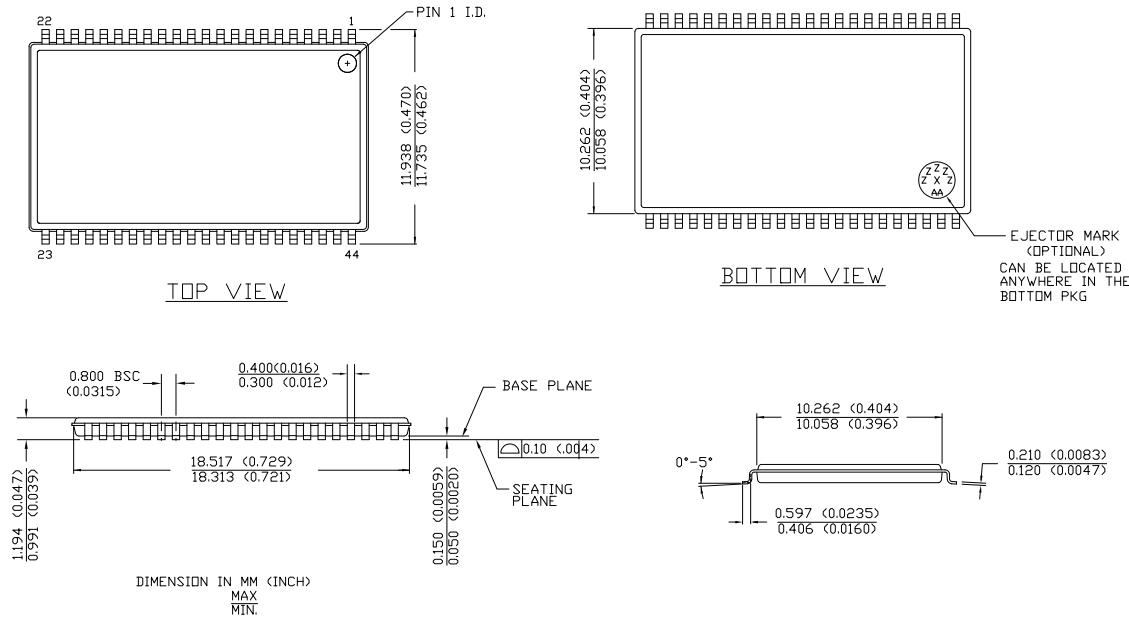
| Speed<br>(ns) | Ordering Code       | Package<br>Diagram | Package Type                 | Operating<br>Range |
|---------------|---------------------|--------------------|------------------------------|--------------------|
| 10            | CY7C1011CV33-10ZSXA | 51-85087           | 44-pin TSOP II (Pb-free)     | Automotive-A       |
| 12            | CY7C1011CV33-12AXI  | 51-85064           | 44-pin TQFP (Pb-free)        | Industrial         |
|               | CY7C1011CV33-12ZSXE | 51-85087           | 44-pin TSOP II (Pb-free)     | Automotive-E       |
|               | CY7C1011CV33-12BVXE | 51-85150           | 48-ball (6 x 8 x 1 mm) VFBGA |                    |

### Ordering Code Definition



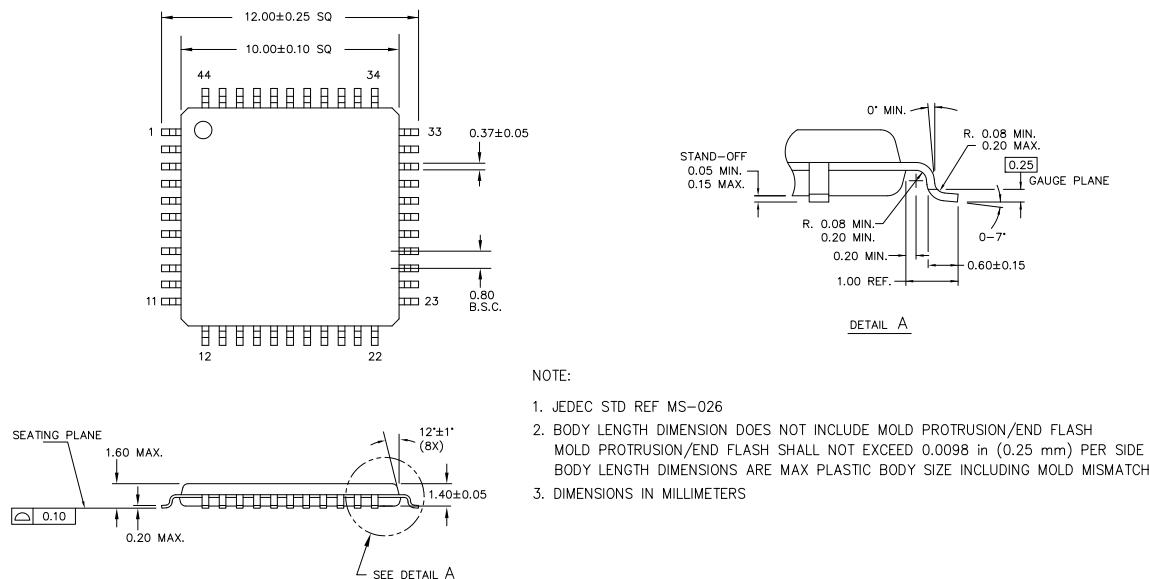
## Package Diagrams

**Figure 10. 44-Pin Thin Small Outline Package Type II, 51-85087**



## Package Diagrams (continued)

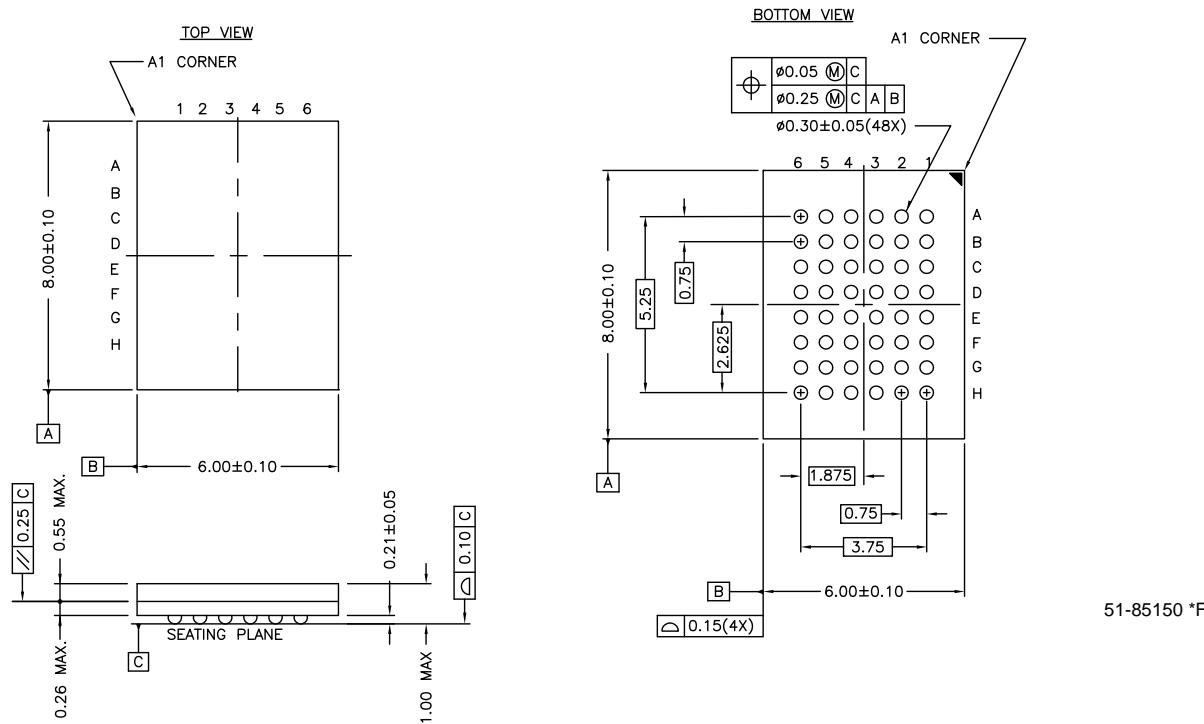
**Figure 11. 44-Pin Thin Plastic Quad Flat Pack, 51-85064**



51-85064 \*D

## Package Diagrams (continued)

Figure 12. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



## Acronyms

| Acronym | Description                             |
|---------|---|
| BHE     | Bye High Enable                         |
| BLE     | Byte Low Enable                         |
| CE      | Chip Enable                             |
| CMOS    | complementary metal oxide semiconductor |
| I/O     | input/output                            |
| SRAM    | static random access memory             |
| VFBGA   | very fine ball grid array               |
| TQFP    | thin quad flat pack                     |
| TSOP    | thin small outline package              |
| WE      | Write Enable                            |

## Document History Page

| Document Title: CY7C1011CV33, 2-Mbit (128K x 16) Static RAM |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Document Number: 38-05232                                   |         |            |                 |  |
| REV.  | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **  | 117132  | 07/31/02   | HGK             | New Data Sheet   |
| *A  | 118057  | 08/19/02   | HGK             | Pin configuration for 48-ball FBGA correction  |
| *B  | 119702  | 10/11/02   | DFP             | Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA   |
| *C  | 386106  | See ECN    | PCI             | Added lead-free parts in Ordering Information Table  |
| *D  | 498501  | See ECN    | NXR             | Corrected typo in the Logic Block Diagram on page# 1<br>Included the Maximum Ratings for Static Discharge Voltage and Latch up Current on page# 3<br>Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Updated the Ordering Information Table |
| *E  | 522620  | See ECN    | VKN             | Added Thermal Resistance Table   |
| *F  | 1891366 | See ECN    | VKN/AESA        | Added -10ZSX part<br>Updated Ordering Information table  |
| *G  | 2428606 | See ECN    | VKN/PYRS        | Corrected typo in the 44-Pin TSOP and 48-Ball FBGA pinout<br>Removed Commercial parts<br>Removed 15 ns speed bin<br>Removed inactive parts from the Ordering Information table   |
| *H  | 2664421 | 02/25/09   | VKN/AESA        | Added Automotive-E specs for 12 ns speed<br>Updated Ordering Information table   |
| *I  | 2898399 | 03/24/2010 | KAO/AJU         | Updated Package Diagrams   |
| *J  | 2950666 | 06/11/2010 | VKN             | Included "CY7C1011CV33-12BVXE" in Ordering Information<br>Added <a href="#">Contents</a> and <a href="#">Acronyms</a><br>Updated <a href="#">Sales, Solutions, and Legal Information</a><br>Added <a href="#">Ordering Code Definition</a> .   |
| *K  | 3089939 | 11/13/2010 | PRAS            | Removed inactive part from Ordering Information.   |

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