MCR12DG, MCR12MG, MCR12NG

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half−wave silicon gate−controlled devices are needed.

Features

- Blocking Voltage to 800 Volts
- On−State Current Rating of 12 Amperes RMS at 80°C
- High Surge Current Capability − 100 Amperes
- Rugged, Economical TO−220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT an IH Specified for Ease of Design
- High Immunity to dv/dt − 100 V/μsec Minimum at 125°C
- These are Pb−Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR12D MCR12M MCR12N	V_{DRM}, V_{RRM}	 400 600 800	V
On-State RMS Current (180° Conduction Angles; T_C = 80°C)	$I_{T(RMS)}$	12	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T_J = 125°C)	I_{TSM}	100	A
Circuit Fusing Consideration (t = 8.33 ms)	I^2t	41	A^2sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 80°C)	P_{GM}	5.0	W
Forward Average Gate Power (t = 8.3 ms, T_C = 80°C)	$P_{G(AV)}$	0.5	W
Average On-State Current (180° Conduction Angles; T_C = 80°C)	$I_{T(AV)}$	7.8	A
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T_C = 90°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

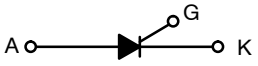
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

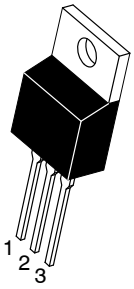
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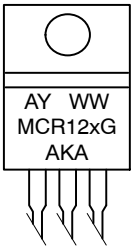
SCRs
12 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO−220
CASE 221A−09
STYLE 3



A = Assembly Location
Y = Year
WW = Work Week
x = D, M, or N
G = Pb−Free Package
AKA = Diode Polarity

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
MCR12DG	TO−220AB (Pb−Free)	50 Units / Rail
MCR12MG	TO−220AB (Pb−Free)	50 Units / Rail
MCR12NG	TO−220AB (Pb−Free)	50 Units / Rail

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THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance,	Junction−to−Case Junction−to−Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds		T_L	260	°C

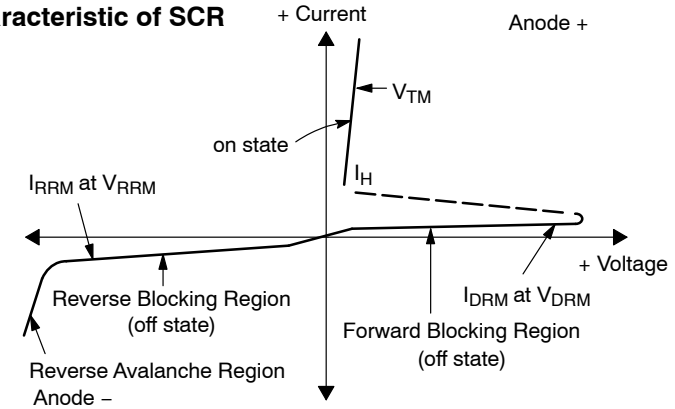
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_D = Rated V_{DRM} and V_{RRM}; Gate Open)	T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	– –	– –	0.01 2.0	mA
ON CHARACTERISTICS						
Peak Forward On−State Voltage (Note 2) (I_{TM} = 24 A)		V_{TM}	–	–	2.2	V
Gate Trigger Current (Continuous dc) (V_D = 12 V; R_L = 100 Ω)		I_{GT}	2.0	8.0	20	mA
Holding Current (V_D = 12 V, Gate Open, Initiating Current = 200 mA)		I_H	4.0	20	40	mA
Latch Current (V_D = 12 V, I_G = 20 mA)		I_L	6.0	25	60	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V; R_L =100 Ω)		V_{GT}	0.5	0.65	1.0	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)		dv/dt	100	250	–	V/μs
Repetitive Critical Rate of Rise of On−State Current IPK = 50 A, Pw = 40 μsec, diG/dt = 1 A/μsec, Igt = 50 mA		di/dt	–	–	50	A/μs

2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current



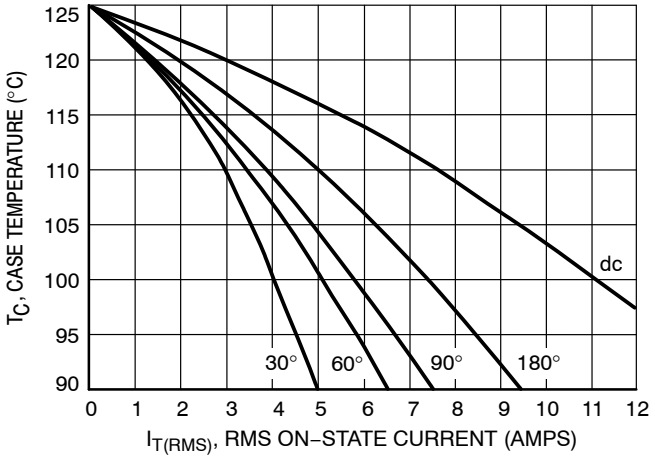


Figure 1. Typical RMS Current Derating

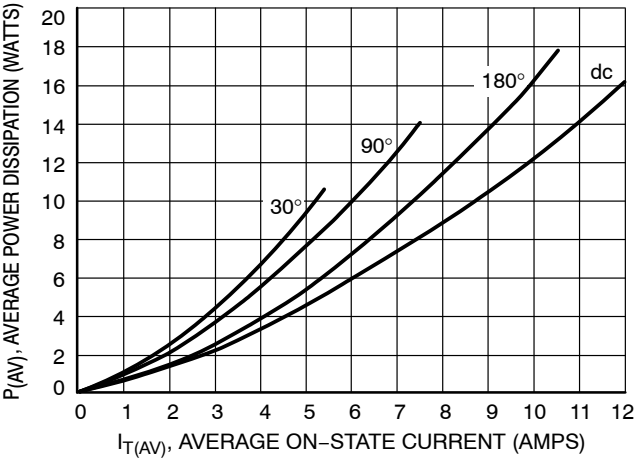


Figure 2. On−State Power Dissipation

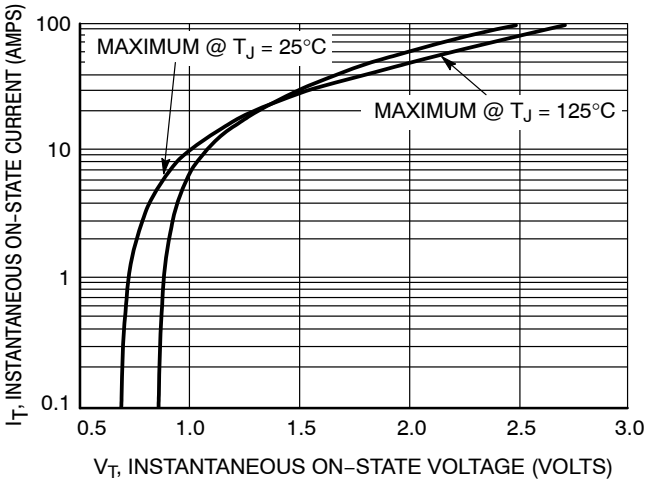


Figure 3. Typical On−State Characteristics

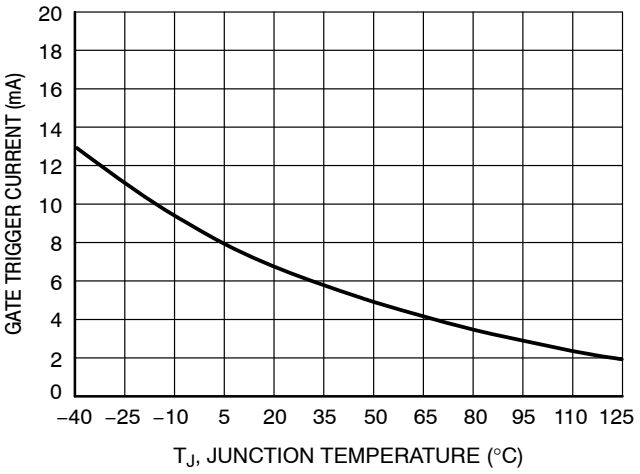


Figure 4. Typical Gate Trigger Current versus Junction Temperature

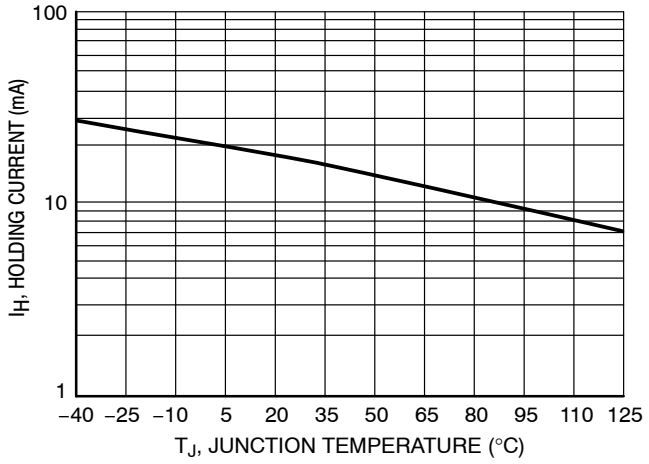


Figure 5. Typical Holding Current versus Junction Temperature

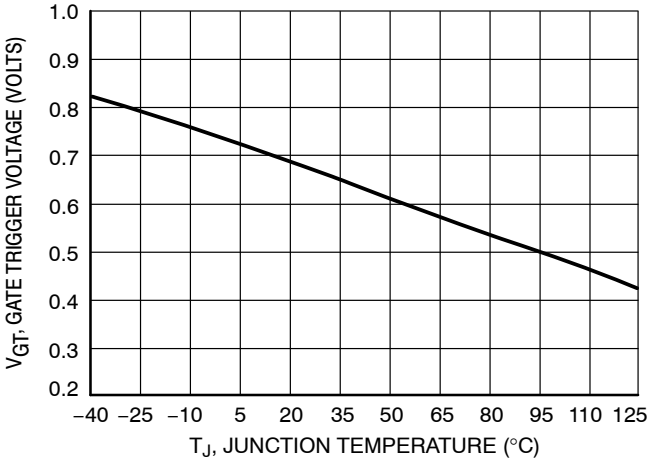


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

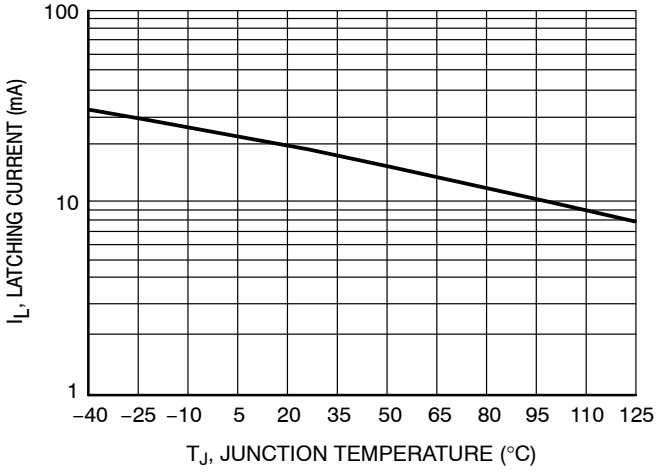
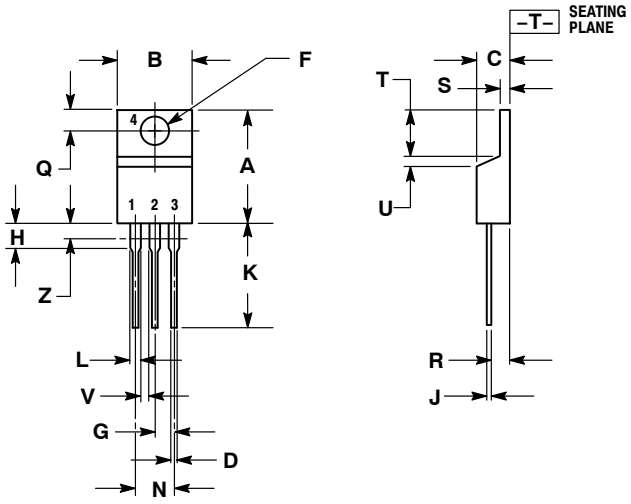


Figure 7. Typical Latching Current versus Junction Temperature

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

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