Description

The ACE25AB400G Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO). The Dual I/O data is transferred at a speed of 240Mbits/s.

Features

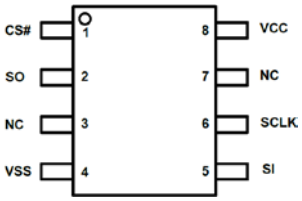
- 4M-bit Serial Flash
  - 512 K-byte
  - 256 bytes per programmable page
- Standard , Dual SPI
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
- Flexible Architecture
  - Sector of 4K-byte
  - Block of 32k-byte
  - Block of 64k-byte
- Software Write Protection
  - Write protect all/portion of memory via soft- ware
- Package Options
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halo- gen-Free and REACH.
- Temperature Range & Moisture Sensitivity Level
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- Low Power Consumption
  - 20mA maximum active current
  - 0.05uA maximum standby current
- Single Power Supply Voltage: Full voltage range:2.7~3.6V
- Support 128 bits Unique ID
- Minimum 100,000 Program/Erase Cycle
- High Speed Clock Frequency
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
- Program/Erase Speed
  - Page Program time: 1.0ms typical
  - Sector Erase time: 60ms typical
  - Block Erase time:0.3s/ 0.45s typical
  - Chip Erase time: 3.2s typical

Absolute Maximum Ratings

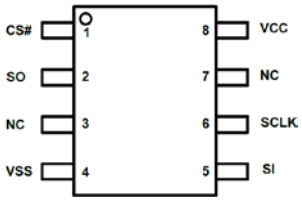
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Packaging Type

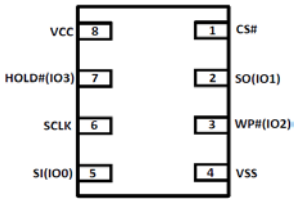
SOP-8/SOP-8L



TSSOP-8



USON3*2-8



Pin Configurations

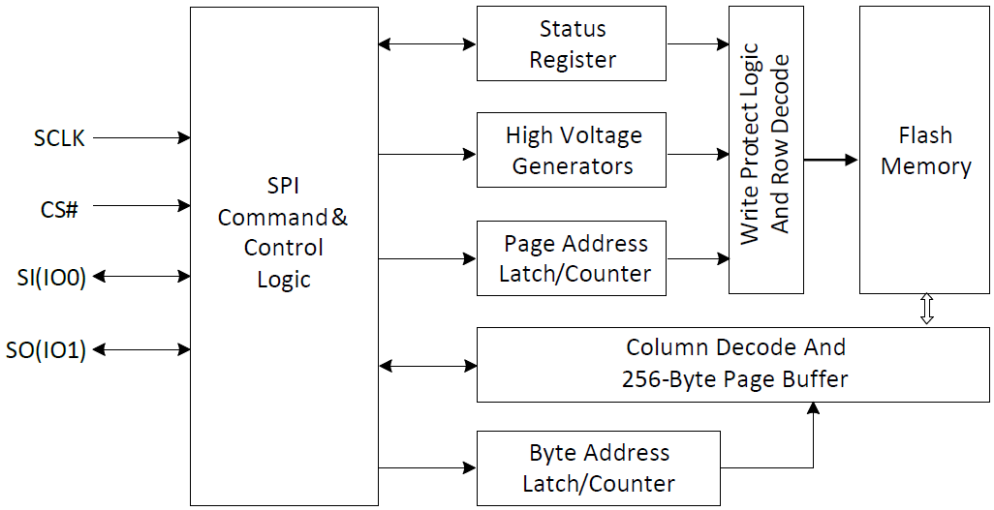
Pin Name	I/O	Functions
CS#	I	Chip Select Input
SO(IO1)	O	Data Output(Data Input Output 1)
VSS		Ground
SI(IO0)	I/O	Data Input(Data Input Output 0)
SCLK	I	Serial Clock Input
VCC		Power Supply

Ordering information

ACE25AB400G XX + X H

- Halogen-free
- U: Tube
  T: Tape and Reel
- Pb - free
- FM: SOP-8
  FML: SOP-8L (208mil)
  TM: TSSOP-8
  UA8: USON3*2-8

Block Diagram



Uniform Block Sector Architecture

ACE25AB400G 64K Bytes Block Sector Architecture

Block	Sector	Address Range	
7	127	07F000H	07FFFFH
	……	……	……
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	……	……	……
	96	060000H	060FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

Device Operation

Standard SPI

The ACE25AB400G features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The ACE25AB400G supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Data Protection

The ACE25AB400G provides the following data protection methods:

Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:

- Power-Up
- Write Disable (WRDI)
- Write Status Register (WRSR)
- Page Program (PP)
- Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)

Software Protection Mode:

- SRWD=0, the Block Protect (BP1, BP0) bits define the section of the memory array that can be read but not change
- SRWD=1, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP1, BP0) are read only.

Table 1.ACE25AB400G Protected Area Sizes

Status bit			Protect level	Protect Block
BP1	BP2	BP0		
0	0	0	0(none)	None
0	0	1	1 (1 block)	Block 7
0	1	0	2 (2 blocks)	Block 6-7
0	1	1	3 (4 blocks)	Block 4-7
1	0	0	4 (8 blocks)	All
1	0	1	5 (All)	All
1	1	0	6 (All)	All
1	1	1	7 (All)	All

Status Register

S7	S6	S5	S4	S3	S2	S1	S0
SRWD	LB1	LB0	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status regis- ter progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

LB1, LB0 bits.

The LB1, LB0 are non-volatile One Time Program (OTP) bits in Status Register (S5) that provide the write protect control and status to the Security Registers. The default state of LB1 and LB0 are 0, the security registers are unlocked. LB1, LB0 can be set to 1 using the Write Register instruction. LB1, LB0 are One Time Programmable, once they were set to 1, the corresponding Security Registers will become read-only permanently.

BP2, BP1, BP0 bits.

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1.0) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. Chip Erase command will be ignored if one or more of the Block Protect (BP2, BP1, BP0) bits are 1.

SRWD bit.

The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit in the status reg- ister that provide another software protection. Once it is set to 1, the Write Status Register (WRSR) instruction is not accepted and the Block Protect bits (BP2, BP1, BP0) are read only.

SRWD	Status register
0	Status register can be written in (WEL bit is set to “1”) and the SRWD, BP2-BP0 bits can be changed
1	The BP2-BP0 of status register bits cannot be changed

Commands Description

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary; otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# be- ing driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Write Status Register	01H	(S7-S0)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Continuous read reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Deep Power-Down	B9H						
Release From Deep Power-Down, and Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Read Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Read Unique ID	4BH	00H	00H	00H	00H	(D7-D0)	
Read SFDP	5AH						
Erase Security Register	44H	A23-A16	A15-A8	A7-A0			
Program Security Register	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	
Enable Reset	66H						
Reset	99H						

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

3. Security Registers Address:

   Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address

   Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address

ID Definitions

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	13
90H	0B		12
ABH			12

Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→Sending the Write Enable command→CS# goes high.

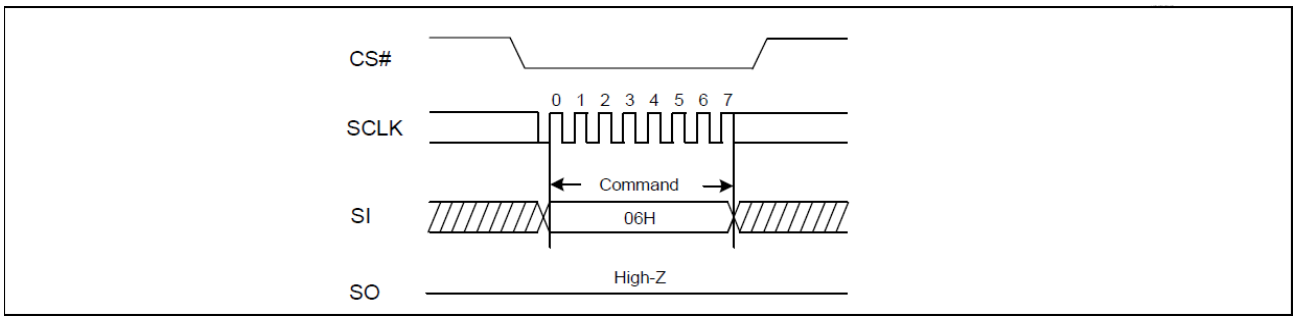


Figure1. Write Enable Sequence Diagram

Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non- volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

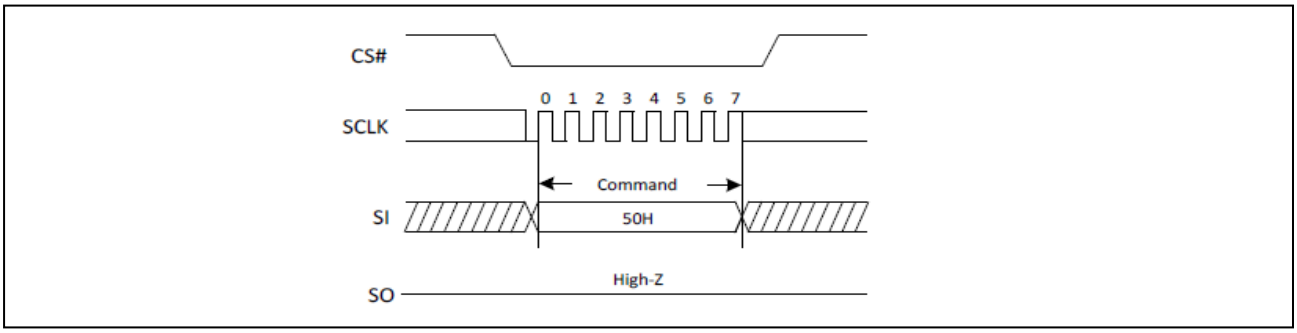


Figure2. Write Enable for Volatile Status Register Sequence Diagram

Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→Sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

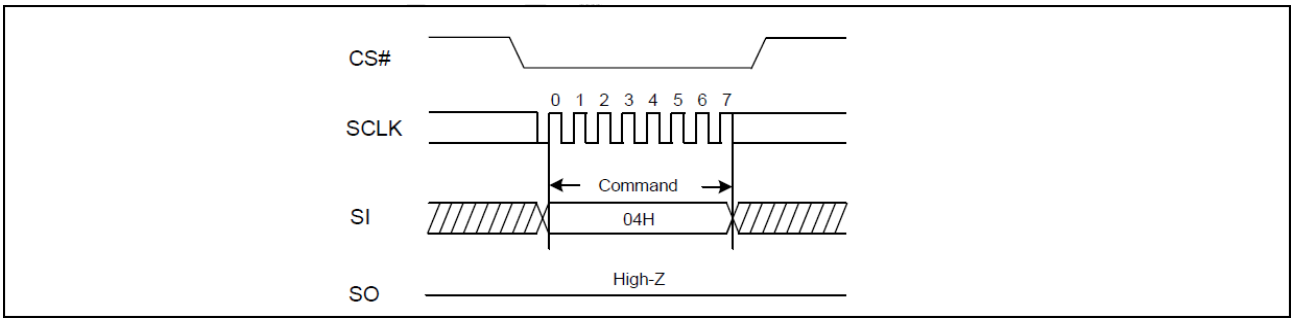


Figure3. Write Disable Sequence Diagram

Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

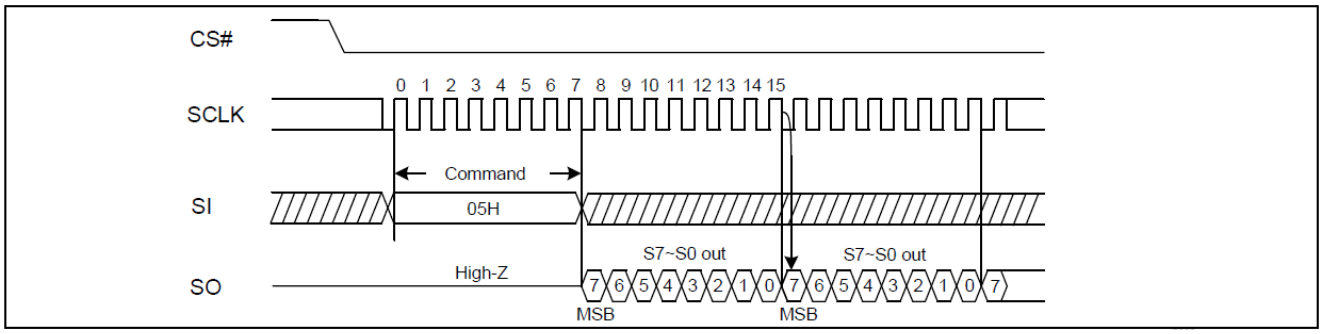


Figure4. Read Status Register Sequence Diagram

Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S6, S5, S4, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self- timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1.0. The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit, the Write Status Register (WRSR) command allows the user to set the Status Register Write Disable (SRWD) bit to 1. The Status Register Write Disable (SRWD) bit allow the device to be put in another Software Protected Mode. Once the SRWD bit is set to 1, the Write Status Register (WRSR) command is not executed, and the Block Protect bits (BP1, BP0) are read only.

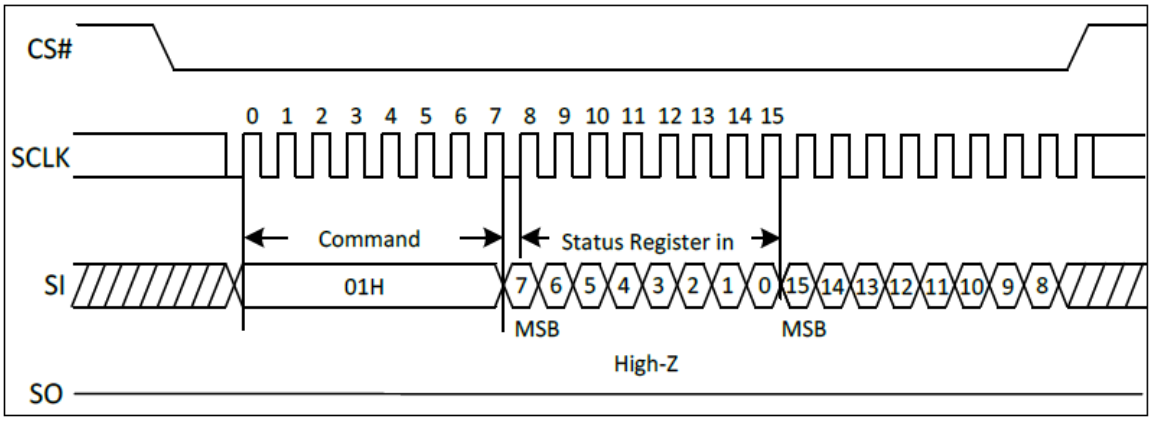


Figure5. Write Status Register Sequence Diagram

Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Therefore, the whole memory can be read with a single Read Data Bytes (READ) command. During an Erase, Program or Write cycle, Read Data Byte (READ) command will be rejected without affecting the cycle in progress.

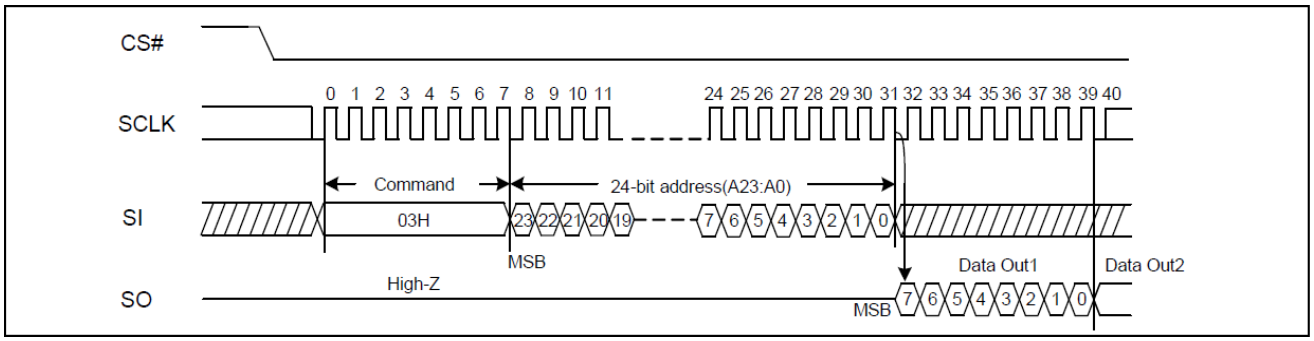


Figure6. Read Data Bytes Sequence Diagram

Read Data Bytes At Higher Speed (Fast Read)(0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

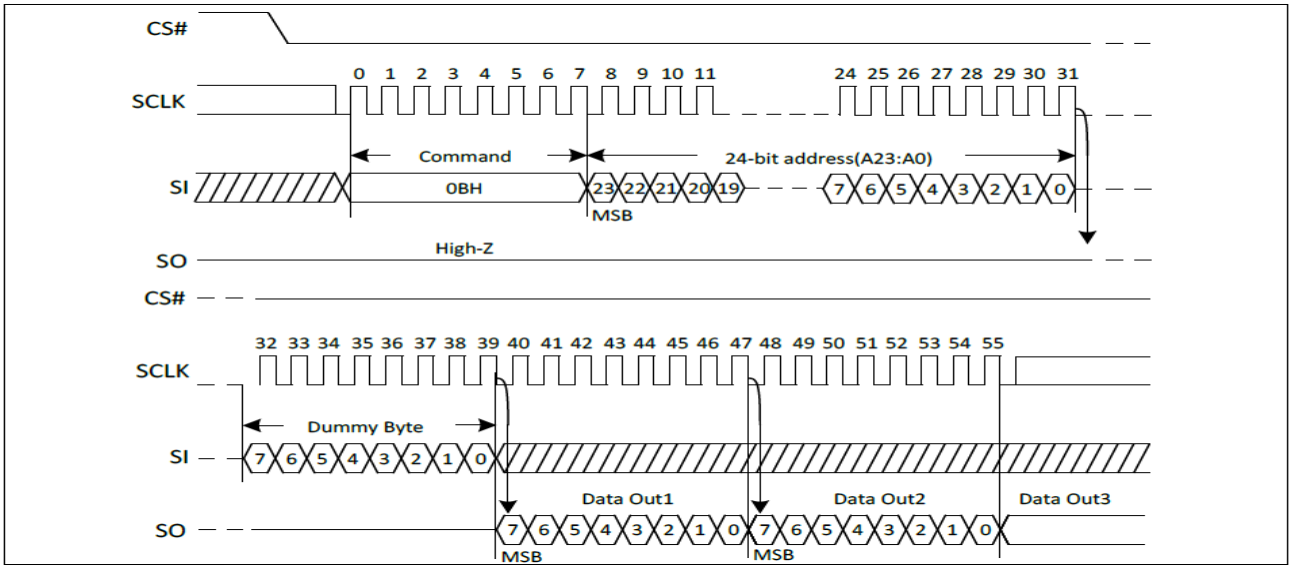


Figure7. Read Data Bytes at Higher Speed Sequence Diagram

Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

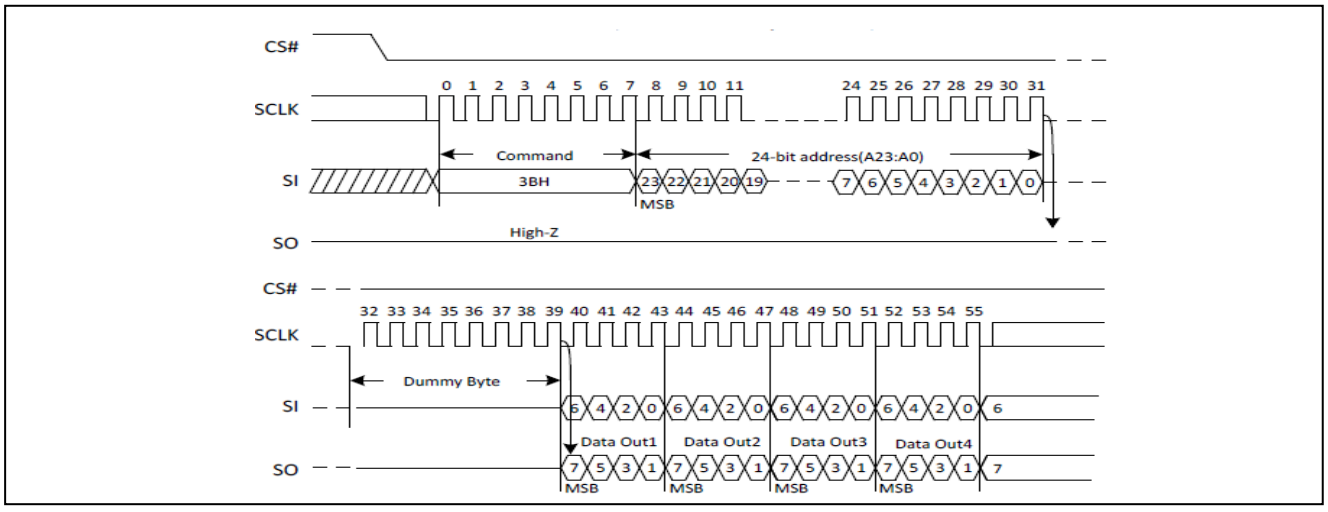


Figure8.Dual Output Fast Read Sequence Diagram

Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 11. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7- 0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4)=(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 12. If the “Continuous Read Mode” bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

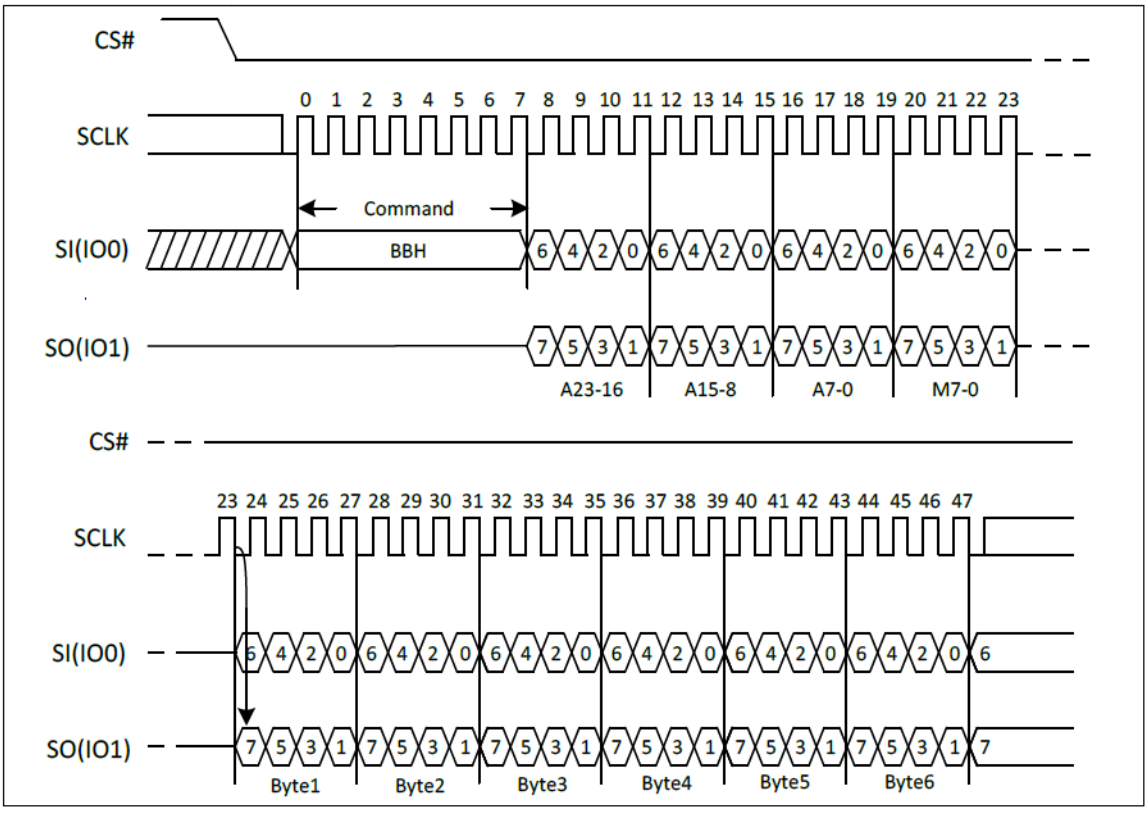


Figure9. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

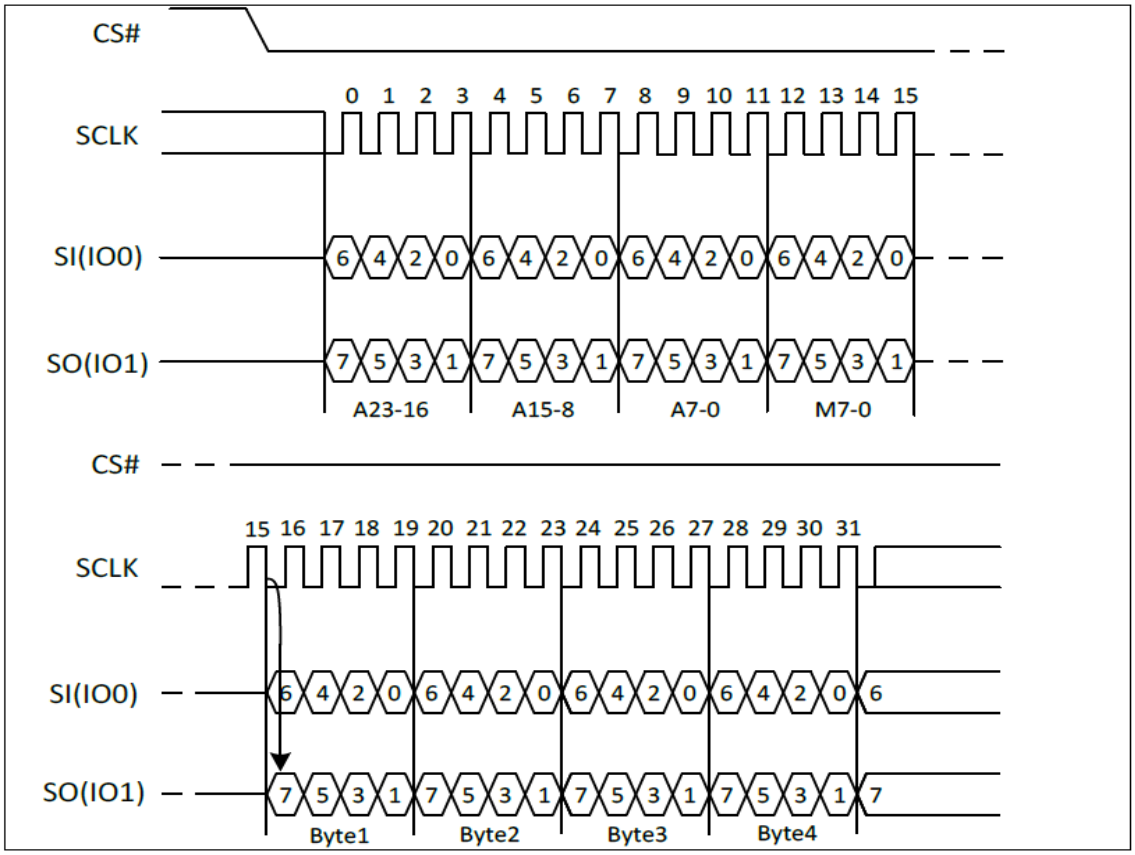


Figure9a. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))

Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low→sending Page Program command→3-byte address on SI→at least 1 byte data on SI→CS# goes high. The command sequence is shown in Figure10. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. As some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP1, BP0) is not executed.

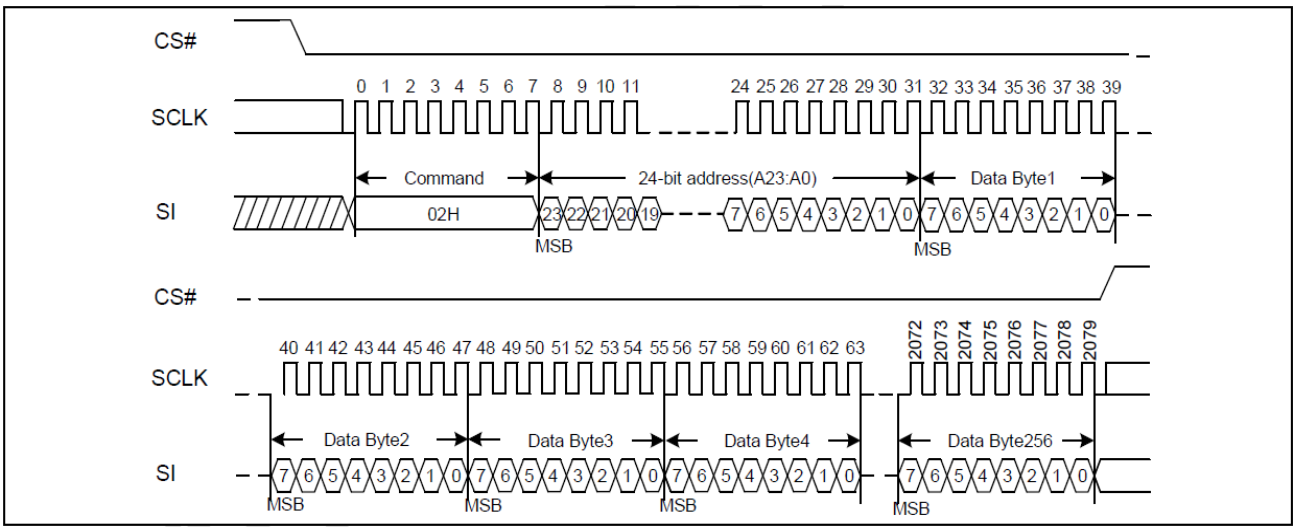


Figure10. Page Program Sequence Diagram

Sector Erase (SE) (20H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program com- mand.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low □ gram command □ byte address on SI □ at lea goes high. The command sequence is shown in Figure 10. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Pro- gress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP1, BP0) is not executed.

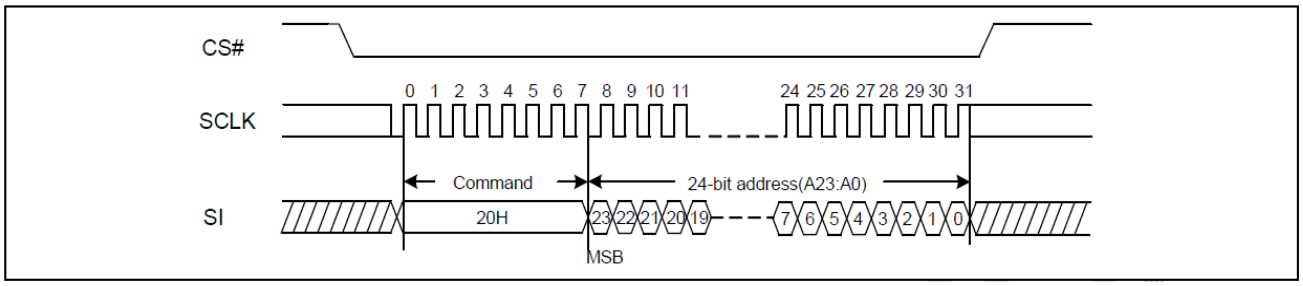


Figure11. Sector Erase Sequence Diagram

64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low→sending 64KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure12. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. Write Enable Latch (WEL) bit is reset t. A 64KB Block Erase (BE) commands applied to a block which is protected by the Block Protect (BP1, BP0) bits (see Table1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase, thus recommend performing a re-erase once power resume.

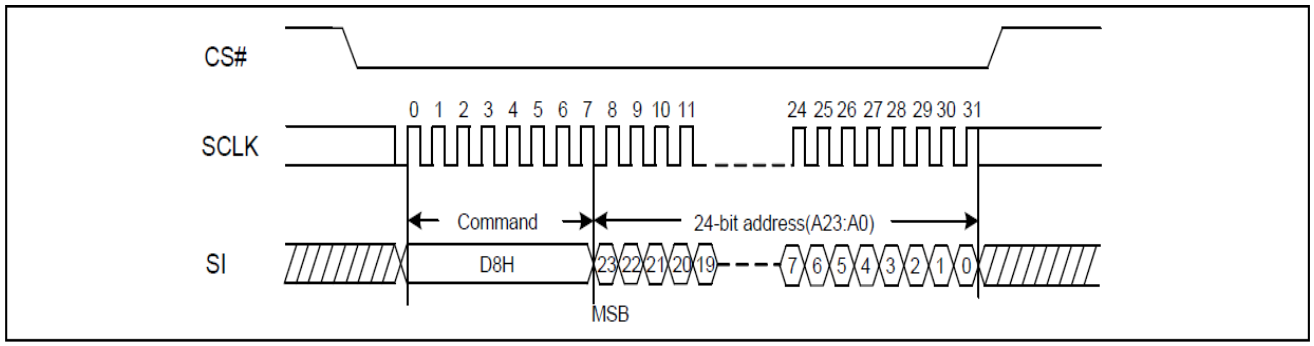


Figure12. 64KB Block Erase Sequence Diagram

Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low→sending Chip Erase command →CS# goes high. The command sequence is shown in Figure 13. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self- timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP1, BP0) bits are all 0. The Chip Erase (CE) command is ignored if one or more sectors are protected. Note: Power disruption during erase operation will cause incomplete erase, thus recommend performing a re-erase once power resume.

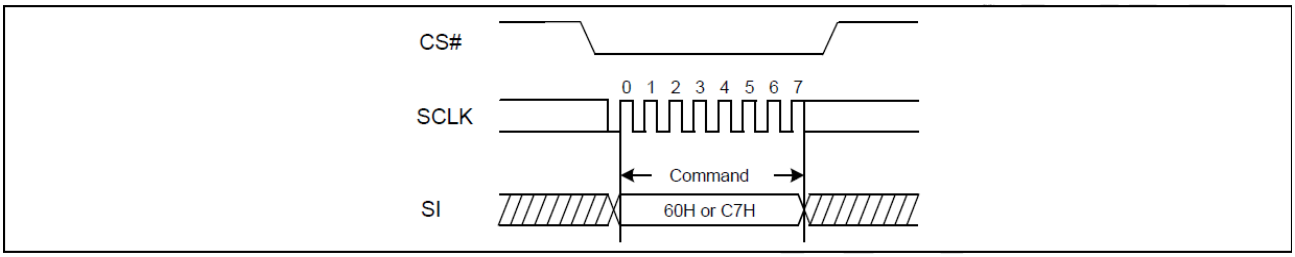


Figure13. Chip Erase Sequence Diagram

Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command support a way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be out- put on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low→sending Deep Power-Down command→ CS# goes high. The command sequence is shown in Figure 14. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Pow- er-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

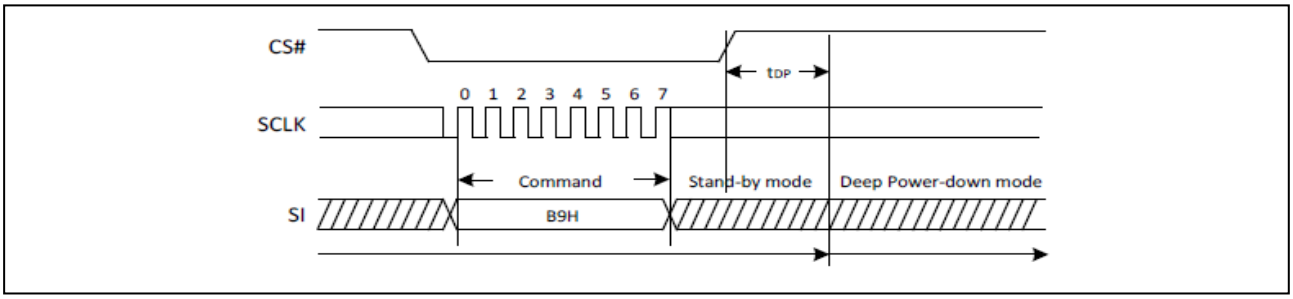


Figure14. Deep Power-Down Sequence Diagram

Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number. To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure15. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure16. The Device ID value for the ACE25AB400G is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure16, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

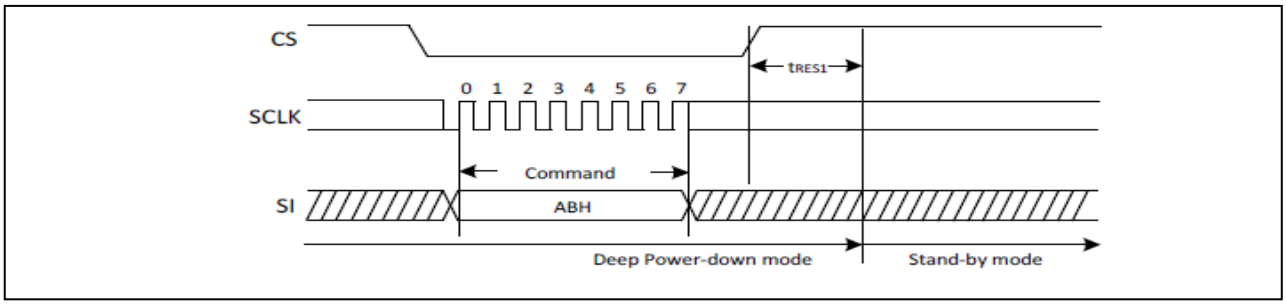


Figure15. Release Power-Down Sequence Diagram

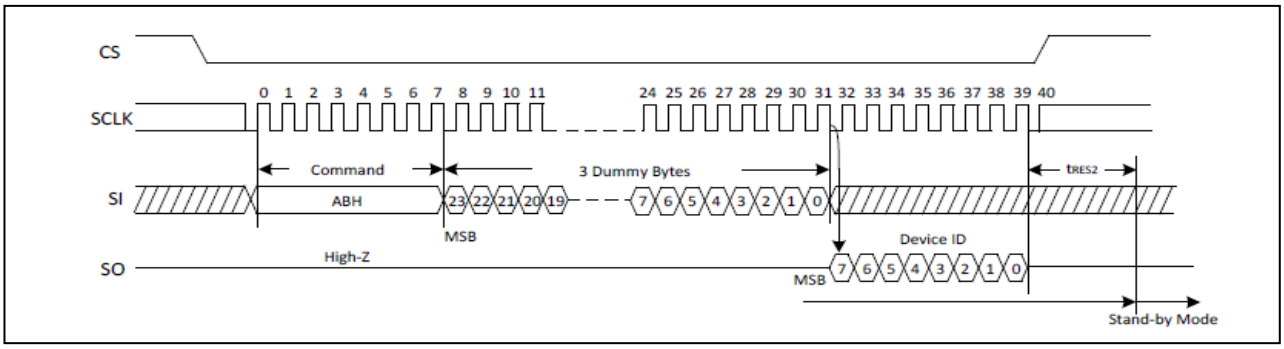


Figure16. Release Power-Down /Read Device ID Sequence Diagram

Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is for reading both the JEDEC assigned Manufacturer ID and the specific Device ID. The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure17. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

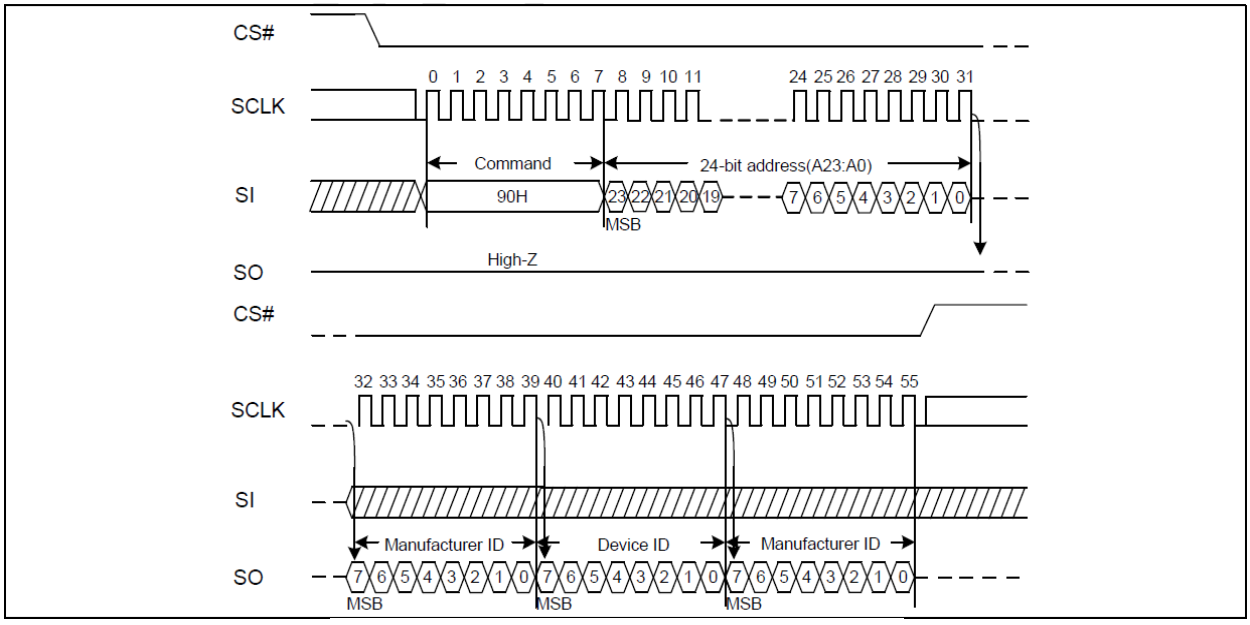


Figure17. Read Sequence Diagram

32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI.

Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low→sending 32KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure18. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated.

While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

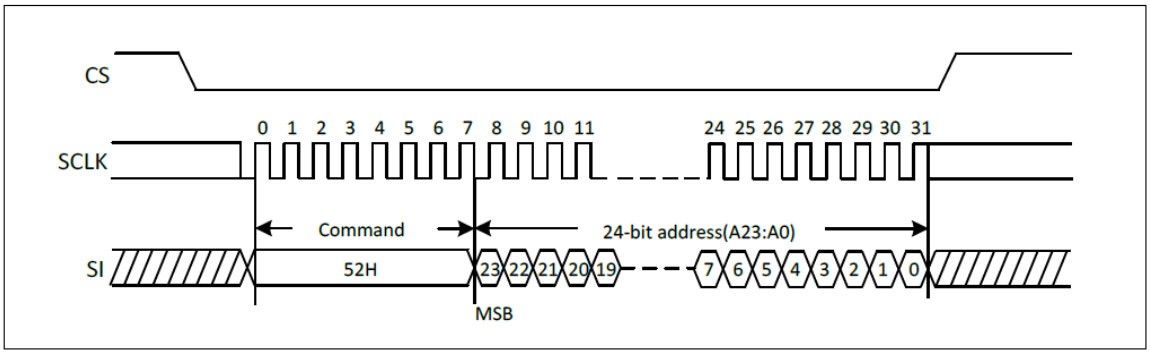


Figure18. 32KB Block Erase Sequence Diagram

Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read identification (RDID)command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure19. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

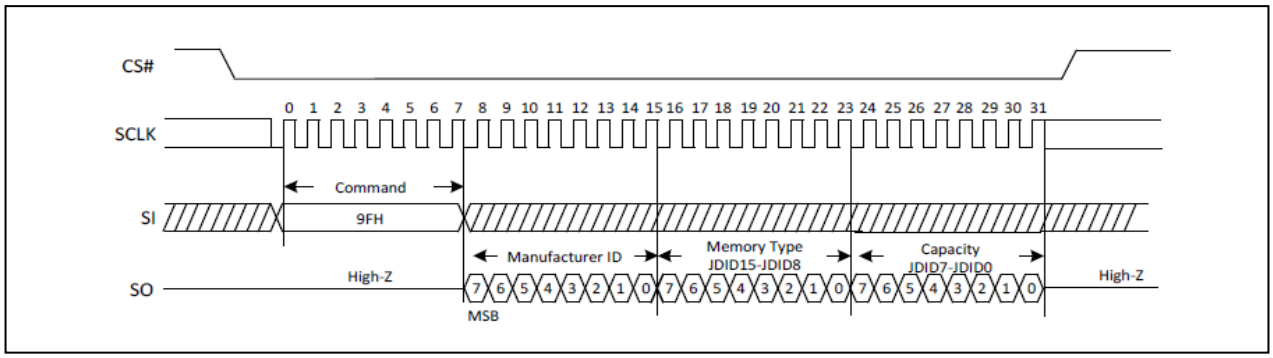


Figure19. Read Identification ID Sequence Diagram

Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each ACE25AB400G device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command sequence: CS# goes low→ sending Read Unique ID command→00H→00H→0H→128bit Unique ID Out→CS# goes high.

The command sequence is show below.

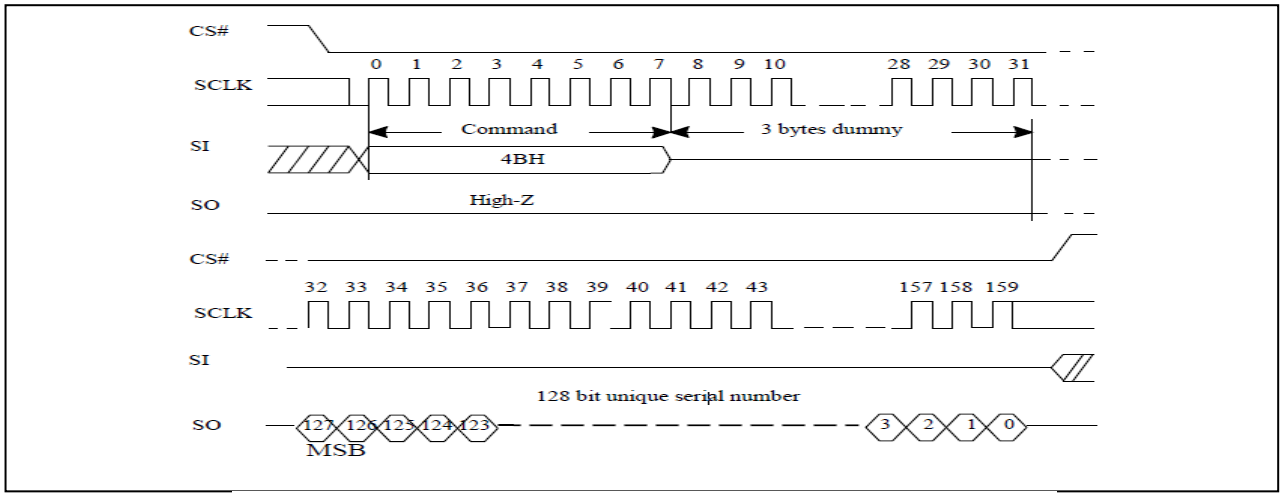


Figure20 Read Unique ID (RUID) Sequence (Command 4B)

Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

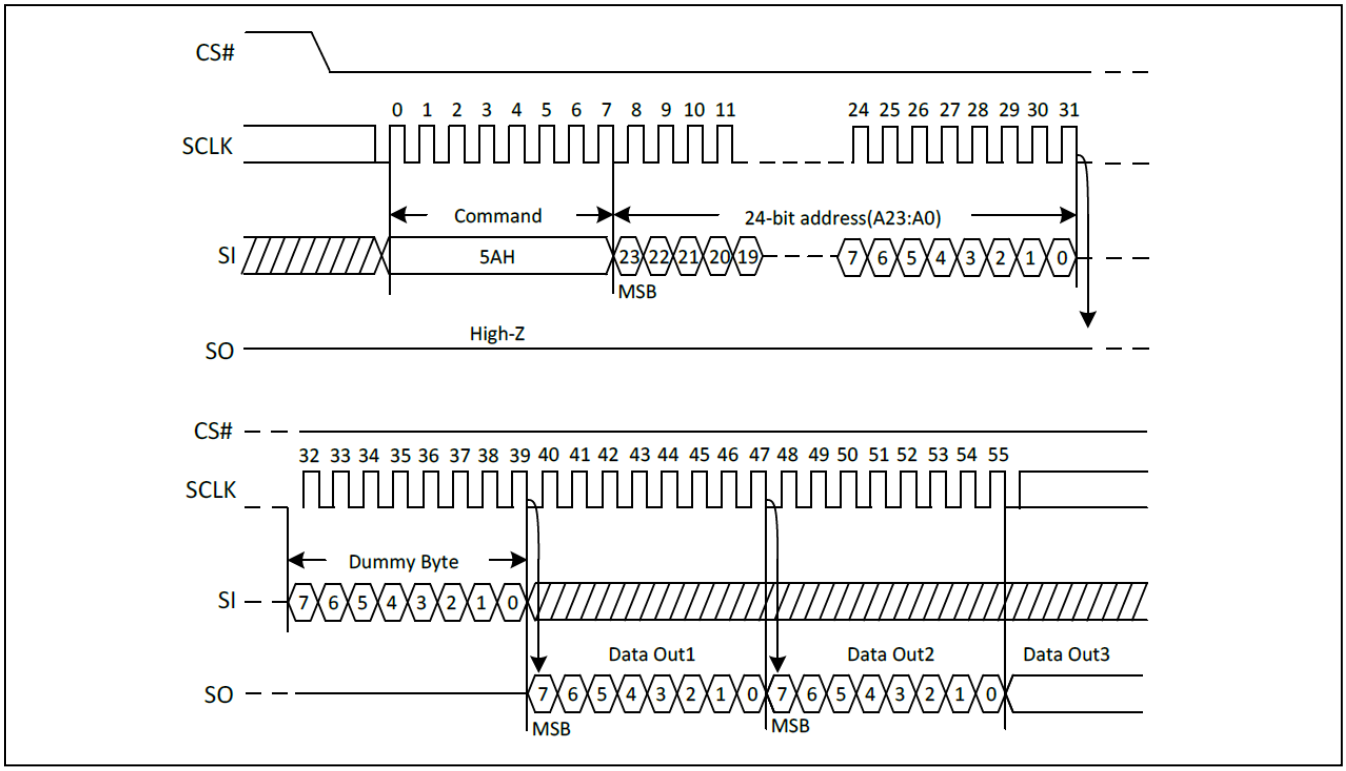


Figure21. Read Serial Flash Discoverable Parameter command Sequence Diagram

Erase Security Registers (44H)

The ACE25AB400G provides two 256-byte Security Registers which only erased all at once but able to pro- gram individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low, sending Erase Security Registers Command, CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated.

While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Don't Care

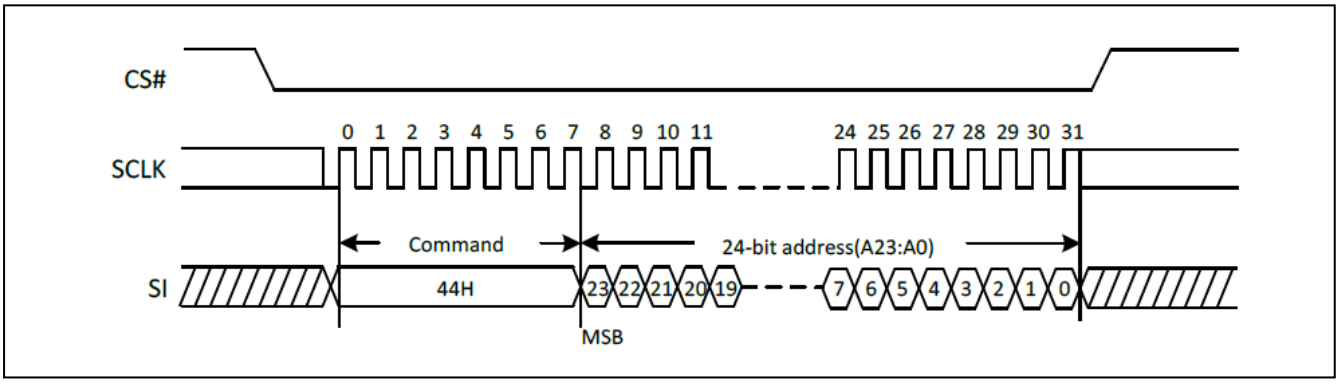


Figure22. Erase Security Registers command Sequence Diagram

Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address

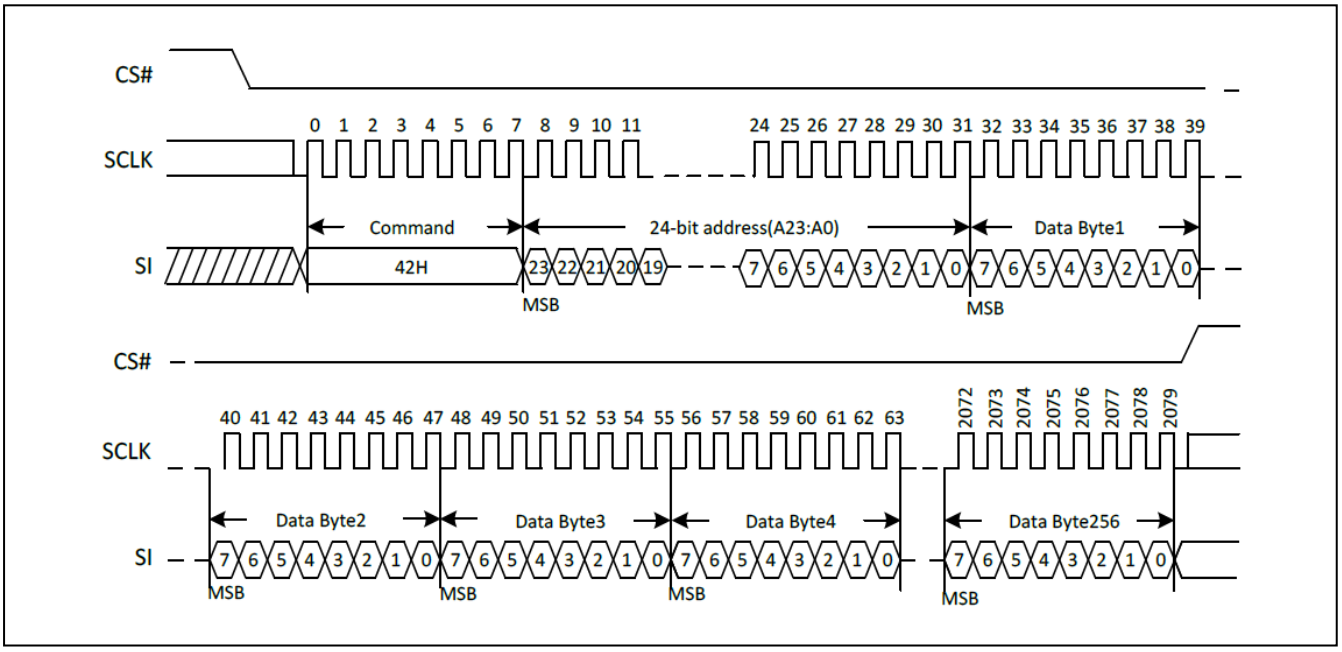


Figure23. Program Security Registers command Sequence Diagram

Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3- byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Address

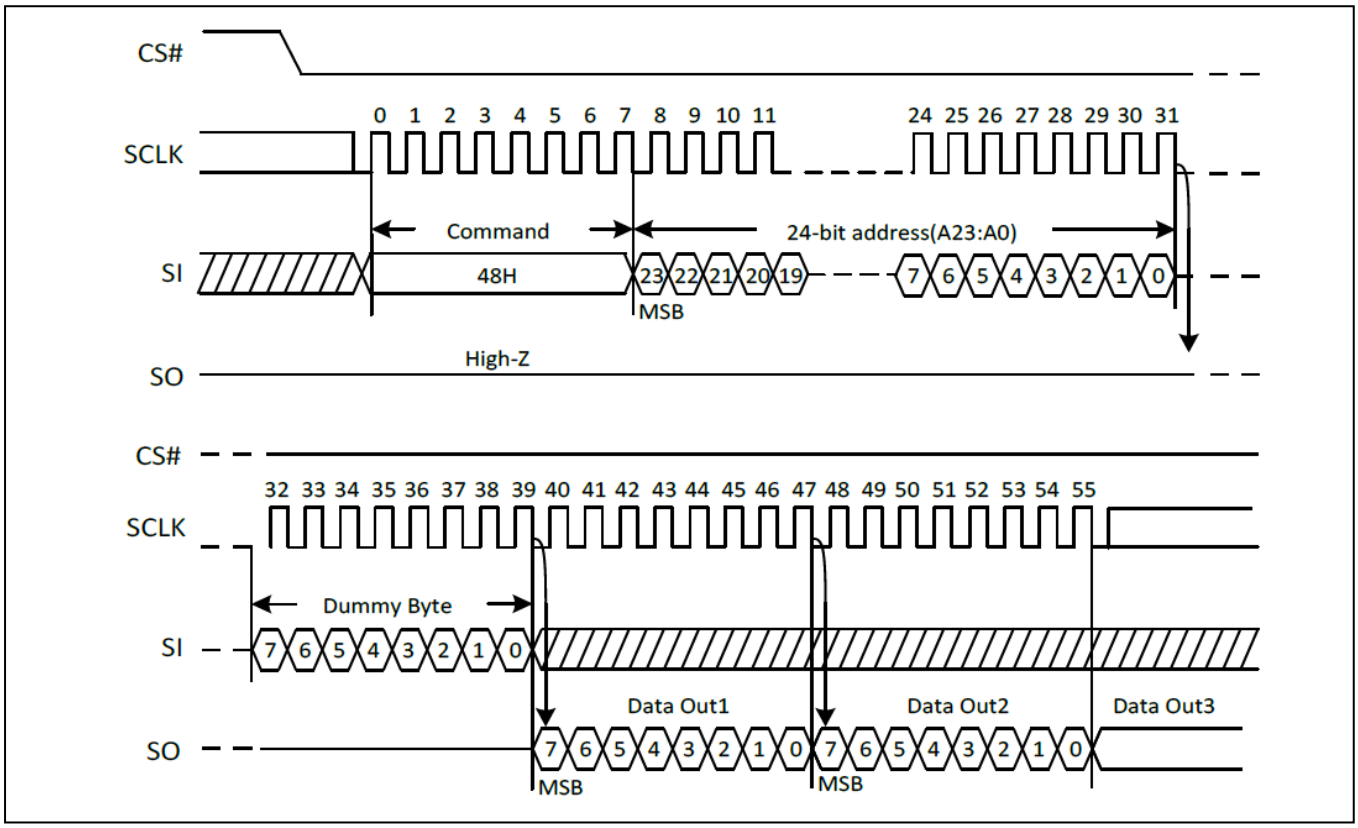


Figure24. Read Security Registers command Sequence Diagram

Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL).

The “Reset (99H)” command sequence as follow: CS# goes low→Sending Enable Reset command→ CS# goes high→CS# goes low→Sending Reset command→CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRSTR to reset. During this period, no command will be accepted.

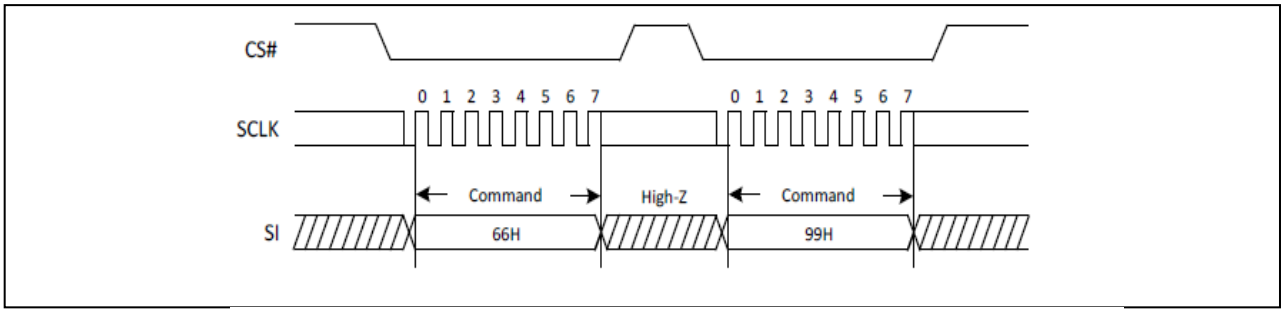


Figure25. Enable Reset and Reset command Sequence Diagram

Continuous Read Mode Reset (CRMR) (FFH)

The Dual I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual I/O Fast Read operations do not require the BBH command code.

Because the ACE25AB400G has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the ACE25AB400G will not recognize any standard SPI commands. So Continuous Read Mode Reset command will re- lease the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is shown in Figure 26.

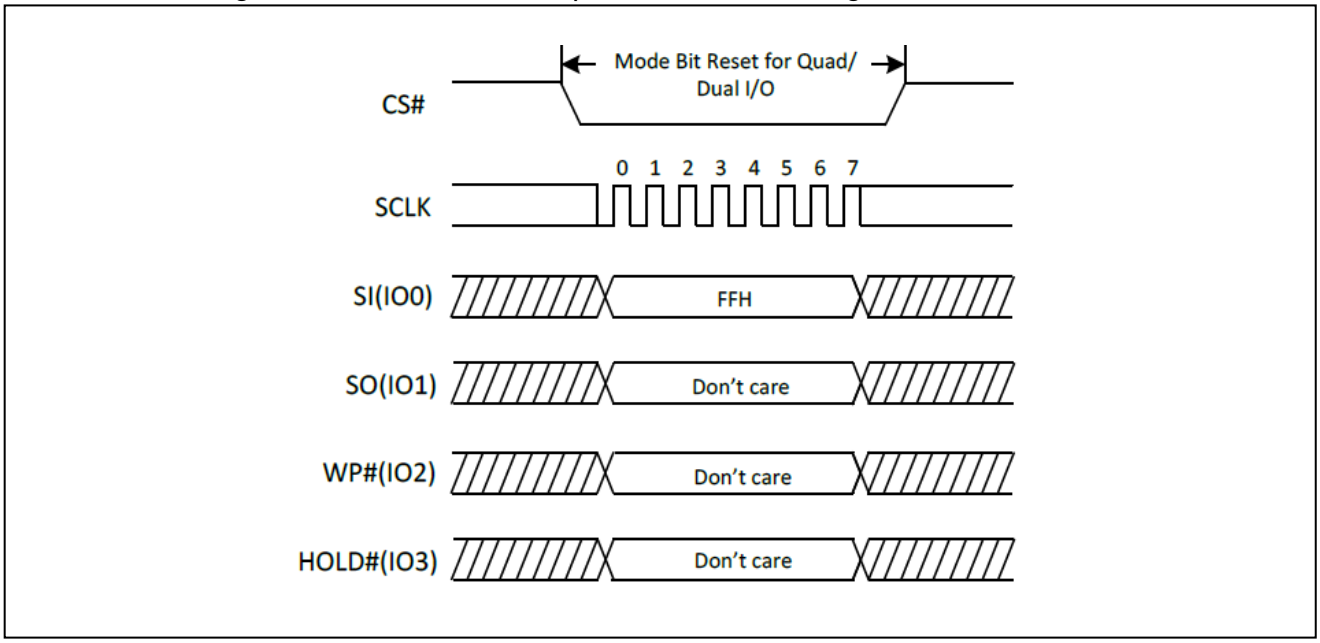


Figure26. Continuous Read Mode Reset Sequence Diagram

Electrical Characteristics

Power-On Timing

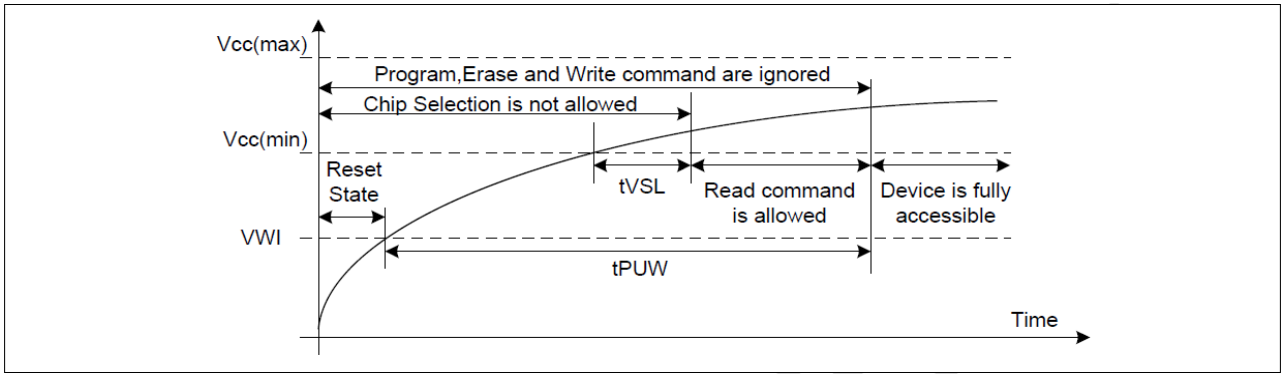


Table3. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	10	ms
V_{WI}	Write Inhibit Voltage	1	2.5	V

Note: An interval of 10ms (minimum) is required between the power-down state and next power-on-reset event.

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

Data Retention and Endurance

Parameter	Typical	Unit
Minimum Pattern Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

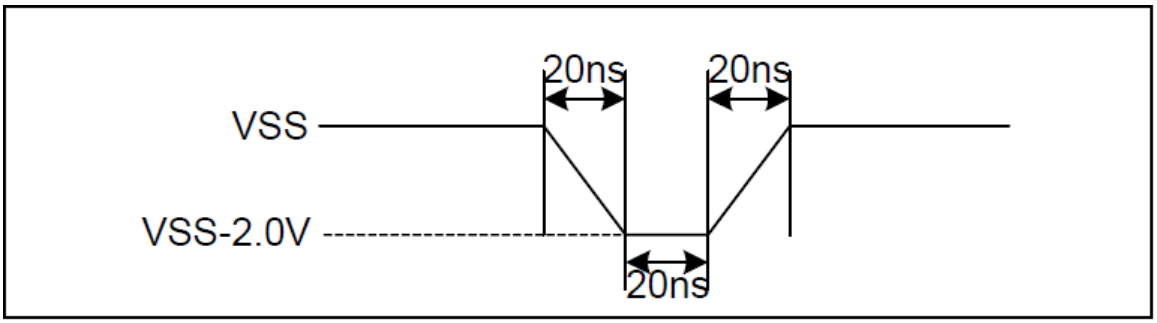
Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

Capacitance Measurement Condition

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			6	pF	VIN=0V
C_{OUT}	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance	30			pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

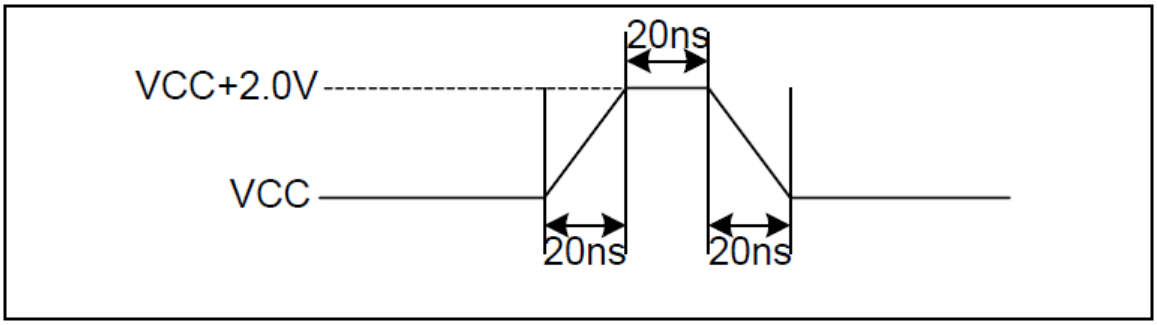


Figure27. Input Test Waveform and Measurement Level

DC Characteristics(T=-40℃~85℃,VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		0.03	0.05	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		0.03	0.05	μA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 40MHZ,Q=Open(*1 I/O)		5	7	mA
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1 I/O)		6	8	
		CLK=0.1VCC/0.9VCC at 120MHZ,Q=Open(*1 I/O)		8	12	
		CLK=0.1VCC/0.9VCC at 40MHZ,Q=Open(*2 I/O)		5	8	
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*2 I/O)		6	9	
		CLK=0.1VCC/0.9VCC at 120MHZ,Q=Open(*2 I/O)		10	15	
I_{CC4}	Operating Current(PP)	CS#=VCC		10	20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC		10	20	mA
I_{CC6}	Operating Current(SE)	CS#=VCC		10	20	mA
I_{CC7}	Operating Current(BE)	CS#=VCC		10	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

AC Characteristics(T=-40℃~85℃,VCC=2.7~3.6V，C_L=30pf)

Symbol	Parameter	Min.	Typ	Max.	Unit
fC	Serial Clock Frequency For:Fast Read(0BH),Dual Output(3BH)	DC		120	MHz
fC1	Serial Clock Frequency For:Dual I/O(BBH),Quad I/O(EBH),Quad Output(6BH)	DC		80	MHz
fR	Serial Clock Frequency For:Read(03H)	DC		40	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time(read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tCLQV	Clock Low To Output Valid			6.5	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			0.1	us
tRES1	CS# High To Standby Mode Without Electronic Signature Read			0.5	us
tRES2	CS# High To Standby Mode With Electronic Signature Read			0.5	us
tW	Write Status Register Cycle Time		10	150	ms
tPP	Page Programming Time		1.0	3.0	ms
tBP	Byte Program Time		3		us
tSE	Sector Erase Time		60	250	ms
tBE	Block Erase Time(32K Bytes)		0.3	1.0	s
tBE	Block Erase Time(64K Bytes)		0.45	1.5	s
tCE	Chip Erase Time(4M)		3.2	10.0	s

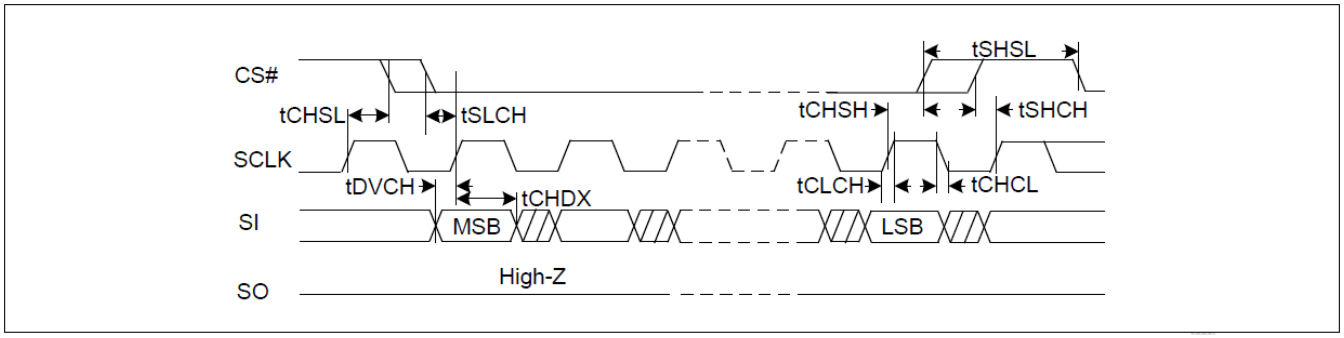


Figure28. Serial Input Timing

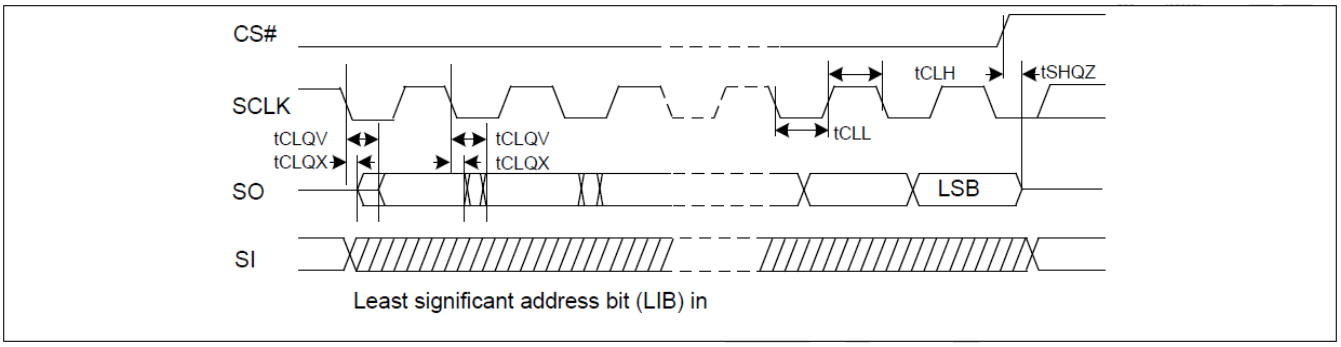
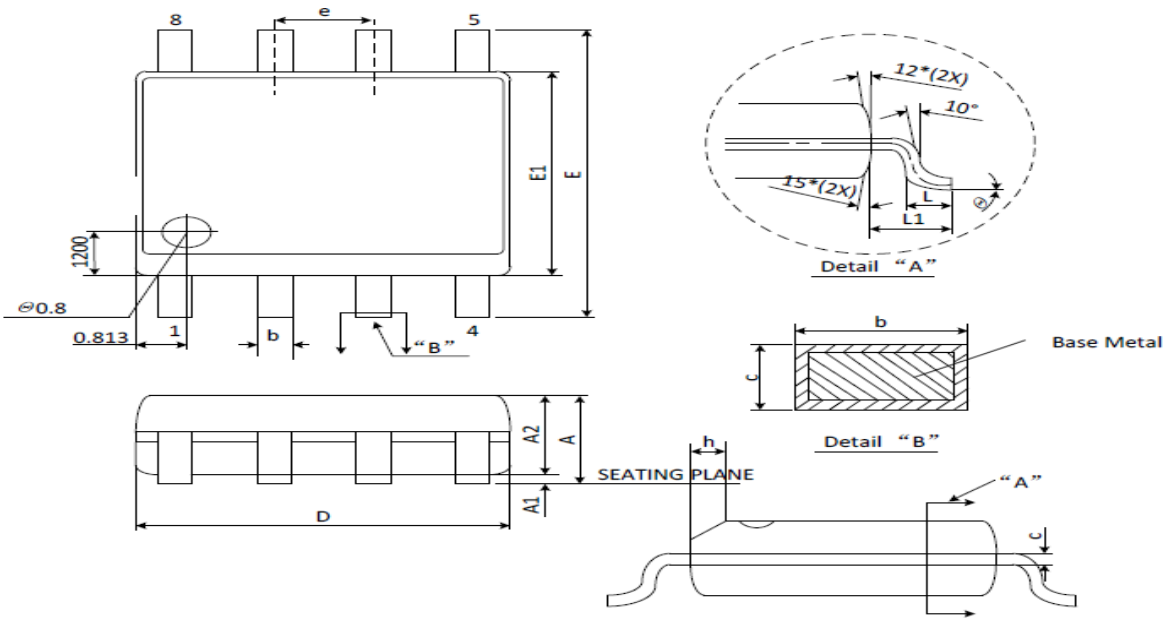


Figure29. Output Timing

Packaging information

SOP-8



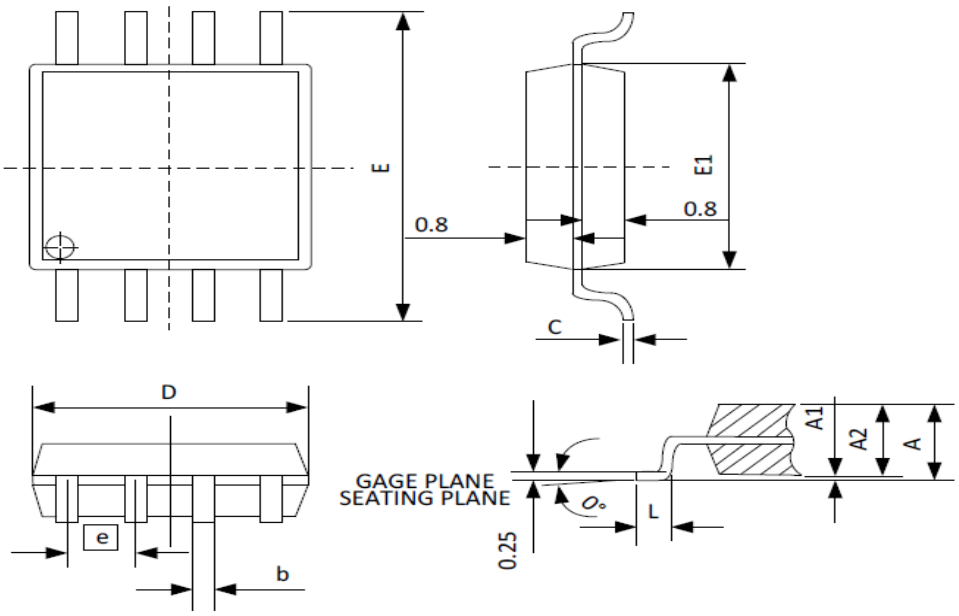
Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.300		1.500
b	0.330		0.510
c	0.190		0.250
D	4.700	4.900	5.000
E1	3.800	3.900	4.000
e		1.270	
E	5.800	6.000	6.200
h	0.250	0.350	0.500
L	0.508	0.635	0.762
L1	0.837	1.040	1.243
θ	0°		8°

Note:

1. Coplanarity: 0.1mm
2. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.
3. All dimensions follow JEDEC MS-012 standard.

Packaging information

SOP-8L (208mil)



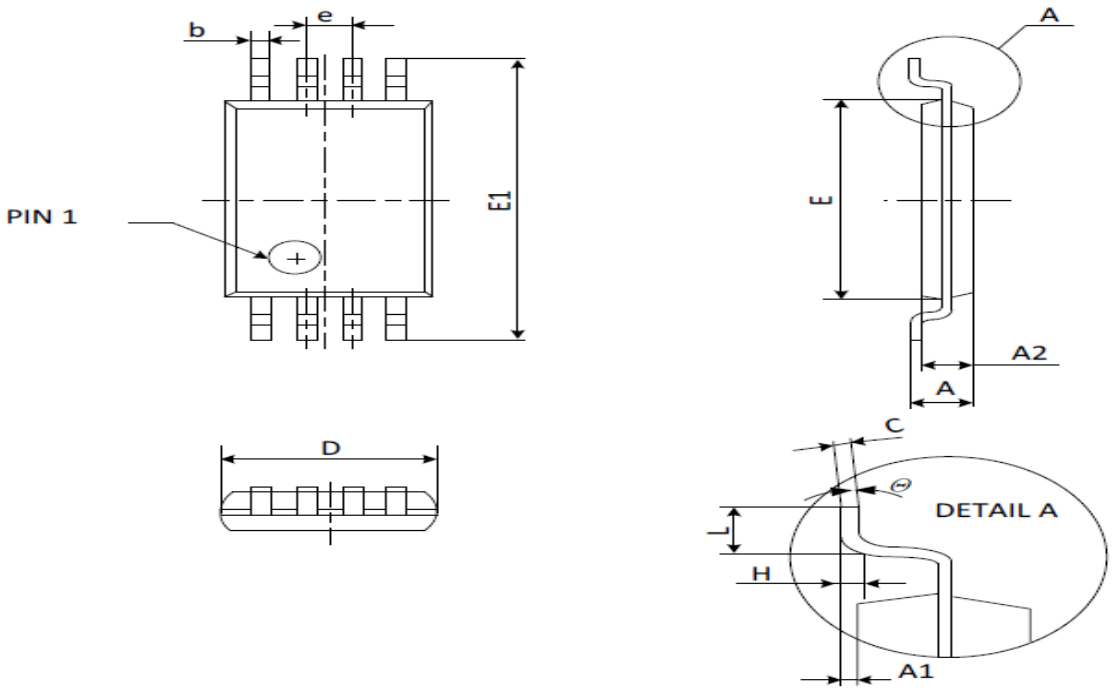
Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	1.750	1.950	2.160
A1	0.050	0.150	0.250
A2	1.700	1.800	1.910
b	0.350	0.420	0.480
c	0.190	0.200	0.250
D	5.130	5.230	5.330
E	7.700	7.900	8.100
E1	5.180	5.280	5.380
e	1.270 BSC		
L	0.500	0.650	0.800
θ	0°		8°

Note:

1. JEDEC Outline : N/A
2. Coplanarity: 0.1mm
3. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.

Packaging information

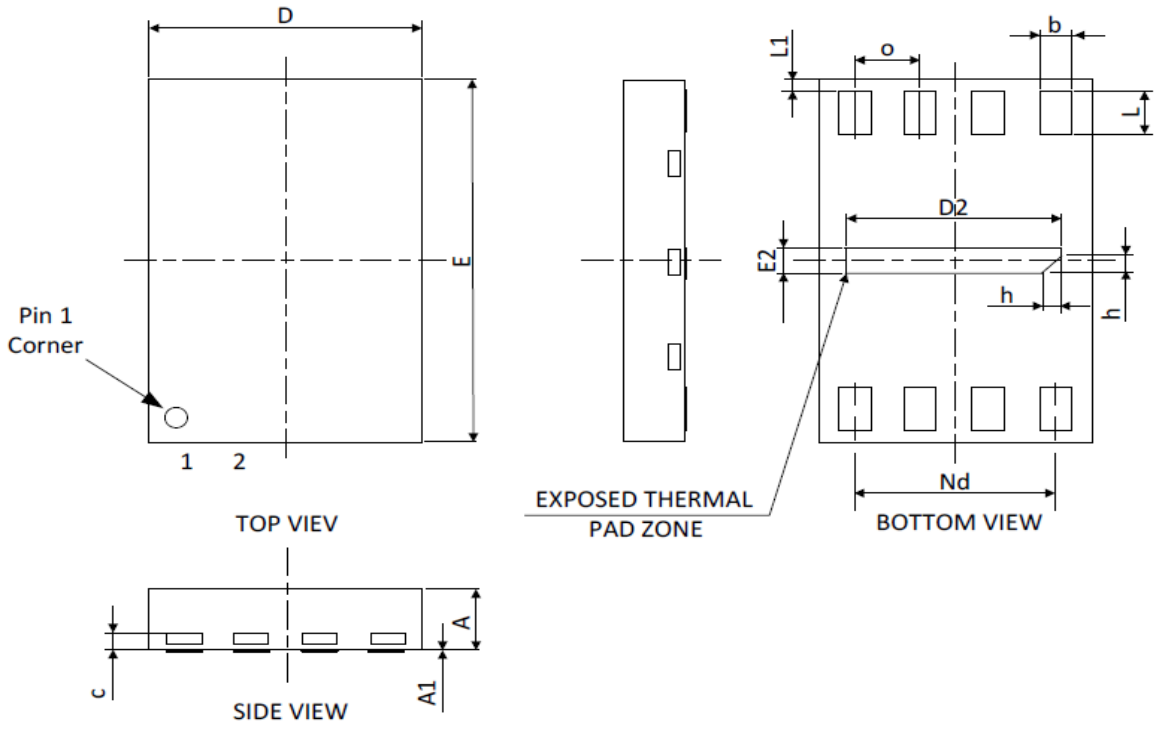
TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Packaging information

USON3*2-8



Symbol	Dimensions In Millimeters		
	Min	Norm	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
b	0.180	0.250	0.030
c	0.100	0.150	0.200
D	1.900	2.000	2.100
D2	1.500	1.600	1.700
e	0.500BSC		
Nd	1.500BSC		
E	2.900	3.000	3.100
E2	0.100	0.200	0.300
L	0.300	0.350	0.400
L1	0.050	0.100	0.150
h	0.05	0.15	0.25

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.