12-Bit, 160 MSPS, 2×/4×/8× Interpolating Dual TxDAC D/A Converter

AD9773

FEATURES

- 12-bit resolution, 160 MSPS/400 MSPS input/output data rate
- Selectable 2×/4×/8× interpolating filter
- Programmable channel gain and offset adjustment
- $f_S/2$, $f_S/4$, $f_S/8$ digital quadrature modulation capability
- Direct IF transmission mode for 70 MHz + IFs
- Enables image rejection architecture
- Fully compatible SPI port
- Excellent ac performance
  - SFDR −69 dBc @ 2 MHz to 35 MHz
  - WCDMA ACPR −69 dB @ IF = 19.2 MHz
- Internal PLL clock multiplier
- Selectable internal clock divider
- Versatile clock input
  - Differential/single-ended sine wave or TTL/CMOS/LVPECL compatible
- Versatile input data interface
  - Twos complement/straight binary data coding
  - Dual-port or single-port interleaved input data
- Single 3.3 V supply operation
- Power dissipation: typical 1.2 W @ 3.3 V
- On-chip 1.2 V reference
- 80-lead thin quad flat package, exposed pad (TQFP_EP)

APPLICATIONS

- Communications
  - Analog quadrature modulation architecture
  - 3G, multicarrier GSM, TDMA, CDMA systems
  - Broadband wireless, point-to-point microwave radios
  - Instrumentation/ATE

FUNCTIONAL BLOCK DIAGRAM

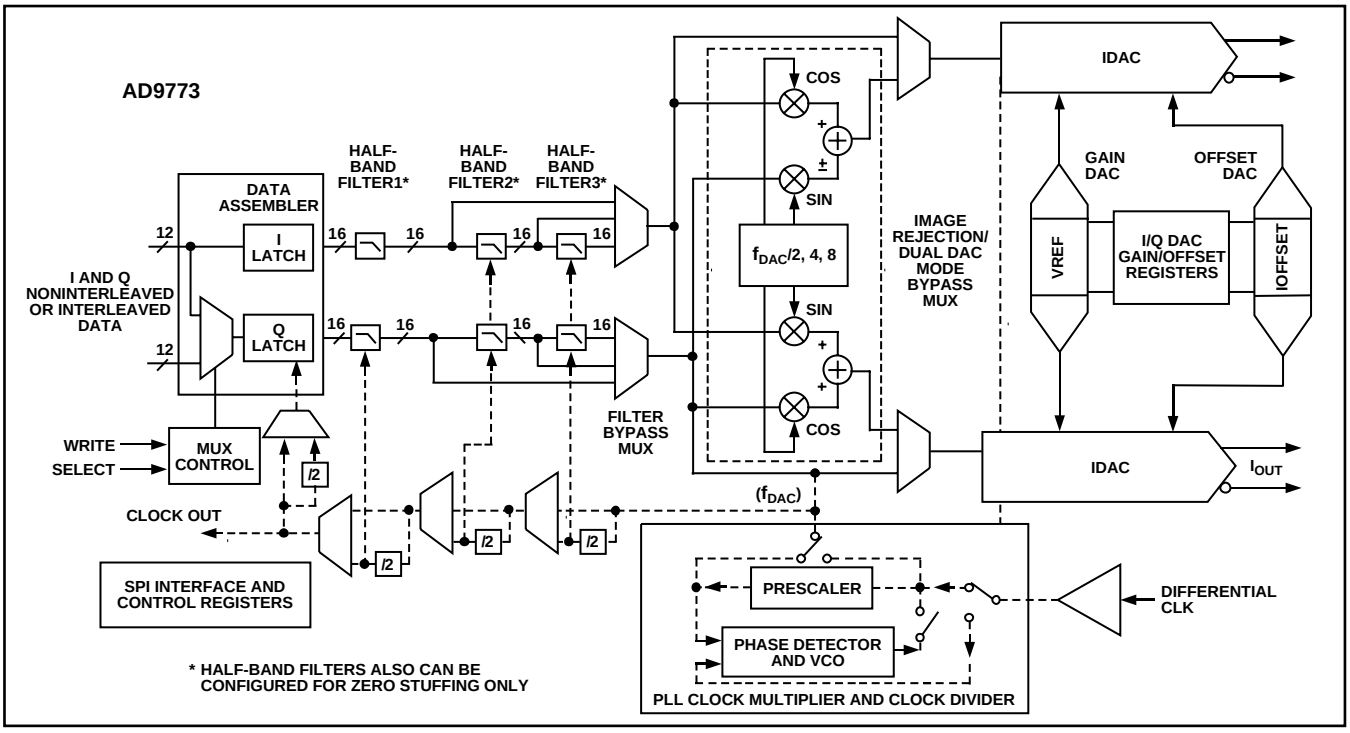


Figure 1.

Rev. D

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GENERAL DESCRIPTION

The AD9773[1] is the 12-bit member of the AD977x pin-compatible, high performance, programmable 2×/4×/8× interpolating TxDAC+® family. The AD977x family features a serial port interface (SPI) that provides a high level of programmability, thus allowing for enhanced system-level options. These options include selectable 2×/4×/8× interpolation filters; $f_S/2$, $f_S/4$, or $f_S/8$ digital quadrature modulation with image rejection; a direct IF mode; programmable channel gain and offset control; programmable internal clock divider; straight binary or twos complement data interface; and a single-port or dual-port data interface.

The selectable 2×/4×/8× interpolation filters simplify the requirements of the reconstruction filters while simultaneously enhancing the TxDAC+ family's pass-band noise/distortion performance. The independent channel gain and offset adjust registers allow the user to calibrate LO feedthrough and sideband suppression errors associated with analog quadrature modulators. The 6 dB of gain adjustment range can also be used to control the output power level of each DAC.

The AD9773 features the ability to perform $f_S/2$, $f_S/4$, and $f_S/8$ digital modulation and image rejection when combined with an analog quadrature modulator. In this mode, the AD9773 accepts I and Q complex data (representing a single or multi-carrier waveform), generates a quadrature modulated IF signal along with its orthogonal representation via its dual DACs, and presents these two reconstructed orthogonal IF carriers to an analog quadrature modulator to complete the image rejection upconversion process. Another digital modulation mode (for example, the direct IF mode) allows the original baseband signal representation to be frequency translated such that pairs of images fall at multiples of one-half the DAC update rate.

The AD977x family includes a flexible clock interface accepting differential or single-ended sine wave or digital logic inputs. An internal PLL clock multiplier is included and generates the necessary on-chip high frequency clocks. It can also be disabled to allow the use of a higher performance external clock source. An internal programmable divider simplifies clock generation in the converter when using an external clock source. A flexible data input interface allows for straight binary or twos complement formats and supports single-port interleaved or dual-port data.

[1] Protected by U.S. Patent Numbers 5,568,145; 5,689,257; and 5,703,519. Other patents pending.

Dual high performance DAC outputs provide a differential current output programmable over a 2 mA to 20 mA range. The AD9773 is manufactured on an advanced 0.35 micron CMOS process, operates from a single supply of 3.1 V to 3.5 V, and consumes 1.2 W of power.

Targeted at a wide dynamic range, multicarrier, and multi-standard systems, the superb baseband performance of the AD9773 is ideal for wide band CDMA, multicarrier CDMA, multicarrier TDMA, multicarrier GSM, and high performance systems employing high order QAM modulation schemes. The image rejection feature simplifies and can help to reduce the number of signal band filters needed in a transmit signal chain. The direct IF mode helps to eliminate a costly mixer stage for a variety of communications systems.

PRODUCT HIGHLIGHTS

1. The AD9773 is the 12-bit member of the AD977x pin compatible, high performance, programmable 2×/4×/8× interpolating TxDAC+ family.
2. Direct IF transmission is possible for 70 MHz + IFs through a novel digital mixing process.
3. $f_S/2$, $f_S/4$, and $f_S/8$ digital quadrature modulation and user selectable image rejection simplify/remove cascaded SAW filter stages.
4. A 2×/4×/8× user selectable interpolating filter eases data rate and output signal reconstruction filter requirements.
5. User selectable twos complement/straight binary data coding.
6. User programmable channel gain control over 1 dB range in 0.01 dB increments.
7. User programmable channel offset control ±10% over the FSR.
8. Ultrahigh speed 400 MSPS DAC conversion rate.
9. Internal clock divider provides data rate clock for easy interfacing.
10. Flexible clock input with single-ended or differential input, CMOS, or 1 V p-p LO sine wave input capability.
11. Low power: Complete CMOS DAC operates on 1.2 W from a 3.1 V to 3.5 V single supply. The 20 mA full-scale current can be reduced for lower power operation, and several sleep functions reduce power during idle periods.
12. On-chip voltage reference: The AD9773 includes a 1.20 V temperature compensated band gap voltage reference.
13. 80-lead thin quad flat package, exposed pad (TQFP_EP).

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	12			Bits
DC Accuracy[1]				
Integral Nonlinearity	−1.5	±0.4	+1.5	LSB
Differential Nonlinearity	−1	±0.2	+1	LSB
Monotonicity	Guaranteed over specified temperature range			
ANALOG OUTPUT (for IR and 2R Gain Setting Modes)				
Offset Error	−0.02	±0.01	+0.02	% of FSR
Gain Error (with Internal Reference)	−1.0		+1.0	% of FSR
Gain Matching	−1.0	±0.1	+1.0	% of FSR
Full-Scale Output Current[2]	2		20	mA
Output Compliance Range	−1.0		+1.25	V
Output Resistance		200		kΩ
Output Capacitance		3		pF
Gain, Offset Cal DACs, Monotonicity Guaranteed				
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		7		kΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (With Internal Reference)		50		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
AVDD				
Voltage Range	3.1	3.3	3.5	V
Analog Supply Current (I_{AVDD})[4]		72.5	76	mA
I_{AVDD} in Sleep Mode		23.3	26	mA
CLKVDD				
Voltage Range	3.1	3.3	3.5	V
Clock Supply Current (I_{CLKVDD})[4]		8.5	10.0	mA
CLKVDD (PLL ON)				
Clock Supply Current (I_{CLKVDD})		23.5		mA
DVDD				
Voltage Range	3.1	3.3	3.5	V
Digital Supply Current (I_{DVDD})[4]		34	41	mA
Nominal Power Dissipation		380	410	mW
P_{DIS}[5]		1.75		W
P_{DIS} in PWDN		6.0		mW
Power Supply Rejection Ratio—AVDD		±0.4		% of FSR/V
OPERATING RANGE	−40		+85	°C

[1] Measured at I_{OUTA} driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3] Use an external amplifier to drive any external load.
[4] 100 MSPS f_{DAC} with f_{OUT} = 1 MHz, all supplies = 3.3 V, no interpolation, no modulation.
[5] 400 MSPS f_{DAC}, f_{DATA} = 50 MSPS, $f_S/2$ modulation, PLL enabled.

DYNAMIC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 0 V, I_{OUTFS} = 20 mA, interpolation = 2×, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum DAC Output Update Rate (f_{DAC})	400			MSPS
Output Settling Time (t_{ST}) (to 0.025%)		11		ns
Output Rise Time (10% to 90%)[1]		0.8		ns
Output Fall Time (10% to 90%)[1]		0.8		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA√Hz
AC LINEARITY—BASEBAND MODE				
Spurious-Free Dynamic Range (SFDR) to Nyquist (f_{OUT} = 0 dBFS)				
f_{DATA} = 100 MSPS, f_{OUT} = 1 MHz	70	84.5		dBc
f_{DATA} = 65 MSPS, f_{OUT} = 1 MHz		83		dBc
f_{DATA} = 65 MSPS, f_{OUT} = 15 MHz		79		dBc
f_{DATA} = 78 MSPS, f_{OUT} = 1 MHz		83		dBc
f_{DATA} = 78 MSPS, f_{OUT} = 15 MHz		77		dBc
f_{DATA} = 160 MSPS, f_{OUT} = 1 MHz		75		dBc
f_{DATA} = 160 MSPS, f_{OUT} = 15 MHz		77		dBc
Spurious-Free Dynamic Range Within a 1 MHz Window				
f_{OUT} = 0 dBFS, f_{DATA} = 100 MSPS, f_{OUT} = 1 MHz	72	92.6		dBc
Two-Tone Intermodulation (IMD) to Nyquist (f_{OUT1} = f_{OUT2} = −6 dBFS)				
f_{DATA} = 65 MSPS, f_{OUT1} = 10 MHz; f_{OUT2} = 11 MHz		80		dBc
f_{DATA} = 65 MSPS, f_{OUT1} = 20 MHz; f_{OUT2} = 21 MHz		75		dBc
f_{DATA} = 78 MSPS, f_{OUT1} = 10 MHz; f_{OUT2} = 11 MHz		80		dBc
f_{DATA} = 78 MSPS, f_{OUT1} = 20 MHz; f_{OUT2} = 21 MHz		75		dBc
f_{DATA} = 160 MSPS, f_{OUT1} = 10 MHz; f_{OUT2} = 11 MHz		80		dBc
f_{DATA} = 160 MSPS, f_{OUT1} = 20 MHz; f_{OUT2} = 21 MHz		75		dBc
Total Harmonic Distortion (THD)				
f_{DATA} = 100 MSPS, f_{OUT} = 1 MHz; 0 dBFS	−70	−82.4		dB
Signal-to-Noise Ratio (SNR)				
f_{DATA} = 78 MSPS, f_{OUT} = 5 MHz; 0 dBFS		70		dB
f_{DATA} = 160 MSPS, f_{OUT} = 5 MHz; 0 dBFS		69		dB
Adjacent Channel Power Ratio (ACPR)				
WCDMA with 3.84 MHz BW, 5 MHz Channel Spacing				
IF = Baseband, f_{DATA} = 76.8 MSPS		69		dBc
IF = 19.2 MHz, f_{DATA} = 76.8 MSPS		69		dBc
Four-Tone Intermodulation				
21 MHz, 22 MHz, 23 MHz, and 24 MHz at −12 dBFS (f_{DATA} = MSPS, Missing Center)		73		dBFS
AC LINEARITY—IF MODE				
Four-Tone Intermodulation at IF = 200 MHz				
201 MHz, 202 MHz, 203 MHz, and 204 MHz at −12 dBFS (f_{DATA} = 160 MSPS, f_{DAC} = 320 MHz)		69		dBFS

[1] Measured single-ended into 50 Ω load.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current	−10		+10	µA
Logic 0 Current	−10		+10	µA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
SERIAL CONTROL BUS				
Maximum SCLK Frequency (f_{SLCK})	15			MHz
Minimum Clock Pulse Width High (t_{PWH})	30			ns
Minimum Clock Pulse Width Low (t_{PWL})	30			ns
Maximum Clock Rise/Fall Time			1	ms
Minimum Data/Chip Select Setup Time (t_{DS})	25			ns
Minimum Data Hold Time (t_{DH})	0			ns
Maximum Data Valid Time (t_{DV})			30	ns
RESET Pulse Width	1.5			ns
Inputs (SDI, SDIO, SCLK, CSB)				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current	−10		+10	µA
Logic 0 Current	−10		+10	µA
Input Capacitance		5		pF
SDIO Output				
Logic 1 Voltage	DRVDD − 0.6			V
Logic 0 Voltage			0.4	V
Logic 1 Current	30	50		mA
Logic 0 Current	30	50		mA

DIGITAL FILTER SPECIFICATIONS

Table 4. Half-Band Filter No. 1 (43 Coefficients)

Tap	Coefficient
1, 43	8
2, 42	0
3, 41	−29
4, 40	0
5, 39	67
6, 38	0
7, 37	−134
8, 36	0
9, 35	244
10, 34	0
11, 33	−414
12, 32	0
13, 31	673
14, 30	0
15, 29	−1079
16, 28	0
17, 27	1772
18, 26	0
19, 25	−3280
20, 24	0
21, 23	10,364
22	16,384

Table 5. Half-Band Filter No. 2 (19 Coefficients)

Tap	Coefficient
1, 19	19
2, 18	0
3, 17	−120
4, 16	0
5, 15	438
6, 14	0
7, 13	−1288
8, 12	0
9, 11	5047
10	8192

Table 6. Half-Band Filter No. 3 (11 Coefficients)

Tap	Coefficient
1, 11	7
2, 10	0
3, 9	−53
4, 8	0
5, 7	302
6	512

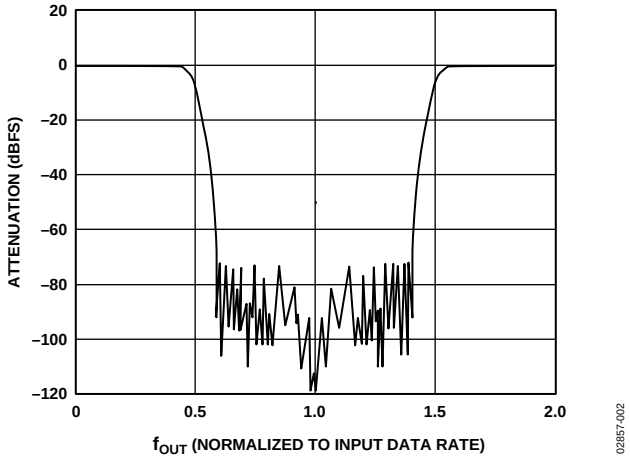


Figure 2. 2× Interpolating Filter Response

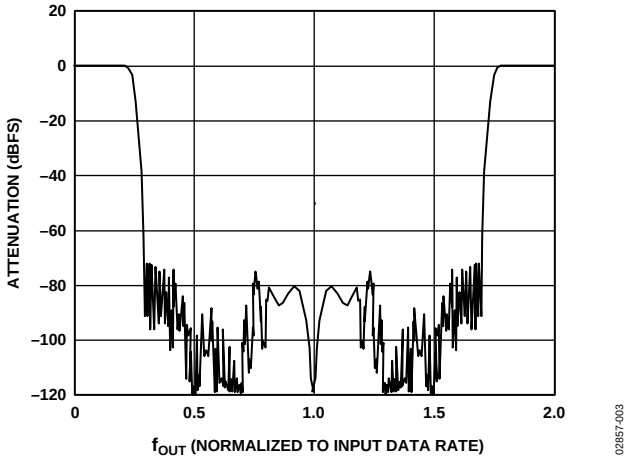


Figure 3. 4× Interpolating Filter Response

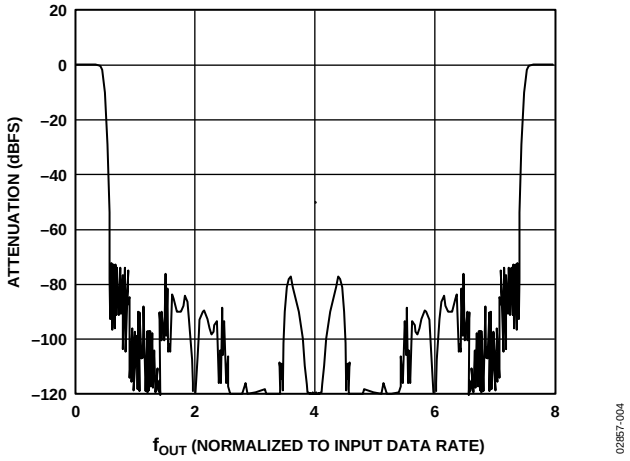


Figure 4. 8× Interpolating Filter Response

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	With Respect To	Min	Max	Unit
AVDD, DVDD, CLKVDD	AGND, DGND, CLKGND	−0.3	+4.0	V
AVDD, DVDD, CLKVDD	AVDD, DVDD, CLKVDD	−4.0	+4.0	V
AGND, DGND, CLKGND	AGND, DGND, CLKGND	−0.3	+0.3	V
REFIO, FSADJ1/FSADJ2	AGND	−0.3	AVDD + 0.3	V
I_{OUTA}, I_{OUTB}	AGND	−1.0	AVDD + 0.3	V
P1B11 to P1B0, P2B11 to P2B0, RESET	DGND	−0.3	DVDD + 0.3	V
DATACLK, PLL_LOCK	DGND	−0.3	DVDD + 0.3	V
CLK+, CLK−	CLKGND	−0.3	CLKVDD + 0.3	V
LPF	CLKGND	−0.3	CLKVDD + 0.3	V
SPI_CSB, SPI_CLK, SPI_SDIO, SPI_SDO	DGND	−0.3	DVDD + 0.3	V
Junction Temperature			125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

80-lead thin quad flat package, exposed pad (TQFP_EP)

θ_{JA} = 23.5°C/W (with thermal pad soldered to PCB)

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

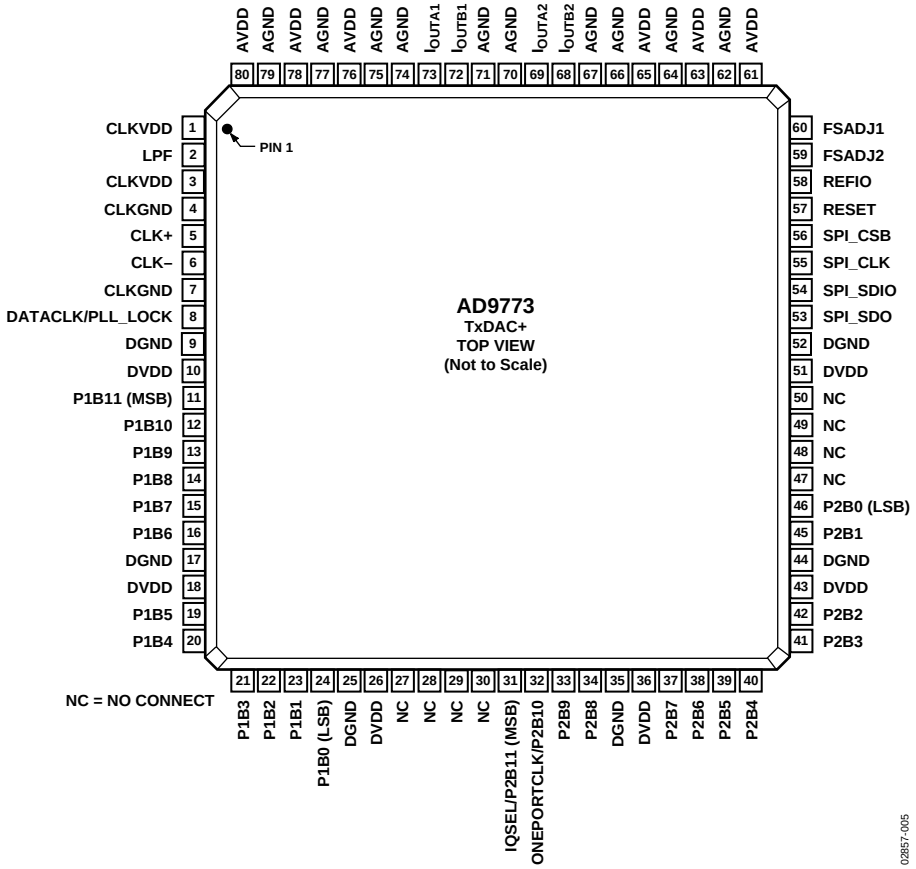


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3	CLKVDD	Clock Supply Voltage.
2	LPF	PLL Loop Filter.
4, 7	CLKGND	Clock Supply Common.
5	CLK+	Differential Clock Input.
6	CLK−	Differential Clock Input.
8	DATACLK/PLL_LOCK	With the PLL enabled, this pin indicates the state of the PLL. A read of a Logic 1 indicates the PLL is in the locked state. Logic 0 indicates the PLL has not achieved lock. This pin can also be programmed to act as either an input or output (Address 02h, Bit 3) DATACLK signal running at the input data rate.
9, 17, 25, 35, 44, 52	DGND	Digital Common.
10, 18, 26, 36, 43, 51	DVDD	Digital Supply Voltage.
11 to 16, 19 to 24,	P1B11 (MSB) to P1B0 (LSB)	Port 1 Data Inputs.
27 to 30, 47 to 50	NC	No Connect.
31	IQSEL/P2B11 (MSB)	In one-port mode, IQSEL = 1 followed by a rising edge of the differential input clock latches the data into the I channel input register. IQSEL = 0 latches the data into the Q channel input register. In two-port mode, this pin becomes the Port 2 MSB.
32	ONEPORTCLK/P2B10	With the PLL disabled and the AD9773 in one-port mode, this pin becomes a clock output that runs at twice the input data rate of the I and Q channels. This allows the AD9773 to accept and demux interleaved I and Q data to the I and Q input registers.
33, 34, 37 to 42, 45, 46	P2B9 to P2B0 (LSB)	Port 2 Data Inputs.
53	SPI_SDO	In the case where SDIO is an input, SDO acts as an output. When SDIO becomes an output, SDO enters a high-Z state. This pin can also be used as an output for the data rate clock. For more information, see the Two-Port Data Input Mode section.
54	SPI_SDIO	Bidirectional Data Pin. Data direction is controlled by Bit 7 of Register Address 00h. The default setting for this bit is 0, which sets SDIO as an input.
55	SPI_CLK	Data input to the SPI port is registered on the rising edge of SPI_CLK. Data output on the SPI port is registered on the falling edge.
56	SPI_CSB	Chip Select/SPI Data Synchronization. On momentary logic high, resets SPI port logic and initializes instruction cycle.
57	RESET	Logic 1 resets all of the SPI port registers, including Address 00h, to their default values. A software reset can also be done by writing a Logic 1 to SPI Register 00h, Bit 5. However, the software reset has no effect on the bits in Address 00h.
58	REFIO	Reference Output, 1.2 V Nominal.
59	FSADJ2	Full-Scale Current Adjust, Q Channel.
60	FSADJ1	Full-Scale Current Adjust, I Channel.
61, 63, 65, 76, 78, 80	AVDD	Analog Supply Voltage.
62, 64, 66, 67, 70, 71, 74, 75, 77, 79	AGND	Analog Common.
68, 69	I_{OUTB2}, I_{OUTA2}	Differential DAC Current Outputs, Q Channel.
72, 73	I_{OUTB1}, I_{OUTA1}	Differential DAC Current Outputs, I Channel.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, interpolation = 2×, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.

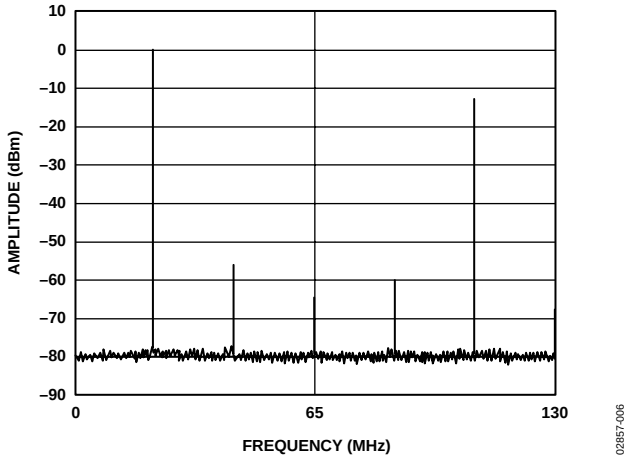


Figure 6. Single-Tone Spectrum @ f_{DATA} = 65 MSPS with f_{OUT} = f_{DATA}/3

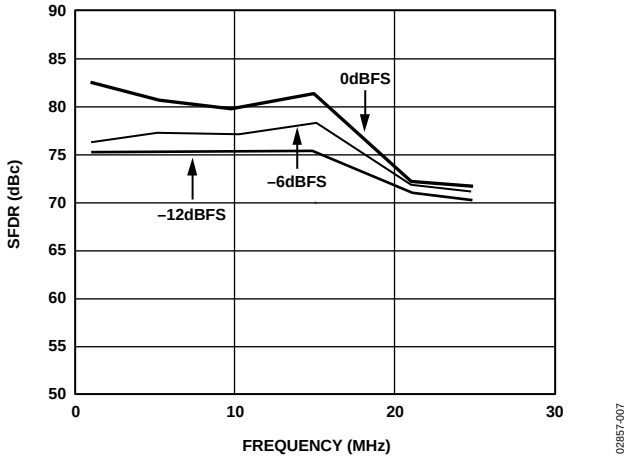


Figure 7. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS

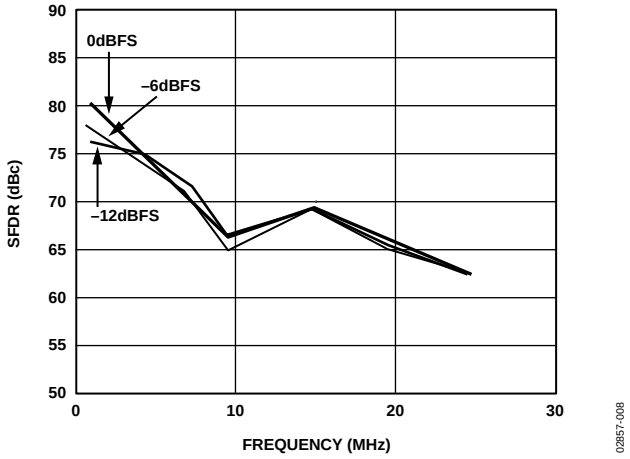


Figure 8. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS

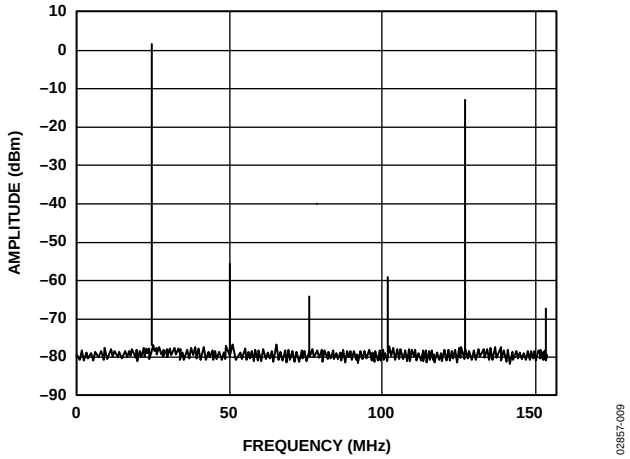


Figure 9. Single-Tone Spectrum @ f_{DATA} = 78 MSPS with f_{OUT} = f_{DATA}/3

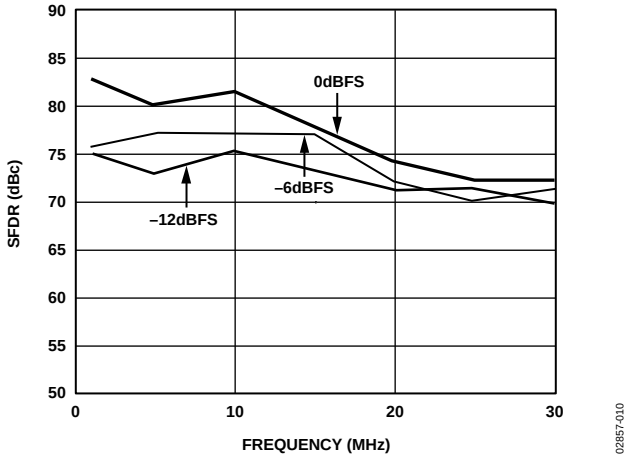


Figure 10. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS

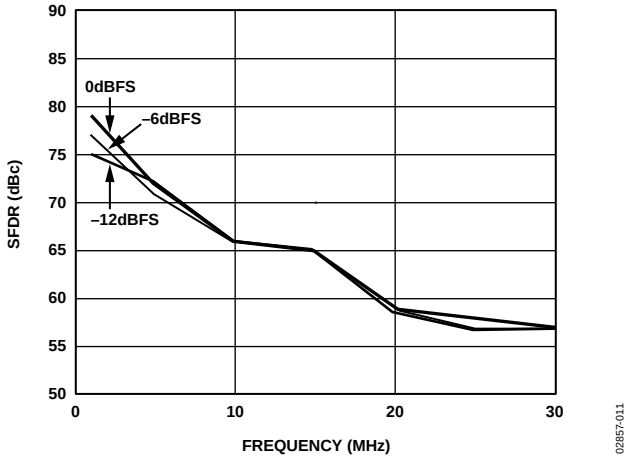


Figure 11. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS

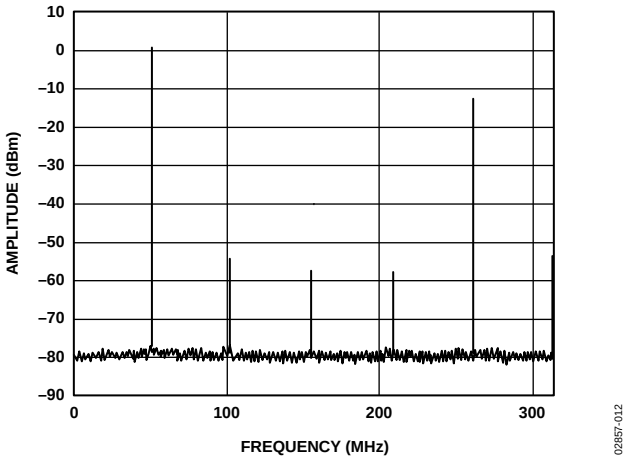


Figure 12. Single-Tone Spectrum @ f_{DATA} = 160 MSPS with $f_{OUT} = f_{DATA}/3$

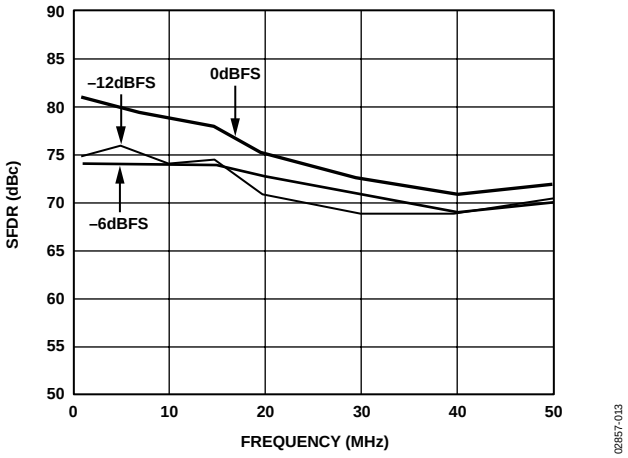


Figure 13. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS

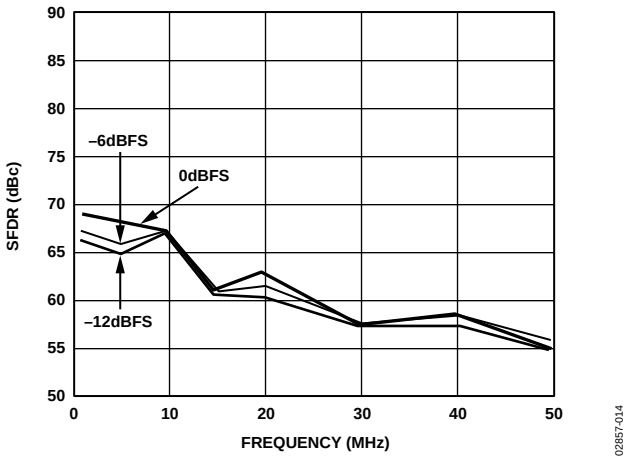


Figure 14. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS

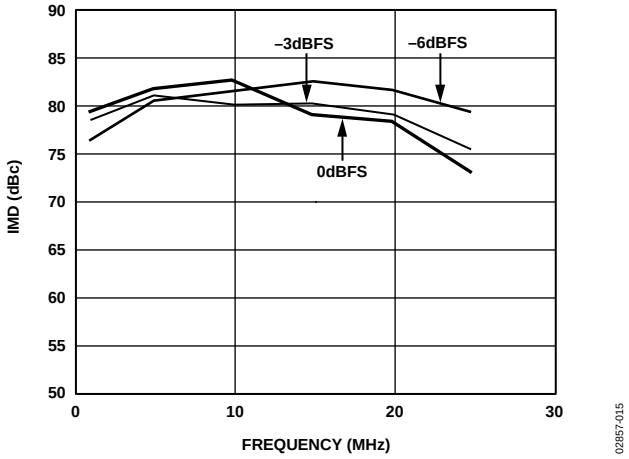


Figure 15. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 65 MSPS

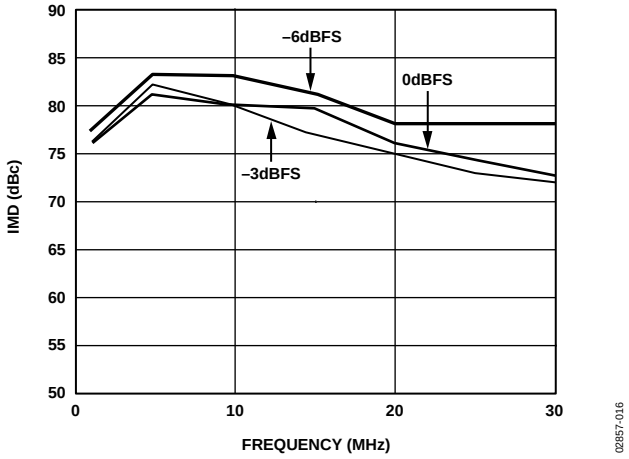


Figure 16. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 78 MSPS

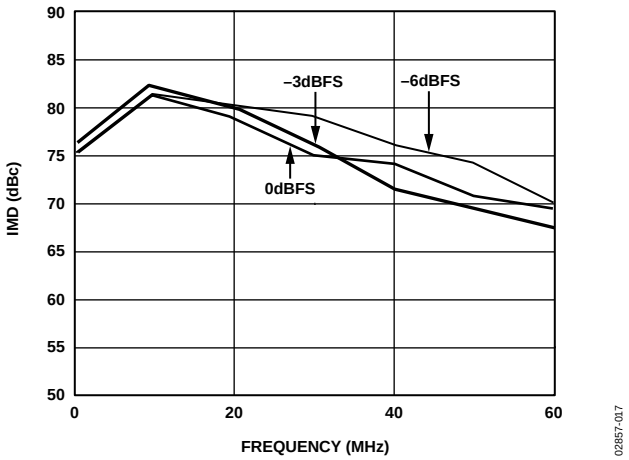


Figure 17. Third-Order IMD Products vs. f_{OUT} @ f_{DATA} = 160 MSPS

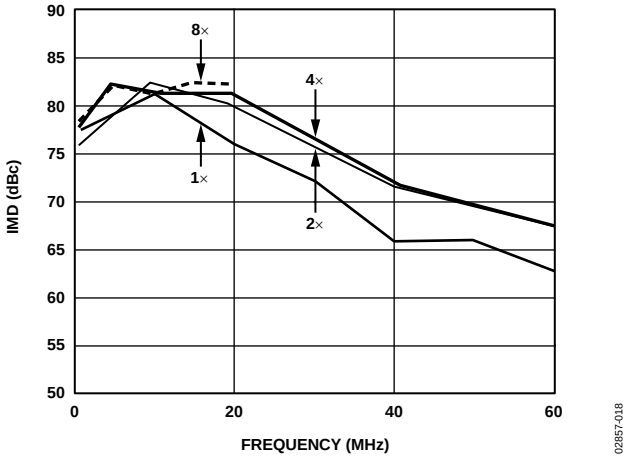


Figure 18. Third-Order IMD Products vs. f_{OUT} and Interpolation Rate, $1\times f_{DATA}$ = 160 MSPS, $2\times f_{DATA}$ = 160 MSPS, $4\times f_{DATA}$ = 80 MSPS, $8\times f_{DATA}$ = 50 MSPS

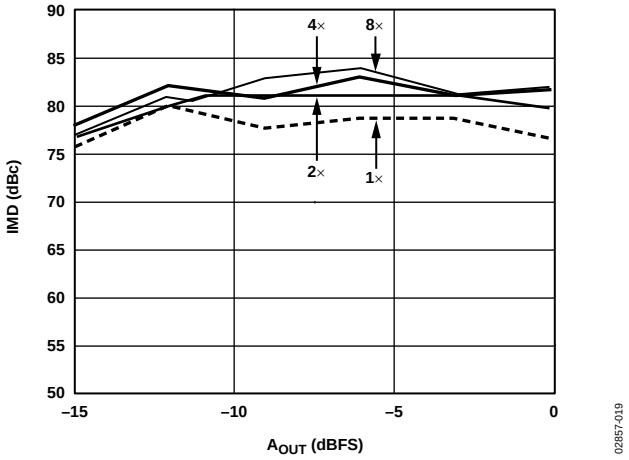


Figure 19. Third-Order IMD Products vs. A_{OUT} and Interpolation Rate, f_{DATA} = 50 MSPS for All Cases, $1\times f_{DAC}$ = 50 MSPS, $2\times f_{DAC}$ = 100 MSPS, $4\times f_{DAC}$ = 200 MSPS, $8\times f_{DAC}$ = 400 MSPS

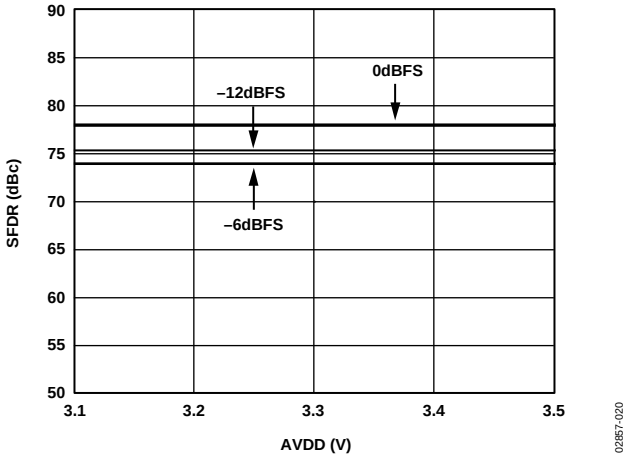


Figure 20. SFDR vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS, f_{DATA} = 160 MSPS

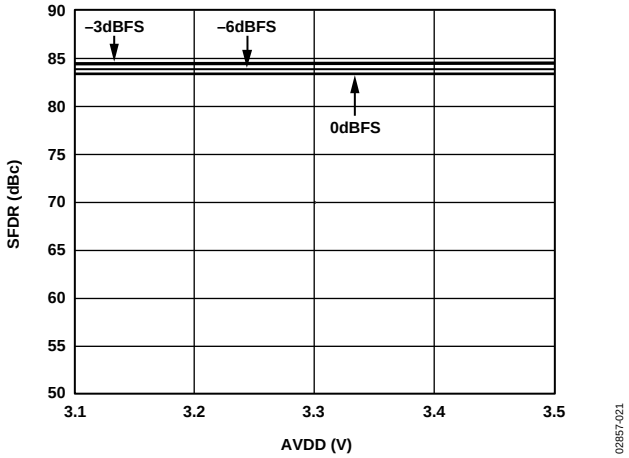


Figure 21. Third-Order IMD Products vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS, f_{DATA} = 160 MSPS

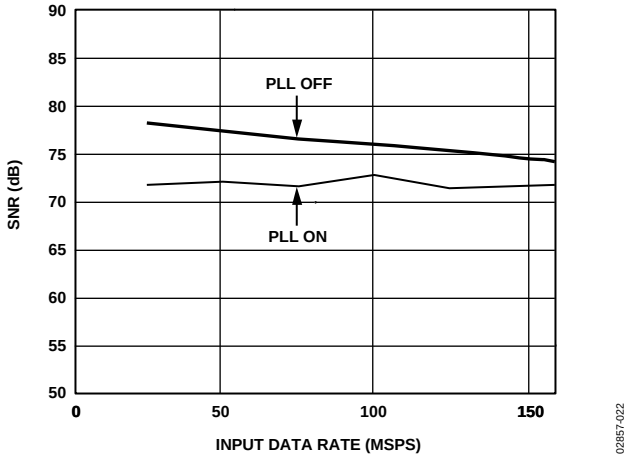


Figure 22. SNR vs. Data Rate for f_{OUT} = 5 MHz

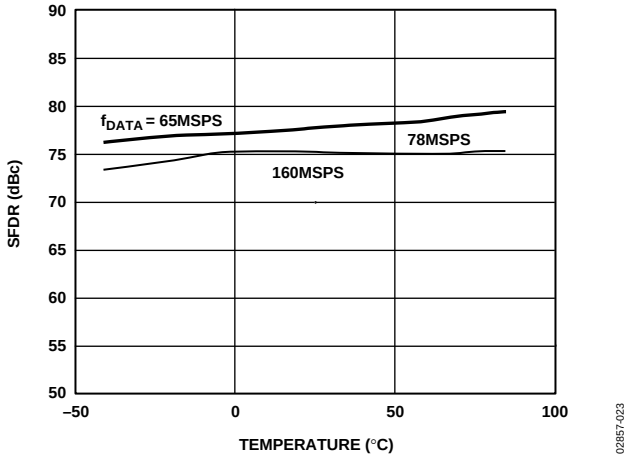


Figure 23. SFDR vs. Temperature @ $f_{OUT} = f_{DATA}/11$

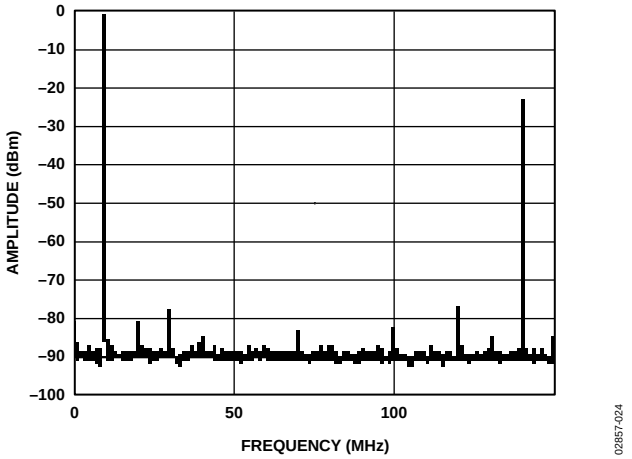


Figure 24. Single-Tone Spurious Performance, f_{OUT} = 10 MHz, f_{DATA} = 150 MSPS, No Interpolation

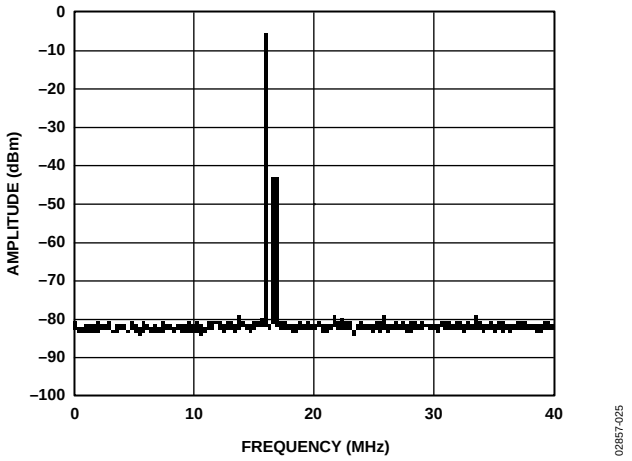


Figure 25. Two-Tone IMD Performance, f_{DATA} = 150 MSPS, No Interpolation

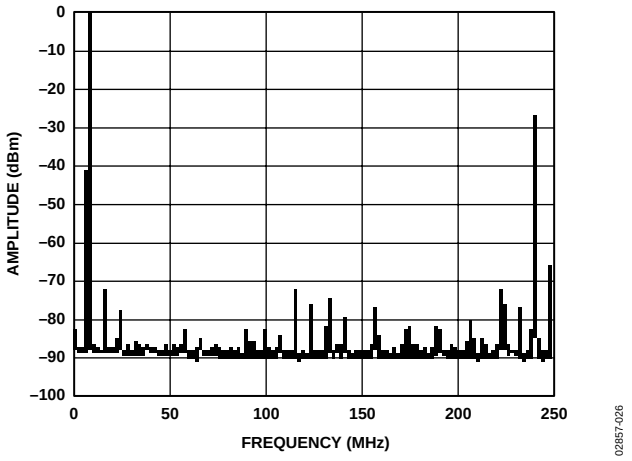


Figure 26. Single-Tone Spurious Performance, f_{OUT} = 10 MHz, f_{DATA} = 150 MSPS, Interpolation = 2×

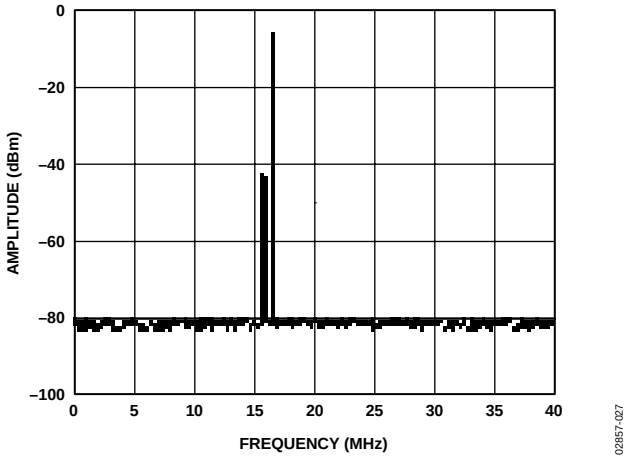


Figure 27. Two-Tone IMD Performance, f_{DATA} = 150 MSPS, Interpolation = 4×

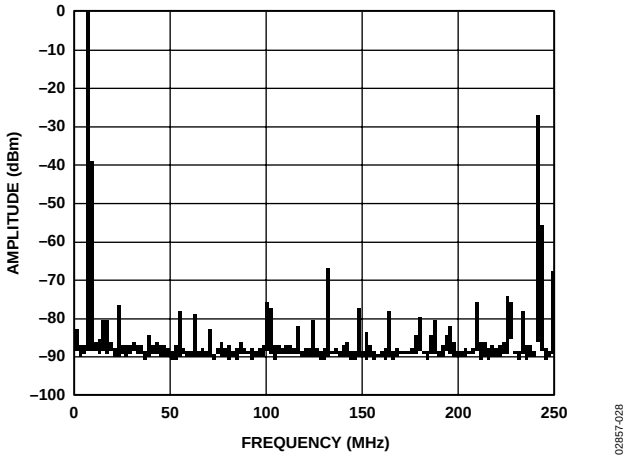


Figure 28. Single-Tone Spurious Performance, f_{OUT} = 10 MHz, f_{DATA} = 80 MSPS, Interpolation = 4×

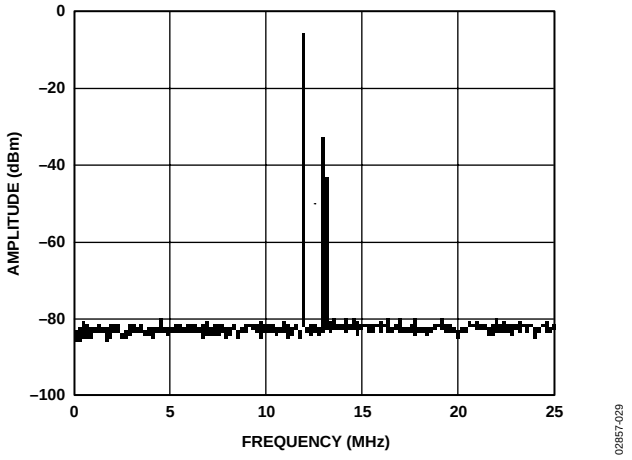


Figure 29. Two-Tone IMD Performance, f_{OUT} = 10 MHz, f_{DATA} = 50 MSPS, Interpolation = 8×

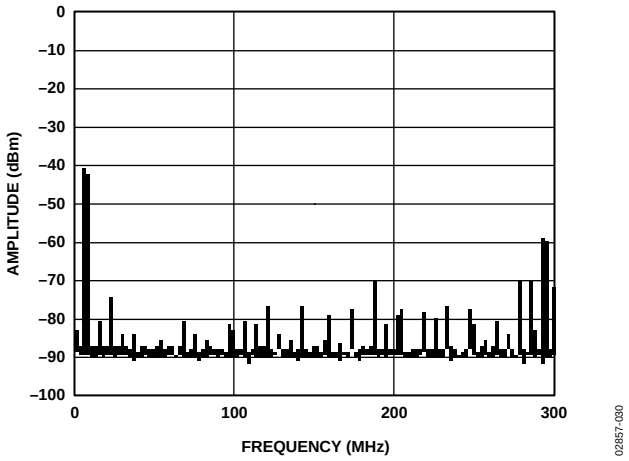


Figure 30. Single-Tone Spurious Performance, f_{OUT} = 10 MHz, f_{DATA} = 50 MSPS, Interpolation = 8×

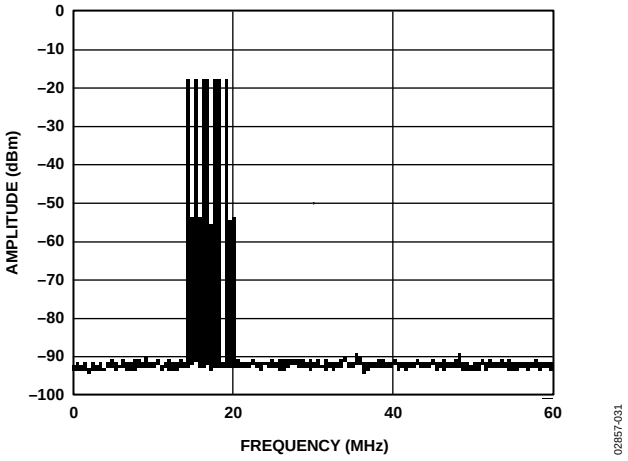


Figure 31. Eight-Tone IMD Performance, f_{DATA} = 160 MSPS, Interpolation = 8×

TERMINOLOGY

Adjacent Channel Power Ratio (ACPR)
A ratio, in dBc, between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images are redundant and have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Complex Modulation
The process of passing the real and imaginary components of a signal through a complex modulator (transfer function = $e^{j\omega t}$ = $\cos\omega t + j\sin\omega t$) and realizing real and imaginary components on the modulator output.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Group Delay
Number of input clocks between an impulse applied at the device input and the peak DAC output current. A half-band FIR filter has constant group delay over its entire frequency range.

Impulse Response
Response of the device to an impulse applied to the input.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed with a sharp transition band near $f_{DATA}/2$. Images that would typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Linearity Error
Also called integral nonlinearity (INL), linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from 0 to full scale.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of 0 is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Pass Band
Frequency band in which any input applied therein passes unattenuated to the DAC output.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Stop-Band Rejection
The amount of attenuation of a frequency outside the pass band applied to the DAC, relative to a full-scale signal applied at the DAC input within the pass band.

Temperature Drift
It is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

MODE CONTROL (VIA SPI PORT)

Table 9. Mode Control via SPI Port[1]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	SDIO Bidirectional **0 = Input** 1 = I/O	LSB, MSB First **0 = MSB** 1 = LSB	Software Reset on Logic 1	Sleep Mode Logic 1 Shuts Down the DAC Output Currents	Power-Down Mode Logic 1 Shuts Down All Digital and Analog Functions	1R/2R Mode DAC Output Current Set by One or Two External Resistors 0 = 2R, 1 = 1R	PLL_LOCK Indicator	
01h	Filter Interpolation Rate (1×, 2×, 4×, 8×)	Filter Interpolation Rate (1×, 2×, 4×, 8×)	Modulation Mode (**None**, $f_S/2$, $f_S/4$, $f_S/8$)	Modulation Mode (**None**, $f_S/2$, $f_S/4$, $f_S/8$)	**0 = No Zero Stuffing on Interpolation Filters**, Logic 1 Enables Zero Stuffing	**1 = Real Mix Mode** 0 = Complex Mix Mode	**0 = $e^{-j\omega t}$** 1 = $e^{+j\omega t}$	DATACLK/ PLL_LOCK[2] Select **0 = PLLLOCK** 1 = DATACLK
02h	**0 = Signed Input Data** 1 = Unsigned	**0 = Two-Port Mode** 1 = One-Port Mode	DATACLK Driver Strength	DATACLK Invert **0 = No Invert** 1 = Invert		ONEPORTCLK Invert **0 = No Invert** 1 = Invert	IQSEL Invert **0 = No Invert** 1 = Invert	Q First **0 = I First** 1 = Q First
03h	Data Rate[2] Output Clock						PLL Divide (Prescaler) Ratio	PLL Divide (Prescaler) Ratio
04h	**0 = PLL OFF**[2] 1 = PLL ON	**0 = Automatic Charge Pump Control** 1 = Programmable				PLL Charge Pump Control	PLL Charge Pump Control	PLL Charge Pump Control
05h	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment	IDAC Fine Gain Adjustment
06h					IDAC Coarse Gain Adjustment	IDAC Coarse Gain Adjustment	IDAC Coarse Gain Adjustment	IDAC Coarse Gain Adjustment
07h	IDAC Offset Adjustment Bit 9	IDAC Offset Adjustment Bit 8	IDAC Offset Adjustment Bit 7	IDAC Offset Adjustment Bit 6	IDAC Offset Adjustment Bit 5	IDAC Offset Adjustment Bit 4	IDAC Offset Adjustment Bit 3	IDAC Offset Adjustment Bit 2
08h	IDAC I_{OFFSET} Direction **0 = I_{OFFSET} on I_{OUTA}** 1 = I_{OFFSET} on I_{OUTB}						IDAC Offset Adjustment Bit 1	IDAC Offset Adjustment Bit 0
09h	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment	QDAC Fine Gain Adjustment

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah					QDAC Coarse Gain Adjustment	QDAC Coarse Gain Adjustment	QDAC Coarse Gain Adjustment	QDAC Coarse Gain Adjustment
0Bh	QDAC Offset Adjustment Bit 9	QDAC Offset Adjustment Bit 8	QDAC Offset Adjustment Bit 7	QDAC Offset Adjustment Bit 6	QDAC Offset Adjustment Bit 5	QDAC Offset Adjustment Bit 4	QDAC Offset Adjustment Bit 3	QDAC Offset Adjustment Bit 2
0Ch	QDAC I_{OFFSET} Direction **0 = I_{OFFSET} on I_{OUTA}** 1 = I_{OFFSET} on I_{OUTB}						QDAC Offset Adjustment Bit 1	QDAC Offset Adjustment Bit 0
0Dh					Version Register	Version Register	Version Register	Version Register

[1] Default values are shown in bold.
[2] See the Two-Port Data Input Mode section for more information.

REGISTER DESCRIPTION

Address 00h

Bit 7: Logic 0 (default) causes the SPI_SDIO pin to act as an input during the data transfer (Phase 2) of the communications cycle. When set to 1, SPI_SDIO can act as an input or output, depending on Bit 7 of the instruction byte.

Bit 6: Logic 0 (default) determines the direction (LSB/MSB first) of the communications and data transfer communications cycles. Refer to the MSB/LSB Transfers section for more details.

Bit 5: Writing a 1 to this bit resets the registers to their default values and restarts the chip. The RESET bit always reads back 0. Register Address 00h bits are not cleared by this software reset. However, a high level at the RESET pin forces all registers, including those in Address 00h, to their default state.

Bit 4: Sleep Mode. A Logic 1 to this bit shuts down the DAC output currents.

Bit 3: Power-Down Mode. Logic 1 shuts down all analog and digital functions except for the SPI port.

Bit 2: 1R/2R Mode. The default (0) places the AD9773 in two-resistor mode. In this mode, the I_{REF} currents for the I and Q DAC references are set separately by the R_{SET} resistors on FSADJ1 and FSADJ2 (Pin 59 and Pin 60). In 2R mode, assuming the coarse gain setting is full scale and the fine gain setting is zero, $I_{FULLSCALE1} = 32 \times V_{REF}/FSADJ1$ and $I_{FULLSCALE2} = 32 \times V_{REF}/FSADJ2$. With this bit set to 1, the reference currents for both I and Q DACs are controlled by a single resistor on Pin 60. $I_{FULLSCALE}$ in one-resistor mode for both I and Q DACs is half of what it would be in 2R mode, assuming all other conditions (R_{SET}, register settings) remain unchanged. The full-scale current of each DAC can still be set to 20 mA by choosing a resistor of half the value of the R_{SET} value used in 2R mode.

Bit 1: PLL_LOCK Indicator. When the PLL is enabled, reading this bit gives the status of the PLL. A Logic 1 indicates the PLL is locked. A Logic 0 indicates an unlocked state.

Address 01h

Bit 7 and Bit 6: This is the filter interpolation rate according to Table 10.

Table 10.

00	1×
01	2×
10	4×
11	8×

Bit 5 and Bit 4: This is the modulation mode according to Table 11.

Table 11.

00	none
01	$f_S/2$
10	$f_S/4$
11	$f_S/8$

Bit 3: Logic 1 enables zero stuffing mode for interpolation filters.

Bit 2: Default (1) enables the real mix mode. The I and Q data channels are individually modulated by $f_S/2$, $f_S/4$, or $f_S/8$ after the interpolation filters. However, no complex modulation is done. In the complex mix mode (Logic 0), the digital modulators on the I and Q data channels are coupled to create a digital complex modulator. When the AD9773 is applied in conjunction with an external quadrature modulator, rejection can be achieved of either the higher or lower frequency image around the second IF frequency (that is, the LO of the analog quadrature modulator external to the AD9773) according to the bit value of Register 01h, Bit 1.

Bit 1: Logic 0 (default) causes the complex modulation to be of the form $e^{-j\omega t}$, resulting in the rejection of the higher frequency image when the AD9773 is used with an external quadrature modulator. A Logic 1 causes the modulation to be of the form $e^{+j\omega t}$, which causes rejection of the lower frequency image.

Bit 0: In two-port mode, a Logic 0 (default) causes Pin 8 to act as a lock indicator for the internal PLL. A Logic 1 in this register causes Pin 8 to act as a DATACLK. For more information, see the Two-Port Data Input Mode section.

Address 02h

Bit 7: Logic 0 (default) causes data to be accepted on the inputs as twos complement. Logic 1 causes data to be accepted as straight binary.

Bit 6: Logic 0 (default) places the AD9773 in two-port mode. I and Q data enters the AD9773 via Port 1 and Port 2, respectively. A Logic 1 places the AD9773 in one-port mode in which interleaved I and Q data is applied to Port 1. See Table 8 for detailed information on the DATACLK/PLL_LOCK, IQSEL, and ONEPORTCLK modes.

Bit 5: DATACLK Driver Strength. With the internal PLL disabled and this bit set to Logic 0, it is recommended that DATACLK be buffered. When this bit is set to Logic 1, DATACLK acts as a stronger driver capable of driving small capacitive loads.

Bit 4: Logic 0 (default). A value of 1 inverts DATACLK at Pin 8.

Bit 2: Logic 0 (default). A value of 1 inverts ONEPORTCLK at Pin 32.

Bit 1: The Logic 0 (default) causes IQSEL = 0 to direct input data to the I channel, while IQSEL = 1 directs input data to the Q channel.

Bit 0: The Logic 0 (default) defines IQ pairing as IQ, IQ, ... while programming a Logic 1 causes the pair ordering to be QI, QI, ...

Address 03h

Bit 7: Allows the data rate clock (divided down from the DAC clock) to be output at either the DATACLK pin (Pin 8) or at the SPI_SDO pin (Pin 53). The default of 0 in this bit enables the data rate clock at DATACLK, while a 1 in this bit causes the data rate clock to be output at SPI_SDO. For more information, see the Two-Port Data Input Mode section.

Bit 1 and Bit 0: Setting this divide ratio to a higher number allows the VCO in the PLL to run at a high rate (for best performance), while the DAC input and output clocks run substantially slower. The divider ratio is set according to Table 12.

Table 12.

00	÷1
01	÷2
10	÷4
11	÷8

Address 04h

Bit 7: Logic 0 (default) disables the internal PLL. Logic 1 enables the PLL.

Bit 6: Logic 0 (default) sets the charge pump control to automatic. In this mode, the charge pump bias current is controlled by the divider ratio defined in Address 03h, Bits 1 and 0. Logic 1 allows the user to manually define the charge pump bias current using Address 04h, Bits 2, 1, and 0. Adjusting the charge pump bias current allows the user to optimize the noise/settling performance of the PLL.

Bit 2, Bit 1, and Bit 0: With the charge pump control set to manual, these bits define the charge pump bias current according to Table 13.

Table 13.

000	50 µA
001	100 µA
010	200 µA
011	400 µA
111	800 µA

Address 05h, 09h

Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0: These bits represent an 8-bit binary number (Bit 7 MSB) that defines the fine gain adjustment of the I (05h) and Q (09h) DAC according to Equation 1.

Address 06h, 0Ah

Bit 3, Bit 2, Bit 1, and Bit 0: These bits represent a 4-bit binary number (Bit 3 MSB) that defines the coarse gain adjustment of the I (06h) and Q (0Ah) DACs according to Equation 1.

Address 07h, 0Bh

Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0: These bits are used in conjunction with Address 08h, Address 0Ch, Bits [1:0].

Address 08h, 0Ch

Bit 1 and Bit 0: The 10 bits from these two address pairs (07h, 08h and 0Bh, 0Ch) represent a 10-bit binary number that defines the offset adjustment of the I and Q DACs according to Equation 1: (07h, 0Bh: Bit 7 MSB; 08h, 0Ch: Bit 0 LSB).

Address 08h, 0Ch

Bit 7: This bit determines the direction of the offset of the I (08h) and Q (0Ch) DACs. A Logic 0 applies a positive offset current to I_{OUTA}, while a Logic 1 applies a positive offset current to I_{OUTB}. The magnitude of the offset current is defined by the bits in Addresses 07h, 0Bh, 08h, and 0Ch according to Equation 1.

Equation 1 shows I_{OUTA} and I_{OUTB} as a function of fine gain, coarse gain, and offset adjustment when using 2R mode. In 1R mode, the current I_{REF} is created by a single FSADJ1 resistor (Pin 60). This current is divided equally into each channel so that a scaling factor of one-half must be added to these equations for full-scale currents for both DACs and the offset.

$$I_{OUTA} = \left[\left(\frac{6\times I_{REF}}{8}\right)\left(\frac{COARSE+1}{16}\right)-\left(\frac{3\times I_{REF}}{32}\right)\left(\frac{FINE}{256}\right)\right]\times\left[\left(\frac{1024}{24}\right)\left(\frac{DATA}{2^{12}}\right)\right](A)$$

$$I_{OUTB} = \left[\left(\frac{6\times I_{REF}}{8}\right)\left(\frac{COARSE+1}{16}\right)-\left(\frac{3\times I_{REF}}{32}\right)\left(\frac{FINE}{256}\right)\right]\times\left[\left(\frac{1024}{24}\right)\left(\frac{2^{12}-DATA-1}{2^{12}}\right)\right](A) \quad (1)$$

$$I_{OFFSET} = 4\times I_{REF}\left(\frac{OFFSET}{1024}\right)(A)$$

FUNCTIONAL DESCRIPTION

The AD9773 dual interpolating DAC consists of two data channels that can be operated completely independently or coupled to form a complex modulator in an image reject transmit architecture. Each channel includes three FIR filters, making the AD9773 capable of 2×, 4×, or 8× interpolation. High speed input and output data rates can be achieved within the limitations shown in Table 14.

Table 14.

Interpolation Rate (MSPS)	Input Data Rate (MSPS)	DAC Sample Rate (MSPS)
1×	160	160
2×	160	320
4×	100	400
8×	50	400

Both data channels contain a digital modulator capable of mixing the data stream with an LO of $f_{DAC}/2$, $f_{DAC}/4$, or $f_{DAC}/8$, where f_{DAC} is the output data rate of the DAC. A zero stuffing feature is also included and can be used to improve pass-band flatness for signals being attenuated by the SIN(x)/x characteristic of the DAC output. The speed of the AD9773, combined with its digital modulation capability, enables direct IF conversion architectures at 70 MHz and higher.

The digital modulators on the AD9773 can be coupled to form a complex modulator. By using this feature with an external analog quadrature modulator, such as Analog Devices' AD8345, an image rejection architecture can be enabled. To optimize the image rejection capability, as well as LO feedthrough in this architecture, the AD9773 offers programmable (via the SPI port) gain and offset adjust for each DAC.

Also included on the AD9773 are a phase-locked loop (PLL) clock multiplier and a 1.20 V band gap voltage reference. With the PLL enabled, a clock applied to the CLK+/CLK– inputs is frequency multiplied internally and generates all necessary internal synchronization clocks. Each 12-bit DAC provides two complementary current outputs whose full-scale currents can be determined either from a single external resistor or independently from two separate resistors (see the 1R/2R Mode section). The AD9773 features a low jitter, differential clock input that provides excellent noise rejection while accepting a sine or square wave input. Separate voltage supply inputs are provided for each functional block to ensure optimum noise and distortion performance.

Sleep and power-down modes can be used to turn off the DAC output current (sleep) or the entire digital and analog sections (power-down) of the chip. An SPI-compliant serial port is used to program the many features of the AD9773. Note that in power-down mode, the SPI port is the only section of the chip still active.

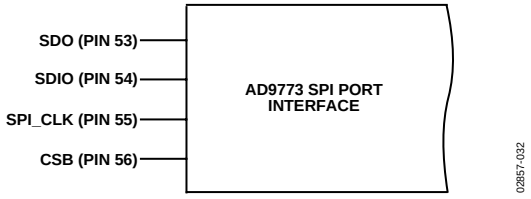


Figure 32. SPI Port Interface

SERIAL INTERFACE FOR REGISTER CONTROL

The AD9773 serial port is a flexible, synchronous serial communications port that allows an easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9773. Single- or multiple-byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9773's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for I/O (SDIO/SDO).

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9773. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9773 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9773 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9773.

A Logic 1 on the SPI_CSB pin, followed by a logic low, resets the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the middle of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9773 and the system controller. Phase 2 of the communication cycle is a transfer of one to four data bytes, as determined by the instruction byte. Normally, using one multibyte transfer is the preferred method. However, single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

INSTRUCTION BYTE

The instruction byte contains the information shown in Table 15.

Table 15.

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

R/W

Bit 7 of the instruction byte determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates read operation. Logic 0 indicates a write operation.

N1, N0

Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the following table.

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

A4, A3, A2, A1, and A0

Bits 4, 3, 2, 1, and 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9773.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SPI_CLK (Pin 55)—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9773 and to run the internal state machines. The SPI_CLK maximum frequency is 15 MHz. All data input to the AD9773 is registered on the rising edge of SPI_CLK. All data is driven out of the AD9773 on the falling edge of SPI_CLK.

SPI_CSB (Pin 56)—Chip Select

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines.

The SPI_SDO and SPI_SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SPI_SDIO (Pin 54)—Serial Data I/O

Data is always written into the AD9773 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of Register Address 00h. The default is Logic 0, which configures the SDIO pin as unidirectional.

SPI_SDO (Pin 53)—Serial Data Out

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9773 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The AD9773 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the first LSB bit in Register 0. The default is MSB first.

When this bit is set active high, the AD9773 serial port is in LSB first format. In LSB first mode, the instruction byte and data bytes must be written from LSB to MSB. In LSB first mode, the serial port internal byte address generator increments for each byte of the multibyte communication cycle.

When this bit is set default low, the AD9773 serial port is in MSB first format. In MSB first mode, the instruction byte and data bytes must be written from MSB to LSB. In MSB first mode, the serial port internal byte address generator decrements for each byte of the multibyte communication cycle.

When incrementing from 1Fh, the address generator changes to 00h. When decrementing from 00h, the address generator changes to 1Fh.

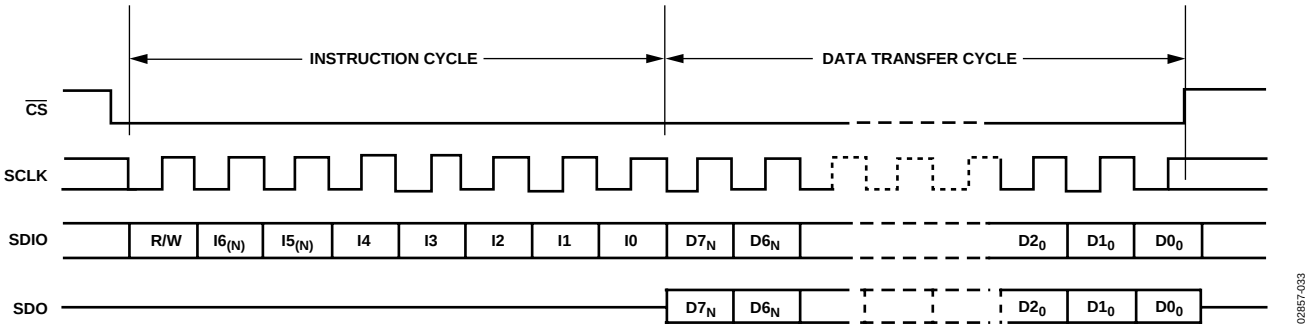


Figure 33. Serial Register Interface Timing MSB First

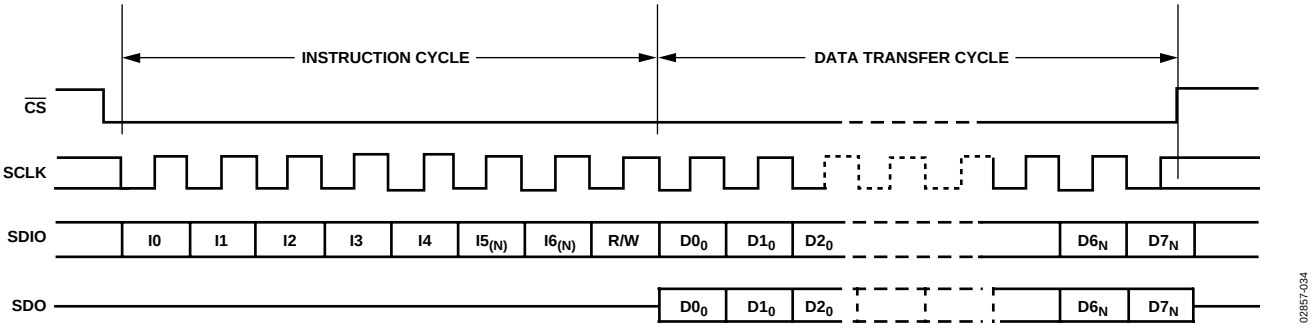


Figure 34. Serial Register Interface Timing LSB First

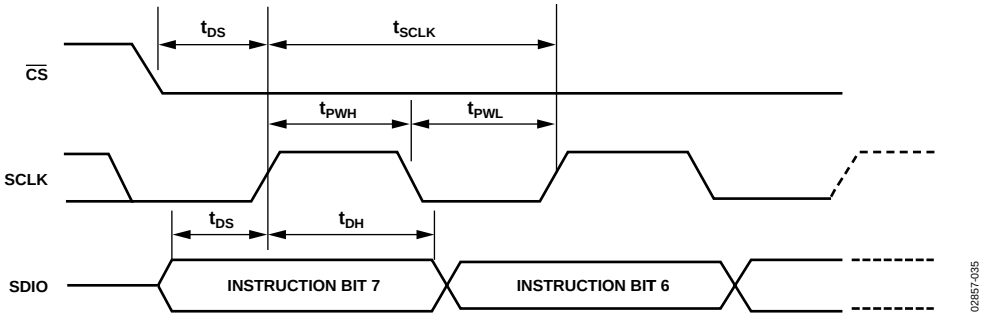


Figure 35. Timing Diagram for Register Write to AD9773

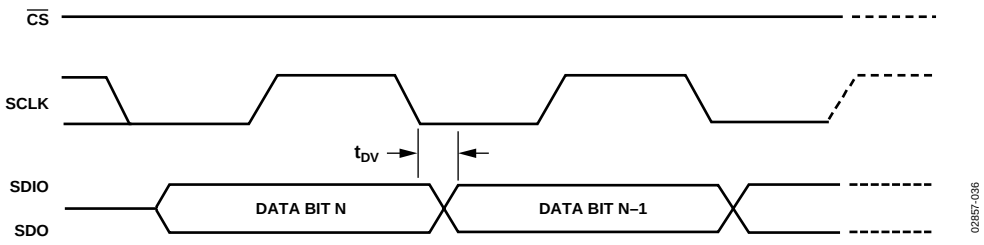


Figure 36. Timing Diagram for Register Read from AD9773

NOTES ON SERIAL PORT OPERATION

The AD9773 serial port configuration bits reside in Bits 6 and 7 of Register Address 00h. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register can occur during the middle of the communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the reset bit in Register Address 00h. All other registers are set to their default values, but the software reset does not affect the bits in Register Address 00h.

It is recommended to use only single-byte transfers when changing serial port configurations or initiating a software reset.

A write to Bit 1, Bit 2, and Bit 3 of Address 00h with the same logic levels as for Bit 7, Bit 6, and Bit 5 (bit pattern: XY1001YX binary) allows the user to reprogram a lost serial port configuration and to reset the registers to their default values. A second write to Address 00h with reset bit low and serial port configuration as previously specified (XY) reprograms the OSC IN multiplier setting. A changed f_{SYSCLK} frequency is stable after a maximum of 200 f_{MCLK} cycles (equals wake-up time).

DAC OPERATION

The dual 12-bit DAC output of the AD9773, along with the reference circuitry, gain, and offset registers, is shown in Figure 37 and Figure 38. Note that an external reference can be used by simply overdriving the internal reference with the external reference. Referring to the transfer functions in Equation 1, a reference current is set by the internal 1.2 V reference, the external R_{SET} resistor, and the values in the coarse gain register. The fine gain DAC subtracts a small amount from this and the result is input to IDAC and QDAC, where it is scaled by an amount equal to 1024/24. Figure 39 and Figure 40 show the scaling effect of the coarse and fine adjust DACs. IDAC and QDAC are PMOS current source arrays, segmented in a 5-4-3 configuration. The five most significant bits control an array of 31 current sources. The next four bits consist of 15 current sources whose values are all equal to 1/16 of an MSB current source. The three LSBs are binary weighted fractions of the middle bits' current sources. All current sources are switched to either I_{OUTA} or I_{OUTB}, depending on the input code.

The fine adjustment of the gain of each channel allows for improved balance of QAM modulated signals, resulting in improved modulation accuracy and image rejection. In the Interfacing the AD9773 with the AD8345 Quadrature Modulator section, the performance data shows to what degree image rejection can be improved when the AD9773 is used with an AD8345 quadrature modulator from Analog Devices Inc.

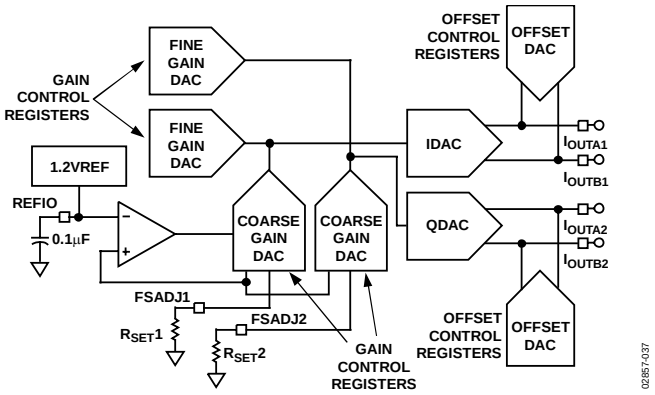


Figure 37. DAC Outputs, Reference Current Scaling, and Gain/Offset Adjust

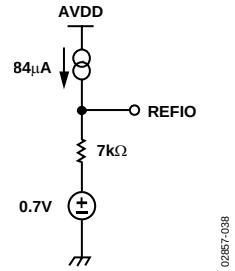


Figure 38. Internal Reference Equivalent Circuit

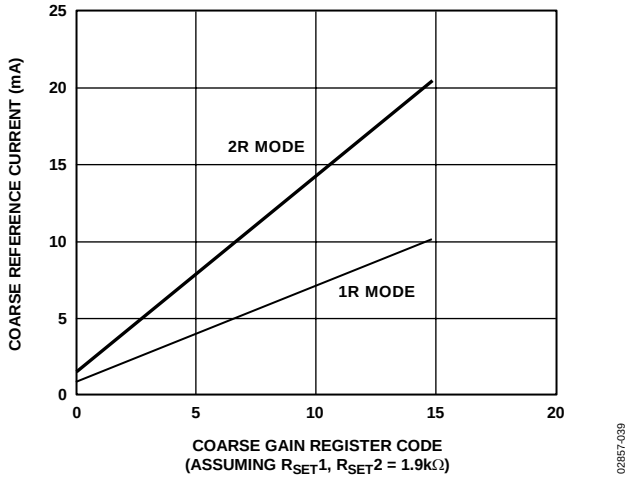


Figure 39. Coarse Gain Effect on $I_{FULLSCALE}$

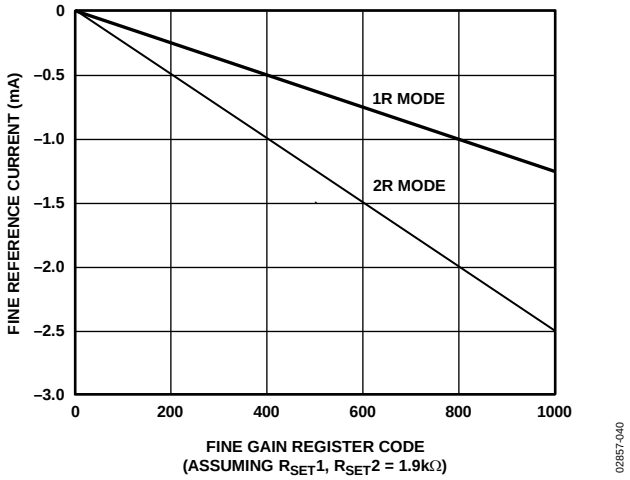


Figure 40. Fine Gain Effect on $I_{FULLSCALE}$

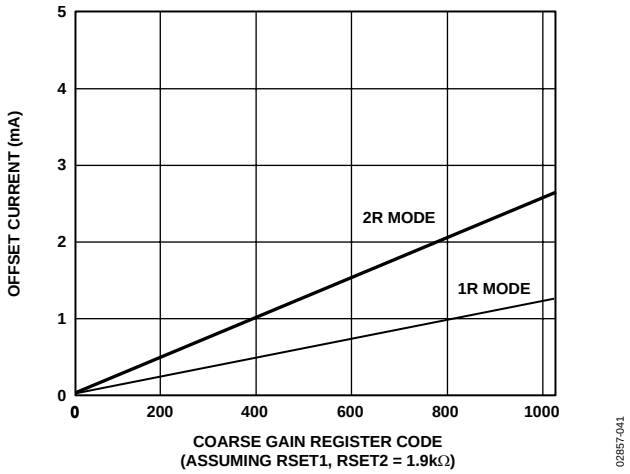


Figure 41. DAC Output Offset Current

The offset control defines a small current that can be added to I_{OUTA} or I_{OUTB} (not both) on the IDAC and QDAC. The selection in which I_{OUT} for this offset current is directed toward is programmable via Register 08h, Bit 7 (IDAC) and Register 0Ch, Bit 7 (QDAC). Figure 41 shows the scale of the offset current that can be added to one of the complementary outputs on the IDAC and QDAC. Offset control can be used for suppression of LO leakage resulting from modulation of dc signal components. If the AD9773 is dc-coupled to an external modulator, this feature can be used to cancel the output offset on the AD9773 as well as the input offset on the modulator. Figure 42 shows a typical example of the effect that the offset control has on LO suppression.

In Figure 42, the negative scale represents an offset added to I_{OUTB}, while the positive scale represents an offset added to I_{OUTA} of the respective DAC. Offset Register 1 corresponds to IDAC, while Offset Register 2 corresponds to QDAC. Figure 42 represents the AD9773 synthesizing a complex signal that is then dc-coupled to an AD8345 quadrature modulator with an LO of 800 MHz. The dc coupling allows the input offset of the AD8345 to be calibrated out as well. The LO suppression at the AD8345 output was optimized first by adjusting Offset Register 1 in the AD9773. When an optimal point was found (roughly Code 54), this code was held in Offset Register 1, and Offset Register 2 was adjusted. The resulting LO suppression is 70 dBFS. These are typical numbers, and the specific code for optimization varies from part to part.

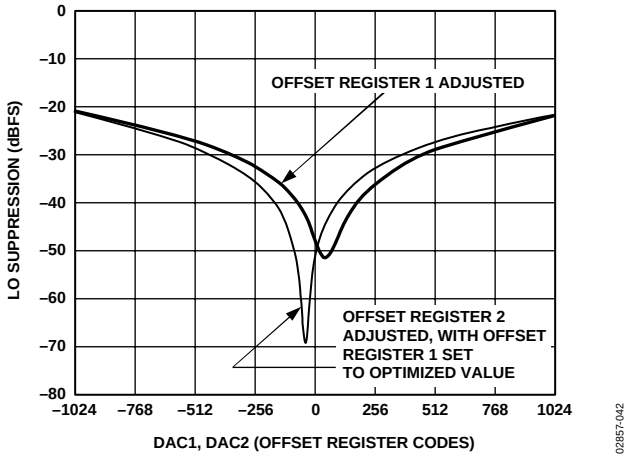


Figure 42. Offset Adjust Control, Effect on LO Suppression

1R/2R MODE

In 2R mode, the reference current for each channel is set independently by the FSADJ resistor on that channel. The AD9773 can be programmed to derive its reference current from a single resistor on Pin 60 by putting the part into 1R mode. The transfer functions in Equation 1 are valid for 2R mode. In 1R mode, the current developed in the single FSADJ resistor is split equally between the two channels. The result is that in 1R mode, a scale factor of 1/2 must be applied to the formulas in Equation 1. The full-scale DAC current in 1R mode can still be set to as high as 20 mA by using the internal 1.2 V reference and a 950 Ω resistor instead of the 1.9 kΩ resistor typically used in 2R mode.

CLOCK INPUT CONFIGURATIONS

The clock inputs to the AD9773 can be driven differentially or single-ended. The internal clock circuitry has supply and ground (CLKVDD, CLKGND) separate from the other supplies on the chip to minimize jitter from internal noise sources.

Figure 43 shows the AD9773 driven from a single-ended clock source. The CLK+/CLK− pins form a differential input (CLKIN) so that the statically terminated input must be dc-biased to the midswing voltage level of the clock driven input.

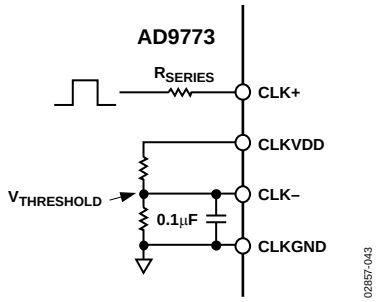


Figure 43. Single-Ended Clock Driving Clock Inputs

A configuration for differentially driving the clock inputs is given in Figure 44. DC-blocking capacitors can be used to couple a clock driver output whose voltage swings exceed CLKVDD or CLKGND. If the driver voltage swings are within the supply range of the AD9773, the dc-blocking capacitors and bias resistors are not necessary.

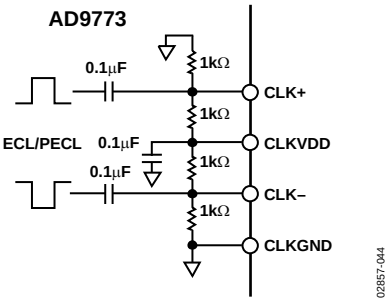


Figure 44. Differential Clock Driving Clock Inputs

A transformer, such as the T1-1T from Mini-Circuits®, can also be used to convert a single-ended clock to differential. This method is used on the AD9773 evaluation board so that an external sine wave with no dc offset can be used as a differential clock.

PECL/ECL drivers require varying termination networks, the details of which are left out of Figure 43 and Figure 44 but can be found in application notes such as the AND8020/D from On Semiconductor®.

These networks depend on the assumed transmission line impedance and power supply voltage of the clock driver. Optimum performance of the AD9773 is achieved when the driver is placed very close to the AD9773 clock inputs, thereby negating any transmission line effects such as reflections due to mismatch.

The quality of the clock and data input signals is important in achieving optimum performance. The external clock driver circuitry should provide the AD9773 with a low jitter clock input that meets the minimum/maximum logic levels while providing fast edges. Although fast clock edges help minimize any jitter that manifests itself as phase noise on a reconstructed waveform, the high gain bandwidth product of the AD9773's clock input comparator can tolerate differential sine wave inputs as low as 0.5 V p-p, with minimal degradation of the output noise floor.

PROGRAMMABLE PLL

CLKIN can function either as an input data rate clock (PLL enabled) or as a DAC data rate clock (PLL disabled) according to the state of Address 02h, Bit 7 in the SPI port register. The internal operation of the AD9773 clock circuitry in these two modes is illustrated in Figure 45 and Figure 46.

The PLL clock multiplier and distribution circuitry produce the necessary internal synchronized 1×, 2×, 4×, and 8× clocks for the rising edge triggered latches, interpolation filters, modulators, and DACs. This circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO), prescaler, clock distribution, and SPI port control. The charge pump, VCO, differential clock input buffer, phase detector, prescaler, and clock distribution are all powered from CLKVDD. PLL lock status is indicated by the logic signal at the DATACLK_PLL_LOCK pin, as well as by the status of Bit 1, Register 00h. To ensure optimum phase noise performance from the PLL clock multiplier and distribution, CLKVDD should originate from a clean analog supply. The VCO speed is a function of the input data rate, the interpolation rate, and the VCO prescaler, according to the following function:

$$VCO\,Speed(MHz) = Input\,Data\,Rate(MHz) \times Interpolation\ Rate \times Prescaler$$

Table 16 defines the minimum input data rates vs. the interpolation and PLL divider setting. If the input data rate drops below the defined minimum rates under these conditions, VCO phase noise may increase significantly.

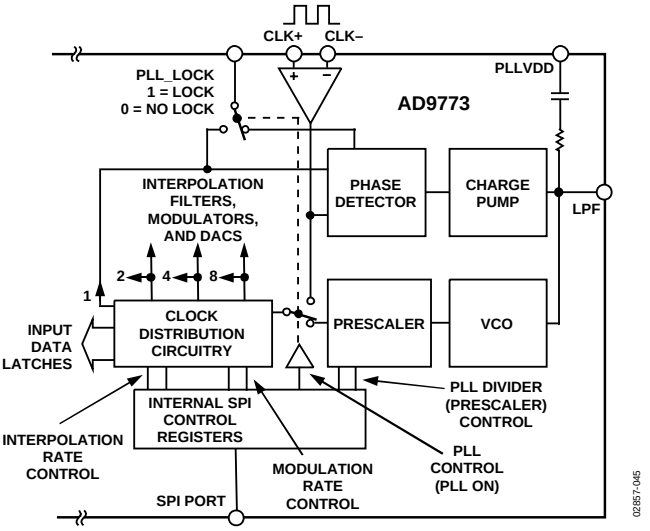


Figure 45. PLL and Clock Circuitry with PLL Enabled

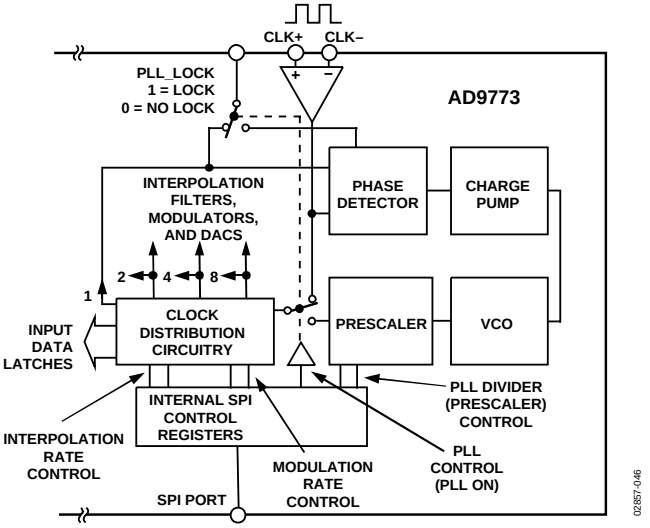


Figure 46. PLL and Clock Circuitry with PLL Disabled

In addition, if the zero stuffing option is enabled, the VCO doubles its speed again. Phase noise may be slightly higher with the PLL enabled. Figure 47 illustrates typical phase noise performance of the AD9773 with 2× interpolation and various input data rates. The signal synthesized for the phase noise measurement was a single carrier at a frequency of $f_{DATA}/4$. The repetitive nature of this signal eliminates quantization noise and distortion spurs as a factor in the measurement. Although the curves blend together in Figure 47, the different conditions are given for clarity in Table 17. Table 16 details PLL divider settings vs. interpolation rate and maximum and minimum f_{DATA} rates. Note that the maximum f_{DATA} rates of 160 MSPS are due to the maximum input data rate of the AD9773.

However, maximum rates of less than 160 MSPS and all minimum f_{DATA} rates are due to the maximum and minimum speeds of the internal PLL VCO. Figure 48 shows typical performance of the PLL lock signal (Pin 8 or Pin 53) when the PLL is in the process of locking.

Table 16. PLL Optimization

Interpolation Rate	Divider Setting	Minimum f_{DATA}	Maximum f_{DATA}
1	1	32	160
1	2	16	160
1	4	8	112
1	8	4	56
2	1	24	160
2	2	12	112
2	4	6	56
2	8	3	28
4	1	24	100
4	2	12	56
4	4	6	28
4	8	3	14
8	1	24	50
8	2	12	28
8	4	6	14
8	8	3	7

Table 17. Required PLL Prescaler Ratio vs. f_{DATA}

f_{DATA}	PLL	Prescaler Ratio
125 MSPS	Disabled	
125 MSPS	Enabled	Div 1
100 MSPS	Enabled	Div 2
75 MSPS	Enabled	Div 2
50 MSPS	Enabled	Div 4

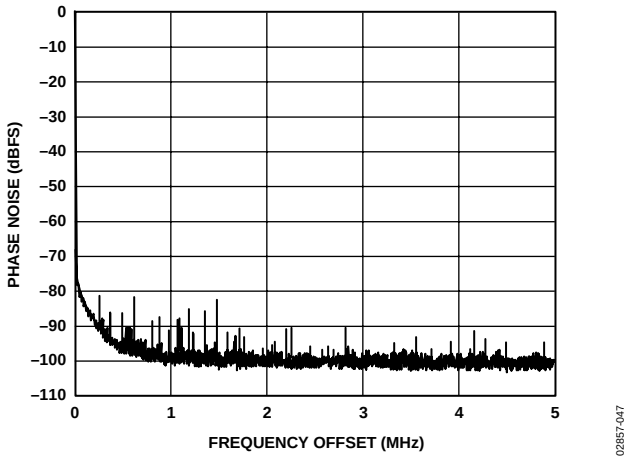


Figure 47. Phase Noise Performance

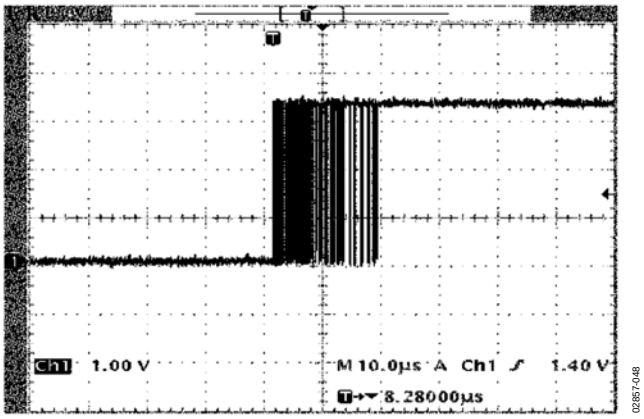


Figure 48. PLL_LOCK Output Signal (Pin 8) in the Process of Locking (Typical Lock Time)

It is important to note that the resistor/capacitor needed for the PLL loop filter is internal on the AD9773. This suffices unless the input data rate is below 10 MHz, in which case an external series RC is required between the LPF and CLKVDD pins.

POWER DISSIPATION

The AD9773 has three voltage supplies: DVDD, AVDD, and CLKVDD. Figure 49, Figure 50, and Figure 51 show the current required from each of these supplies when each is set to the 3.3 V nominal specified for the AD9773. Power dissipation (P_D) can easily be extracted by multiplying the given curves by 3.3. As Figure 49 shows, I_{DVDD} is very dependent on the input data rate, the interpolation rate, and the activation of the internal digital modulator. I_{DVDD}, however, is relatively insensitive to the modulation rate by itself. In Figure 50, I_{AVDD} shows the same type of sensitivity to the data, the interpolation rate, and the modulator function but to a much lesser degree (<10%). In Figure 51, I_{CLKVDD} varies over a wide range yet is responsible for only a small percentage of the overall AD9773 supply current requirements.

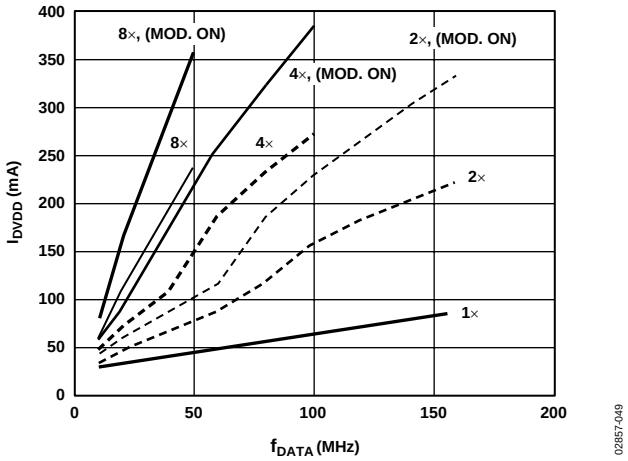


Figure 49. I_{DVDD} vs. f_{DATA} vs. Interpolation Rate, PLL Disabled

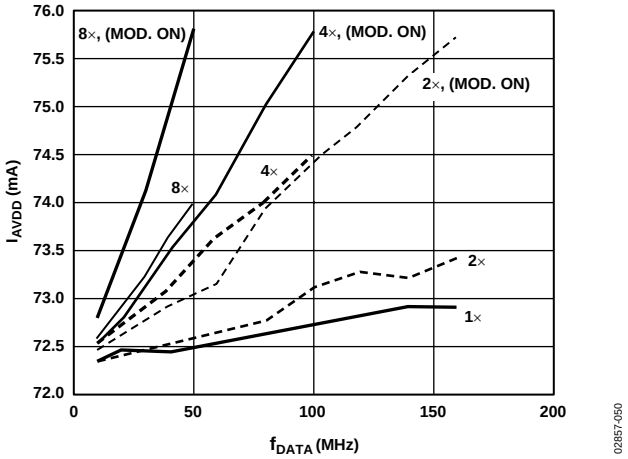


Figure 50. I_{AVDD} vs. f_{DATA} vs. Interpolation Rate, PLL Disabled

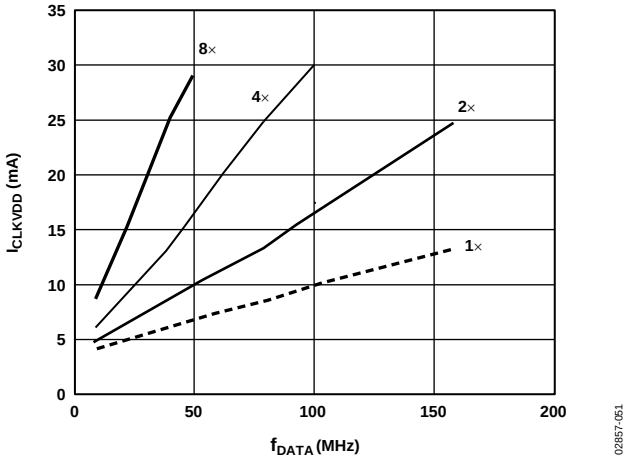


Figure 51. I_{CLKVDD} vs. f_{DATA} vs. Interpolation Rate, PLL Disabled

SLEEP/POWER-DOWN MODES

(Control Register 00h, Bit 3 and Bit 4)

The AD9773 provides two methods for programmable reduction in power savings. The sleep mode, when activated, turns off the DAC output currents but the rest of the chip remains functioning. When coming out of sleep mode, the AD9773 immediately returns to full operation. Power-down mode, on the other hand, turns off all analog and digital circuitry in the AD9773 except for the SPI port. When returning from power-down mode, enough clock cycles must be allowed to flush the digital filters of random data acquired during the power-down cycle.

TWO-PORT DATA INPUT MODE

The digital data input ports can be configured as two independent ports or as a single (one-port mode) port. In the two-port mode, data at the two input ports is latched into the AD9773 on every rising edge of the data rate clock (DATACLK). Also, in the two-port mode, the AD9773 can be programmed to generate an externally available DATACLK for the purpose of data synchronization. This data rate clock can be programmed to be available at either Pin 8 (DATACLK/PLL_LOCK) or Pin 53 (SPI_SDO). Because Pin 8 can also function as a PLL lock indicator when the PLL is enabled, there are several options for configuring Pin 8 and Pin 53. The following information describes the options.

PLL Off (Register 4, Bit 7 = 0)

Register 4, Bit 7 = 0; DATACLK out of Pin 8.
Register 4, Bit 7 = 1; DATACLK out of Pin 53.

PLL On (Register 4, Bit 7 = 1)

Register 4, Bit 7 = 0, Register 1, Bit 0 = 0; PLL lock indicator out of Pin 8.
Register 4, Bit 7 = 1, Register 1, Bit 0 = 0; PLL lock indicator out of Pin 53.
Register4, Bit 7 = 0, Register 1, Bit 0 = 1; DATACLK out of Pin 8.
Register 4, Bit 7 = 1, Register 1, Bit 0 = 1; DATACLK out of Pin 53.

In one-port mode, P2B14 and P2B15 from input data port two are redefined as IQSEL and ONEPORTCLK, respectively. The input data in one-port mode is steered to one of the two internal data channels based on the logic level of IQSEL. A clock signal, ONEPORTCLK, is generated by the AD9773 in this mode for the purpose of data synchronization. ONEPORTCLK runs at the input interleaved data rate, which is 2× the data rate at the internal input to either channel.

Test configurations showing the various clocks that are required and generated by the AD9773 with the PLL enabled/disabled and in the one-port/two-port modes are given in Figure 101 to Figure 104. Jumper positions needed to operate the AD9773 evaluation board in these modes are given as well.

ONE-PORT/TWO-PORT INPUT MODES

The digital data input ports can be configured as two independent ports or as a single (one-port mode) port. In two-port mode, the AD9773 can be programmed to generate an externally available data rate clock (DATACLK) for the purpose of data synchronization. Data at the two input ports can be latched into the AD9773 on every rising clock edge of DATACLK. In one-port mode, P2B10 and P2B11 from Input Data Port 2 are redefined as IQSEL and ONEPORTCLK, respectively. The input data in one-port mode is steered to one of the two internal data channels based on the logic level of IQSEL. A clock signal, ONEPORTCLK, is generated by the AD9773 in this mode for the purpose of external data synchronization. ONEPORTCLK runs at the input interleaved data rate, which is 2× the data rate at the internal input to either channel.

Test configurations showing the various clocks required and produced by the AD9773 in the PLL and one-port/two-port modes are given in Figure 101 to Figure 104. Jumper positions needed to operate the AD9773 evaluation board in these modes are given as well.

PLL ENABLED, TWO-PORT MODE

(Control Register 02h, Bits [6:0] and 04h, Bits [7:1]

With the phase-locked loop (PLL) enabled and the AD9773 in two-port mode, the speed of CLKIN is inherently that of the input data rate. In two-port mode, Pin 8 (DATACLK/PLL_ LOCK) can be programmed (Control Register 01h, Bit 0) to function as either a lock indicator for the internal PLL or as a clock running at the input data rate. When Pin 8 is used as a clock output (DATACLK), its frequency is equal to that of CLKIN. Data at the input ports is latched into the AD9773 on the rising edge of the CLKIN. Figure 52 shows the delay, t_{OD}, inherent between the rising edge of CLKIN and the rising edge of DATACLK, as well as the setup and hold requirements for the data at Ports 1 and 2. The setup and hold times given in Figure 52 are the input data transitions with respect to CLKIN. Note that in two-port mode (PLL enabled or disabled), the data rate at the interpolation filter inputs is the same as the input data rate at Ports 1 and 2.

The DAC output sample rate in two-port mode is equal to the clock input rate multiplied by the interpolation rate. If zero stuffing is used, another factor of 2 must be included to calculate the DAC sample rate.

DATACLK INVERSION

(Control Register 02h, Bit 4)

By programming this bit, the DATACLK signal shown in Figure 52 can be inverted. With inversion enabled, t_{OD} refers to the time between the rising edge of CLKIN and the falling edge of DATACLK. No other effect on timing occurs.

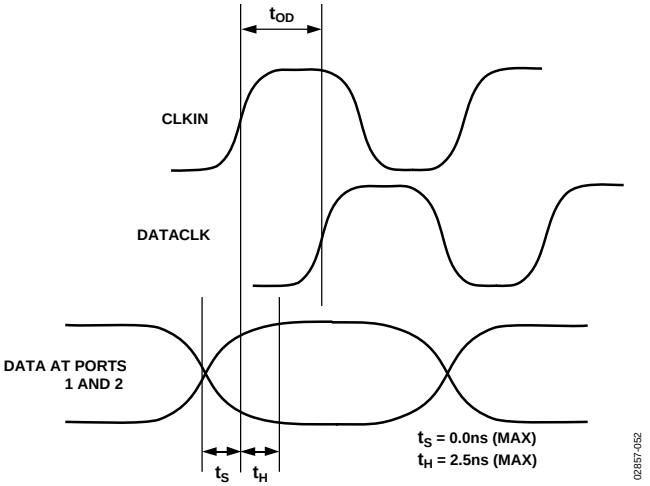


Figure 52. Timing Requirements in Two-Port Input Mode with PLL Enabled

DATACLK DRIVER STRENGTH

(Control Register 02h, Bit 5)

The DATACLK output driver strength is capable of driving >10 mA into a 330 Ω load while providing a rise time of 3 ns. Figure 53 shows DATACLK driving a 330 Ω resistive load at a frequency of 50 MHz. By enabling the drive strength option (Control Register 02h, Bit 5), the amplitude of DATACLK under these conditions increases by approximately 200 mV.

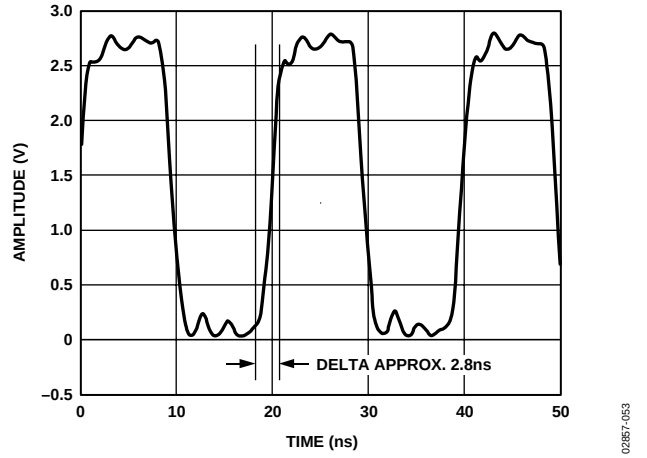


Figure 53. DATACLK Driver Capability into 330 Ω at 50 MHz

PLL ENABLED, ONE-PORT MODE

(Control Register 02h, Bits [6:1] and 04h, Bits [7:1]

In one-port mode, the I and Q channels receive their data from an interleaved stream at Digital Input Port 1. The function of Pin 32 is defined as an output (ONEPORTCLK) that generates a clock at the interleaved data rate, which is 2× the internal input data rate of the I and Q channels. The frequency of CLKIN is equal to the internal input data rate of the I and Q channels. The selection of the data for the I or Q channel is determined by the state of the logic level at Pin 31 (IQSEL when the AD9773 is in one-port mode) on the rising edge of ONEPORTCLK. Under these conditions, IQSEL = 0 latches the data into the I channel on the clock rising edge, while IQSEL = 1 latches the data into the Q channel. It is possible to invert the I and Q selection by setting Control Register 02h, Bit 1 to the invert state (Logic 1). Figure 54 illustrates the timing requirements for the data inputs as well as the IQSEL input. Note that the 1× interpolation rate is not available in the one-port mode.

The DAC output sample rate in one port mode is equal to CLKIN multiplied by the interpolation rate. If zero stuffing is used, another factor of 2 must be included to calculate the DAC sample rate.

ONEPORTCLK INVERSION

(Control Register 02h, Bit 2)

By programming this bit, the ONEPORTCLK signal shown in Figure 54 can be inverted. With inversion enabled, t_{OD} refers to the delay between the rising edge of the external clock and the falling edge of ONEPORTCLK. The setup and hold times, t_S and t_H, are with respect to the falling edge of ONEPORTCLK. There is no other effect on timing.

ONEPORTCLK DRIVER STRENGTH

The drive capability of ONEPORTCLK is identical to that of DATACLK in the two-port mode. Refer to Figure 53 for performance under load conditions.

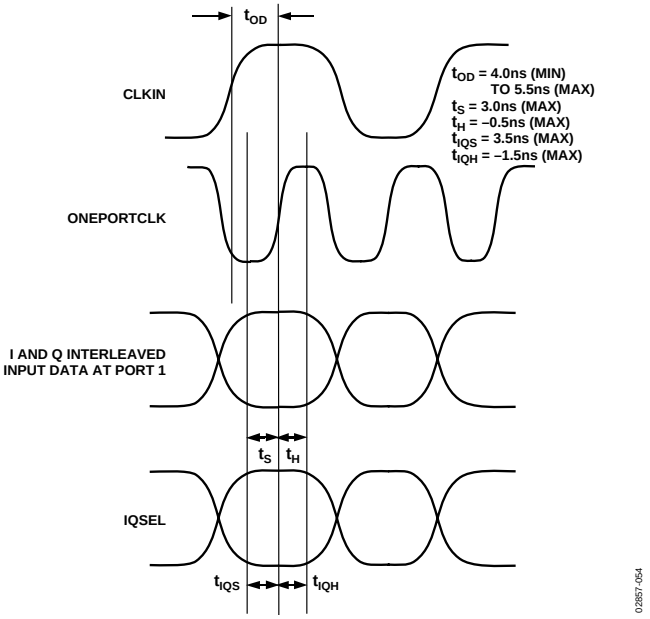


Figure 54. Timing Requirements in One-Port Input Mode with the PLL Enabled

IQ PAIRING

(Control Register 02h, Bit 0)

In one-port mode, the interleaved data is latched into the AD9773 internal I and Q channels in pairs. The order of how the pairs are latched internally is defined by this control register. The following is an example of the effect this has on incoming interleaved data.

Given the following interleaved data stream, where the data indicates the value with respect to full scale:

I	Q	I	Q	I	Q	I	Q	I	Q
0.5	0.5	1	1	0.5	0.5	0	0	0.5	0.5

With the control register set to 0 (I first), the data appears at the internal channel inputs in the following order in time:

I Channel	0.5	1	0.5	0	0.5
Q Channel	0.5	1	0.5	0	0.5

With the control register set to 1 (Q first), the data appears at the internal channel inputs in the following order in time:

I Channel	0.5	1	0.5	0	0.5	x
Q Channel	y	0.5	1	0.5	0	0.5

The values x and y represent the next I value and the previous Q value in the series.

PLL DISABLED, TWO-PORT MODE

With the PLL disabled, a clock at the DAC output rate must be applied to CLKIN. Internal clock dividers in the AD9773 synthesize the DATACLK signal at Pin 8, which runs at the input data rate and can be used to synchronize the input data. Data is latched into input Ports 1 and 2 of the AD9773 on the rising edge of DATACLK. DATACLK speed is defined as the speed of CLKIN divided by the interpolation rate. With zero stuffing enabled, this division increases by a factor of 2. Figure 55 illustrates the delay between the rising edge of CLKIN and the rising edge of DATACLK, as well as t_S and t_H in this mode.

The programmable modes DATACLK inversion and DATACLK driver strength described in the previous section (PLL Enabled, Two-Port Mode) have identical functionality with the PLL disabled.

The data rate clock created by dividing down the DAC clock in this mode can be programmed (via Register 03h, Bit 7) to be output from the SPI_SDO pin, rather than the DATACLK pin. In some applications, this may improve complex image rejection. When SPI_SDO is used as data rate clock out, t_{OD} increases by 1.6 ns.

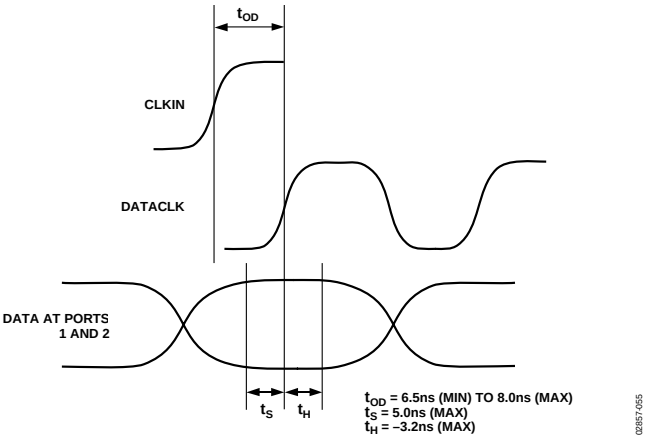


Figure 55. Timing Requirements in Two-Port Input Mode with PLL Disabled

PLL DISABLED, ONE-PORT MODE

In one-port mode, data is received into the AD9773 as an interleaved stream on Port 1. A clock signal (ONEPORTCLK), running at the interleaved data rate, which is 2× the input data rate of the internal I and Q channels, is available for data synchronization at Pin 32.

With PLL disabled, a clock at the DAC output rate must be applied to CLKIN. Internal dividers synthesize the ONEPORTCLK signal at Pin 32. The selection of the data for the I or Q channel is determined by the state of the logic level applied to Pin 31 (IQSEL when the AD9773 is in one-port mode) on the rising edge of ONEPORTCLK.

Under these conditions, IQSEL = 0 latches the data into the I channel on the clock rising edge, while IQSEL = 1 latches the data into the Q channel. It is possible to invert the I and Q selection by setting Control Register 02h, Bit 1 to the invert state (Logic 1). Figure 56 illustrates the timing requirements for the data inputs as well as the IQSEL input. Note that the 1× interpolation rate is not available in the one-port mode.

One-port mode is very useful when interfacing with devices such as the Analog Devices AD6622 or AD6623 transmit signal processors, in which two digital data channels have been interleaved (multiplexed).

The programmable modes' ONEPORTCLK inversion, ONEPORTCLK driver strength and IQ pairing described in the PLL Enabled, Two-Port Mode section have identical functionality with the PLL disabled.

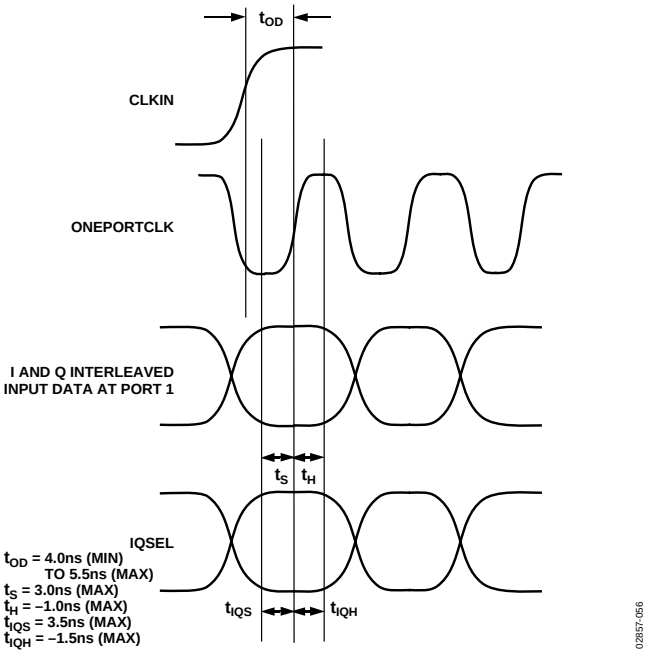


Figure 56. Timing Requirements in One-Port Input Mode with DLL Disabled

DIGITAL FILTER MODES

The I and Q data paths of the AD9773 have their own independent half-band FIR filters. Each data path consists of three FIR filters, providing up to 8× interpolation for each channel. The rate of interpolation is determined by the state of Control Register 01h, Bits 7 and 6. Figure 2 to Figure 4 show the response of the digital filters when the AD9773 is set to 2×, 4×, and 8× modes. The frequency axes of these graphs have been normalized to the input data rate of the DAC. As the graphs show, the digital filters can provide greater than 75 dB of out-of-band rejection.

An online tool is available for quick and easy analysis of the AD9773 interpolation filters in the various modes.

AMPLITUDE MODULATION

Given two sine waves at the same frequency, but with a 90° phase difference, a point of view in time can be taken such that the waveform that leads in phase is cosinusoidal and the waveform that lags is sinusoidal. Analysis of complex variables states that the cosine waveform can be defined as having real positive and negative frequency components, while the sine waveform consists of imaginary positive and negative frequency images. This is shown graphically in the frequency domain in Figure 57.

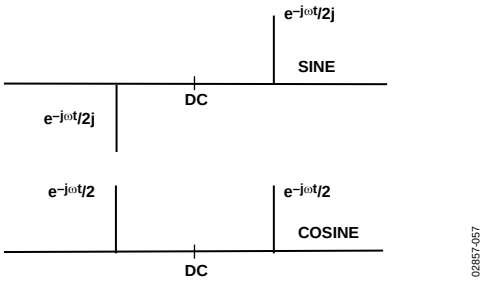


Figure 57. Real and Imaginary Components of Sinusoidal and Cosinusoidal Waveforms

Amplitude modulating a baseband signal with a sine or a cosine convolves the baseband signal with the modulating carrier in the frequency domain. Amplitude scaling of the modulated signal reduces the positive and negative frequency images by a factor of 2. This scaling is very important in the discussion of the various modulation modes. The phase relationship of the modulated signals is dependent on whether the modulating carrier is sinusoidal or cosinusoidal, again with respect to the reference point of the viewer. Examples of sine and cosine modulation are given in Figure 58.

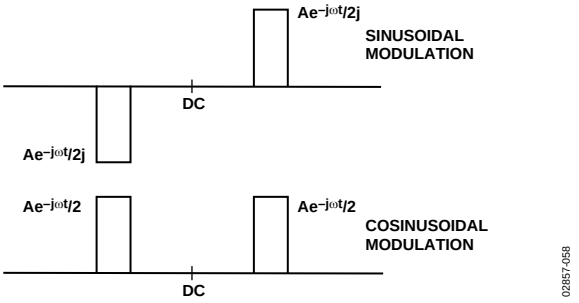


Figure 58. Baseband Signal, Amplitude Modulated with Sine and Cosine Carriers

MODULATION, NO INTERPOLATION

With Control Register 01h, Bit 7 and Bit 6 set to 00, the interpolation function on the AD9773 is disabled. Figure 59 to Figure 62 show the DAC output spectral characteristics of the AD9773 in the various modulation modes, all with the interpolation filters disabled. The modulation frequency is determined by the state of Control Register 01h, Bits 5 and 4. The tall rectangles represent the digital domain spectrum of a baseband signal of narrow bandwidth.

By comparing the digital domain spectrum to the DAC SIN(x)/x roll-off, an estimate can be made for the characteristics required for the DAC reconstruction filter. Note also, per the previous discussion on amplitude modulation, that the spectral components (where modulation is set to $f_S/4$ or $f_S/8$) are scaled by a factor of 2. In the situation where the modulation is $f_S/2$, the modulated spectral components add constructively, and there is no scaling effect.

The Effects of the Digital Modulation on the DAC Output Spectrum, Interpolation Disabled

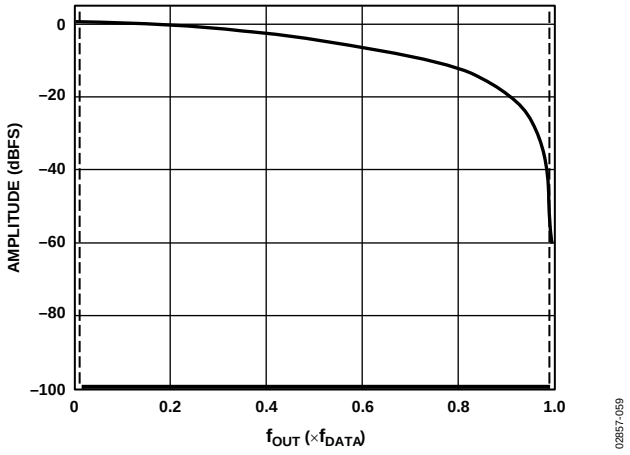


Figure 59. No Interpolation, Modulation Disabled

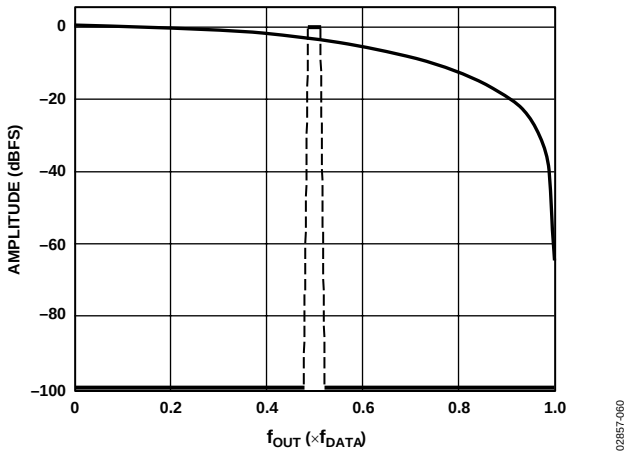


Figure 60. No Interpolation, Modulation = $f_{DAC}/2$

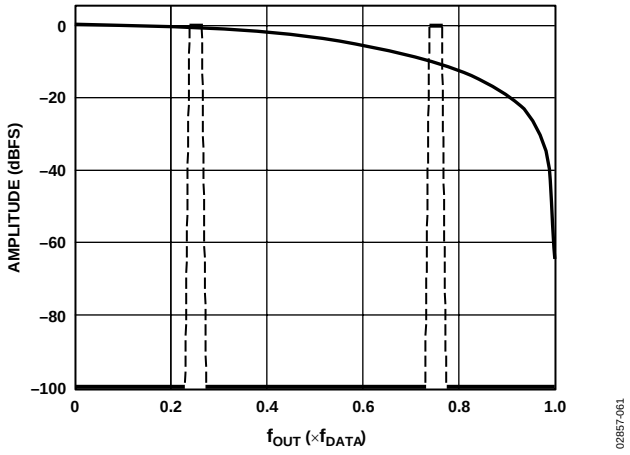


Figure 61. No Interpolation, Modulation = $f_{DAC}/4$

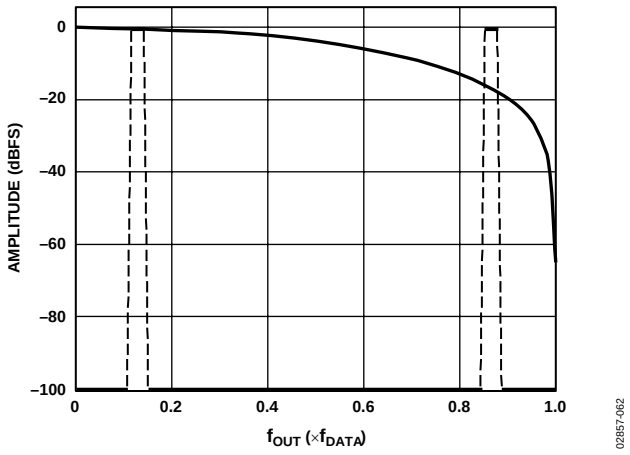


Figure 62. No Interpolation, Modulation = $f_{DAC}/8$

MODULATION, INTERPOLATION = 2×

With Control Register 01h, Bit 7 and Bit 6 set to 01, the interpolation rate of the AD9773 is 2×. Modulation is achieved by multiplying successive samples at the interpolation filter output by the sequence (+1, −1). Figure 63 to Figure 66 represent the spectral response of the AD9773 DAC output with 2× interpolation in the various modulation modes to a narrow band baseband signal (again, the tall rectangles in the graphic). The advantage of interpolation becomes clear in Figure 63 to Figure 66, where it can be seen that the images that would normally appear in the spectrum around the input data rate frequency are suppressed by >70 dB.

Another significant point is that the interpolation filtering is done previous to the digital modulator. For this reason, as Figure 63 to Figure 66 show, the pass band of the interpolation filters can be frequency shifted, giving the equivalent of a high-pass digital filter.

Note that when using the $f_S/4$ modulation mode, there is no true stop band as the band edges coincide with each other. In the $f_S/8$ modulation mode, amplitude scaling occurs over only a portion of the digital filter pass band due to constructive addition over just that section of the band.

The Effects of the Digital Modulation on the DAC Output Spectrum, Interpolation = 2×

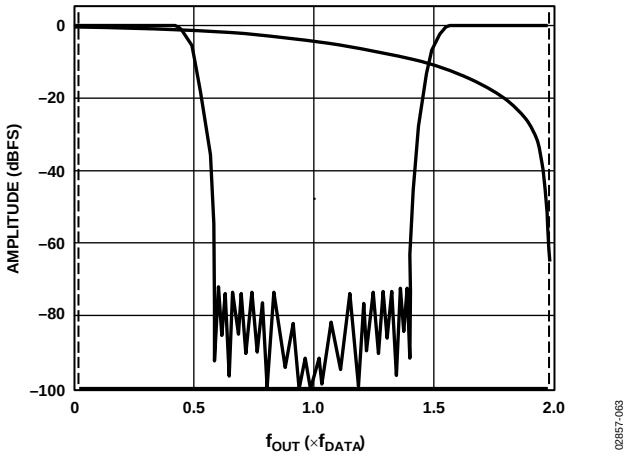


Figure 63. 2x Interpolation, Modulation = Disabled

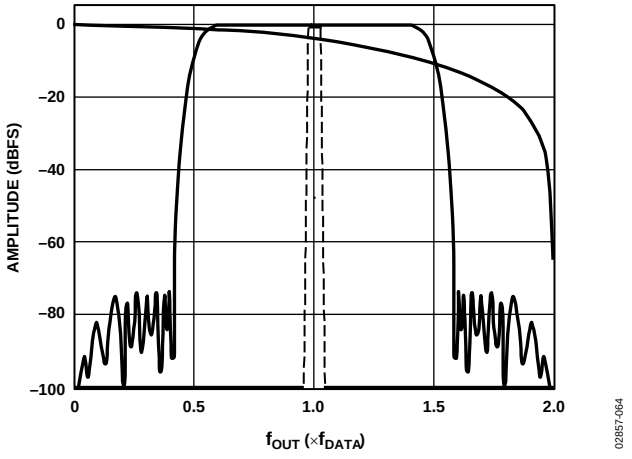


Figure 64. 2x Interpolation, Modulation = $f_{DAC}/2$

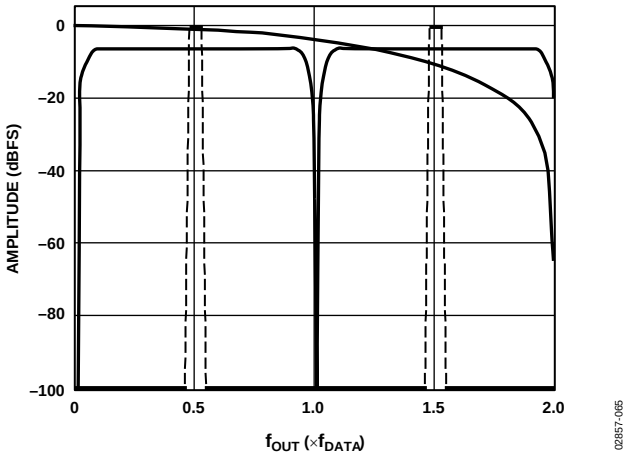


Figure 65. 2x Interpolation, Modulation = $f_{DAC}/4$

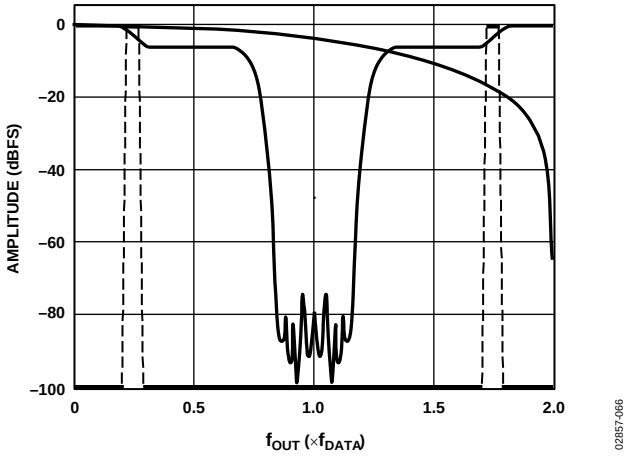


Figure 66. 2x Interpolation, Modulation = $f_{DAC}/8$

MODULATION, INTERPOLATION = 4×

With Control Register 01h, Bit 7 and Bit 6 set to 10, the interpolation rate of the AD9773 is 4×. Modulation is achieved by multiplying successive samples at the interpolation filter output by the sequence (0, +1, 0, −1).

Figure 67 to Figure 70 represent the spectral response of the AD9773 DAC output with 4× interpolation in the various modulation modes to a narrow band baseband signal.

The Effects of the Digital Modulation on the DAC Output Spectrum Interpolation = 4×

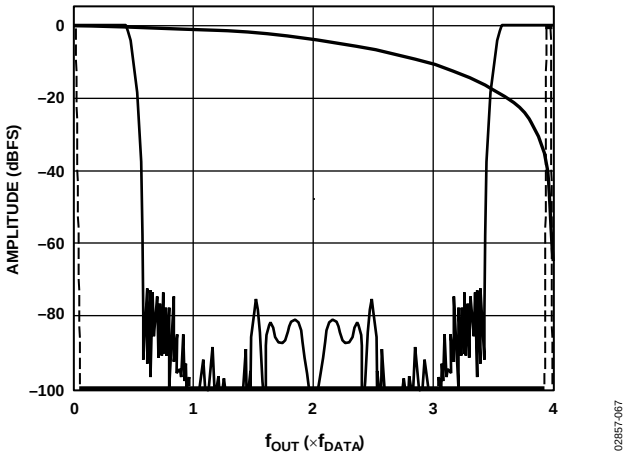


Figure 67. 4x Interpolation, Modulation Disabled

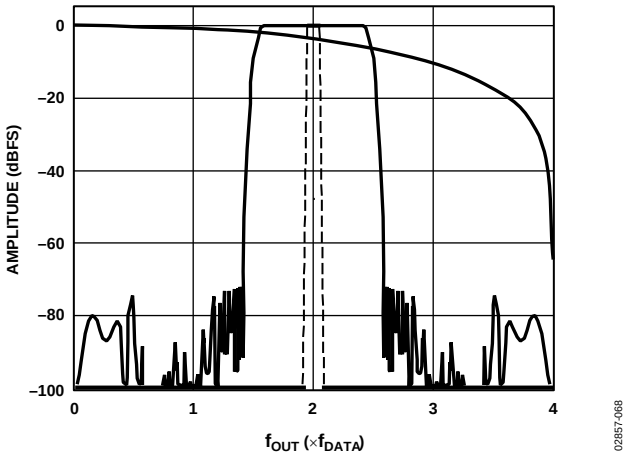


Figure 68. 4x Interpolation, Modulation = $f_{DAC}/2$

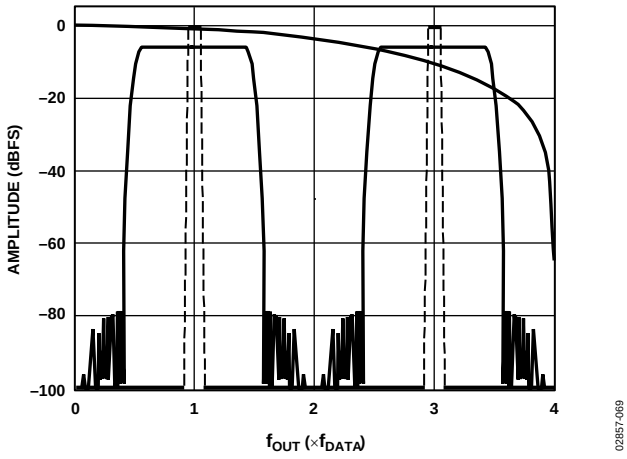


Figure 69. 4x Interpolation, Modulation = $f_{DAC}/4$

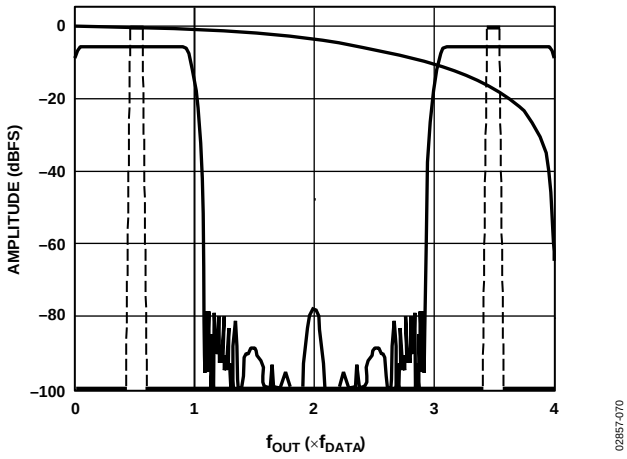


Figure 70. 4x Interpolation, Modulation = $f_{DAC}/8$

MODULATION, INTERPOLATION = 8×

With Control Register 01h, Bit 7 and Bit 6 set to 11, the interpolation rate of the AD9773 is 8×. Modulation is achieved by multiplying successive samples at the interpolation filter output by the sequence (0, +0.707, +1, +0.707, 0, −0.707, −1, +0.707). Figure 71 to Figure 74 represent the spectral response of the AD9773 DAC output with 8× interpolation in the various modulation modes to a narrow band baseband signal.

Looking at Figure 63 to Figure 74, the user can see how higher interpolation rates reduce the complexity of the reconstruction filter needed at the DAC output. It also becomes apparent that the ability to modulate by $f_S/2$, $f_S/4$, or $f_S/8$ adds a degree of flexibility in frequency planning.

The Effects of the Digital Modulation on the DAC Output Spectrum, Interpolation = 8×

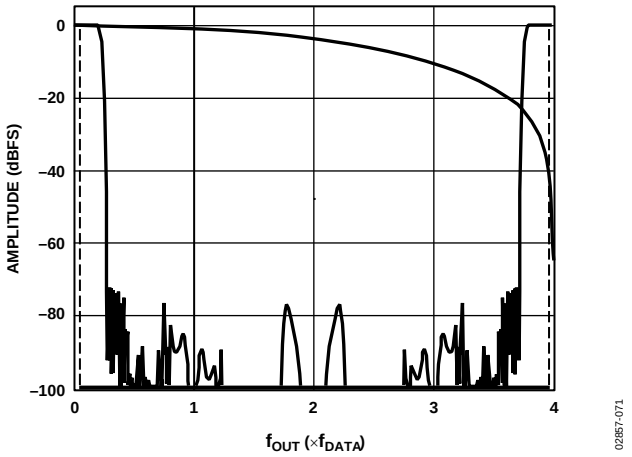


Figure 71. 8x Interpolation, Modulation Disabled

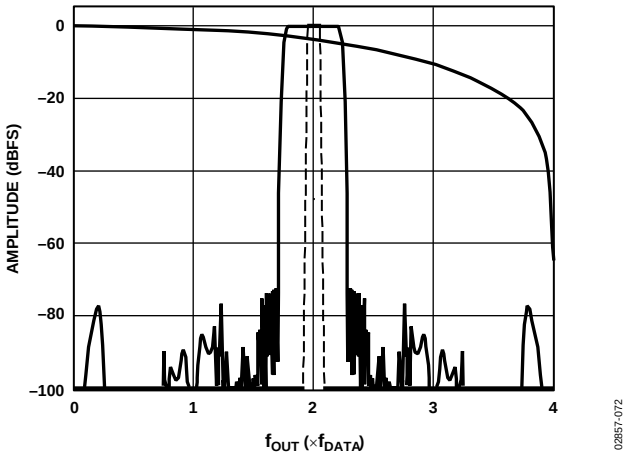


Figure 72. 8x Interpolation, Modulation = $f_{DAC}/2$

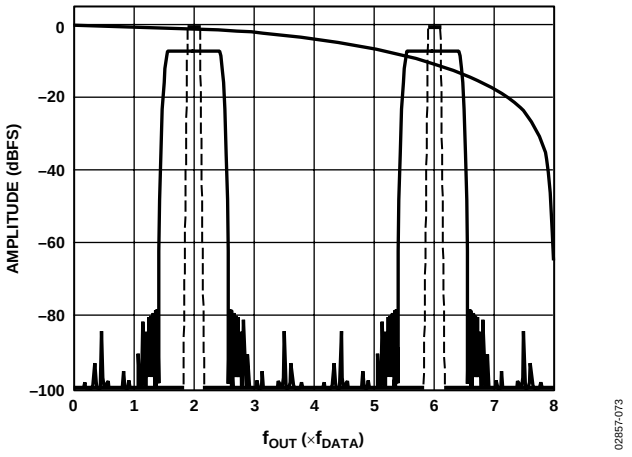


Figure 73. 8x Interpolation, Modulation = $f_{DAC}/4$

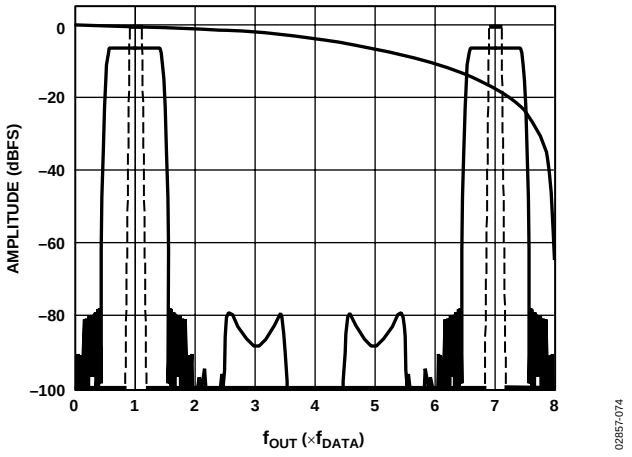


Figure 74. 8x Interpolation, Modulation = $f_{DAC}/8$

ZERO STUFFING

(Control Register 01h, Bit 3)

As shown in Figure 75, a 0 or null in the output frequency response of the DAC (after interpolation, modulation, and DAC reconstruction) occurs at the final DAC sample rate (f_{DAC}). This is due to the inherent SIN(x)/x roll-off response in the digital-to-analog conversion. In applications where the desired frequency content is below $f_{DAC}/2$, this may not be a problem. Note that at $f_{DAC}/2$, the loss due to SIN(x)/x is 4 dB. In direct RF applications, this roll-off may be problematic due to the increased pass-band amplitude variation as well as the reduced amplitude of the desired signal.

Consider an application where the digital data into the AD9773 represents a baseband signal around $f_{DAC}/4$ with a pass band of $f_{DAC}/10$. The reconstructed signal out of the AD9773 would experience only a 0.75 dB amplitude variation over its pass band. However, the image of the same signal occurring at $3 \times f_{DAC}/4$ suffers from a pass-band flatness variation of 3.93 dB. This image may be the desired signal in an IF application using one of the various modulation modes in the AD9773. This roll-off of image frequencies can be seen in Figure 59 to Figure 74, where the effect of the interpolation and modulation rate is apparent as well.

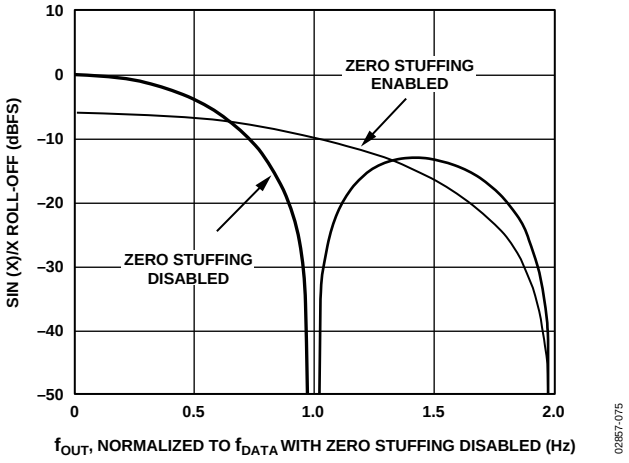


Figure 75. Effect of Zero Stuffing on DAC's SIN(x)/x Response

To improve upon the pass-band flatness of the desired image, the zero stuffing mode can be enabled by setting the control register bit to Logic 1. This option increases the ratio of f_{DAC}/f_{DATA} by a factor of 2 by doubling the DAC sample rate and inserting a midscale sample (that is, 1000 0000 0000 0000) after every data sample originating from the interpolation filter. This is important as it affects the PLL divider ratio needed to keep the VCO within its optimum speed range. Note that the zero stuffing takes place in the digital signal chain at the output of the digital modulator, before the DAC.

The net effect is to increase the DAC output sample rate by a factor of 2× with the 0 in the SIN(x)/x DAC transfer function occurring at twice the original frequency. A 6 dB loss in amplitude at low frequencies is also evident, as can be seen in Figure 76.

It is important to realize that the zero stuffing option by itself does not change the location of the images but rather their amplitude, pass-band flatness, and relative weighting. For instance, in the previous example, the pass-band amplitude flatness of the image at $3 \times f_{DATA}/4$ is now improved to 0.59 dB while the signal level has increased slightly from −10.5 dBFS to −8.1 dBFS.

INTERPOLATING (COMPLEX MIX MODE)

(Control Register 01h, Bit 2)

In the complex mix mode, the two digital modulators on the AD9773 are coupled to provide a complex modulation function. In conjunction with an external quadrature modulator, this complex modulation can be used to realize a transmit image rejection architecture. The complex modulation function can be programmed for $e^{+j\omega t}$ or $e^{-j\omega t}$ to give upper or lower image rejection. As in the real modulation mode, the modulation frequency ω can be programmed via the SPI port for $f_{DAC}/2$, $f_{DAC}/4$, and $f_{DAC}/8$, where f_{DAC} represents the DAC output rate.

OPERATIONS ON COMPLEX SIGNALS

Truly complex signals cannot be realized outside of a computer simulation. However, two data channels, both consisting of real data, can be defined as the real and imaginary components of a complex signal. I (real) and Q (imaginary) data paths are often defined this way. By using the architecture defined in Figure 76, a system can be realized that operates on complex signals, giving a complex (real and imaginary) output.

If a complex modulation function ($e^{+j\omega t}$) is desired, the real and imaginary components of the system correspond to the real and imaginary components of $e^{+j\omega t}$ or cosωt and sinωt. As Figure 77 shows, the complex modulation function can be realized by applying these components to the structure of the complex system defined in Figure 76.

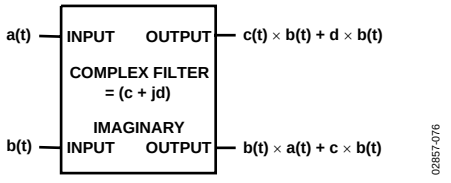


Figure 76. Realization of a Complex System

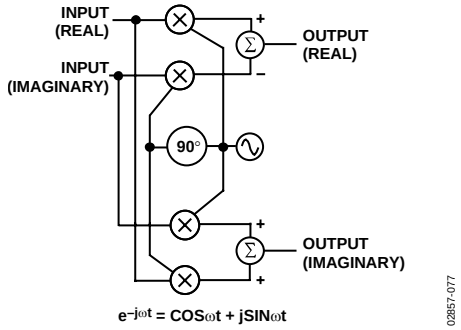


Figure 77. Implementation of a Complex Modulator

COMPLEX MODULATION AND IMAGE REJECTION OF BASEBAND SIGNALS

In traditional transmit applications, a two-step upconversion is done in which a baseband signal is modulated by one carrier to an intermediate frequency (IF) and then modulated a second time to the transmit frequency. Although this approach has several benefits, a major drawback is that two images are created near the transmit frequency. Only one image is needed, the other being an exact duplicate. Unless the unwanted image is filtered, typically with analog components, transmit power is wasted and the usable bandwidth available in the system is reduced.

A more efficient method of suppressing the unwanted image can be achieved by using a complex modulator followed by a quadrature modulator. Figure 78 is a block diagram of a quadrature modulator. Note that it is in fact the real output half of a complex modulator. The complete upconversion can actually be referred to as two complex upconversion stages, the real output of which becomes the transmitted signal.

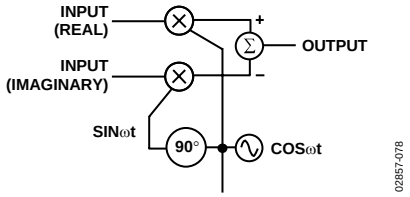
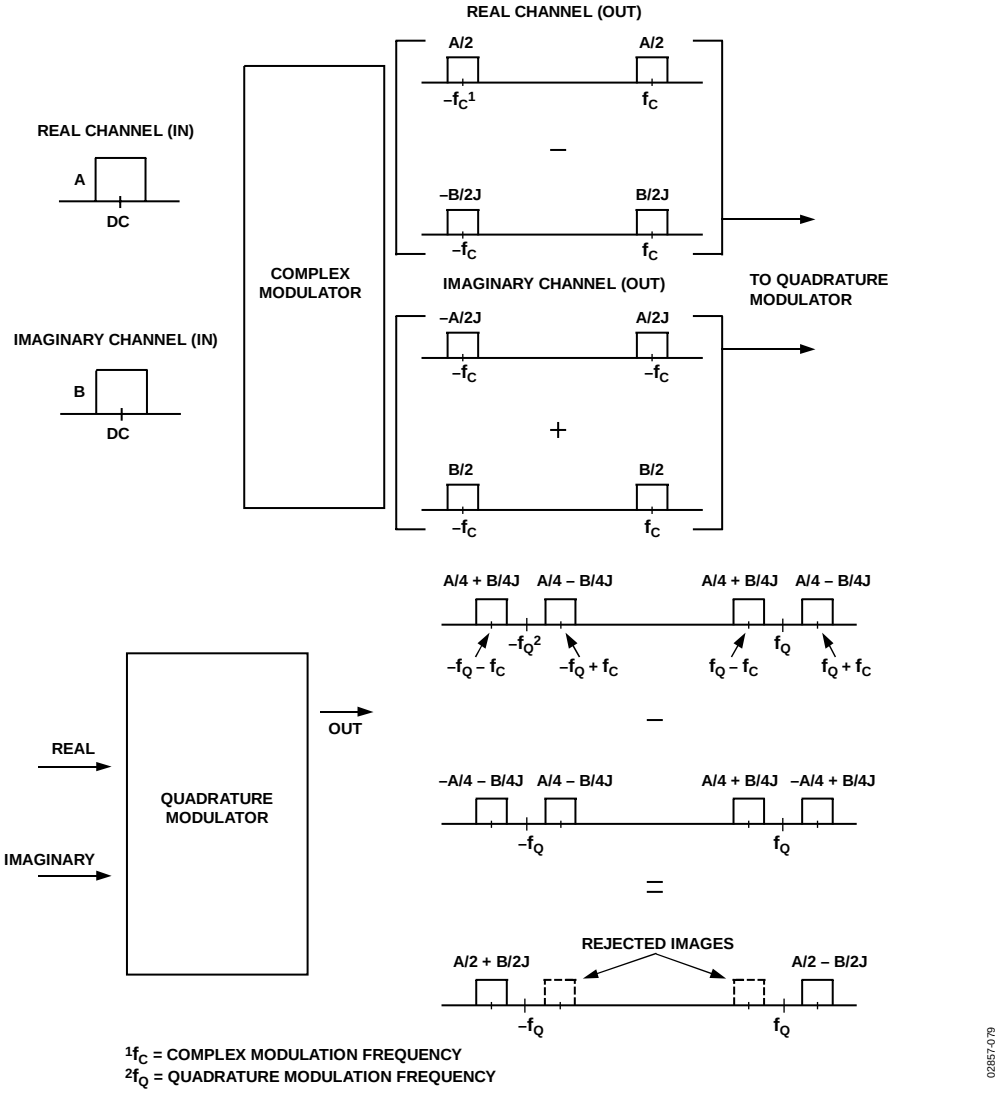


Figure 78. Quadrature Modulator

The entire upconversion from baseband to transmit frequency is represented graphically in Figure 79. The resulting spectrum shown in Figure 79 represents the complex data consisting of the baseband real and imaginary channels, now modulated onto orthogonal (cosine and negative sine) carriers at the transmit frequency. It is important to remember that in this application (two baseband data channels) the image rejection is not dependent on the data at either of the AD9773 input channels. In fact, image rejection still occurs with either one or both of the AD9773 input channels active. Note that by changing the sign of the sinusoidal multiplying term in the complex modulator, the upper sideband image could be suppressed while passing the lower one. This is easily done in the AD9773 by selecting the $e^{+j\omega t}$ bit (Register 01h, Bit 1). In purely complex terms, Figure 79 represents the two-stage upconversion from complex baseband to carrier.



1fC = COMPLEX MODULATION FREQUENCY
2fQ = QUADRATURE MODULATION FREQUENCY

Figure 79. Two-Stage Upconversion and Resulting Image Rejection

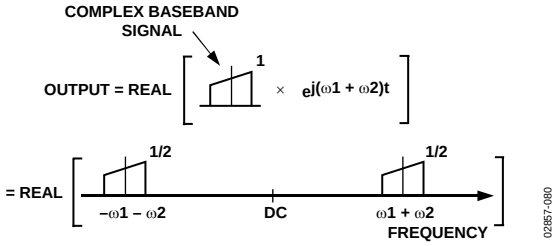


Figure 80. Two-Stage Complex Upconversion

IMAGE REJECTION AND SIDEBAND SUPPRESSION OF MODULATED CARRIERS

As shown in Figure 79, image rejection can be achieved by applying baseband data to the AD9773 and following the AD9773 with a quadrature modulator. To process multiple carriers while still maintaining image reject capability, each carrier must be complex modulated. As Figure 81 shows, single or multiple complex modulators can be used to synthesize complex carriers. These complex carriers are then summed and applied to the real and imaginary inputs of the AD9773.

A system in which multiple baseband signals are complex modulated and then applied to the AD9773 real and imaginary inputs followed by a quadrature modulator is shown in Figure 82, which also describes the transfer function of this system and the spectral output. Note the similarity of the transfer functions given in Figure 82 and Figure 80. Figure 82 adds an additional complex modulator stage for the purpose of summing multiple carriers at the AD9773 inputs. Also, as in Figure 79, the image rejection is not dependent on the real or imaginary baseband data on any channel. Image rejection on a channel occurs if either the real or imaginary data, or both, is present on the baseband channel.

It is important to remember that the magnitude of a complex signal can be 1.414× the magnitude of its real or imaginary components. Due to this 3 dB increase in signal amplitude, the real and imaginary inputs to the AD9773 must be kept at least 3 dB below full scale when operating with the complex modulator. Overranging in the complex modulator results in severe distortion at the DAC output.

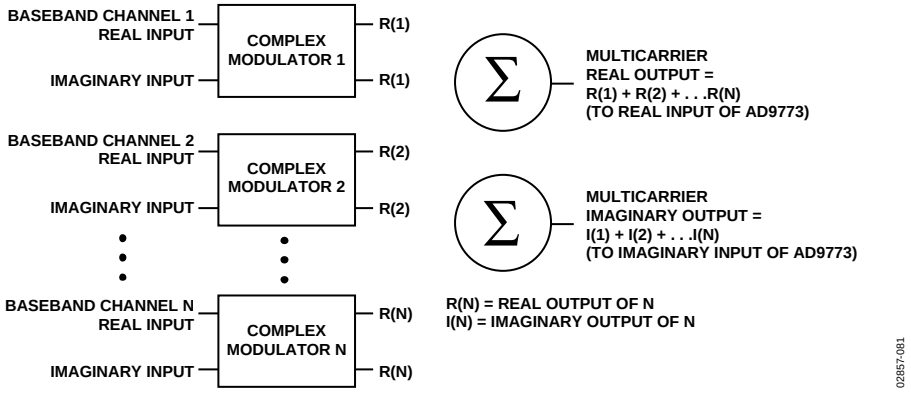


Figure 81. Synthesis of Multicarrier Complex Signal

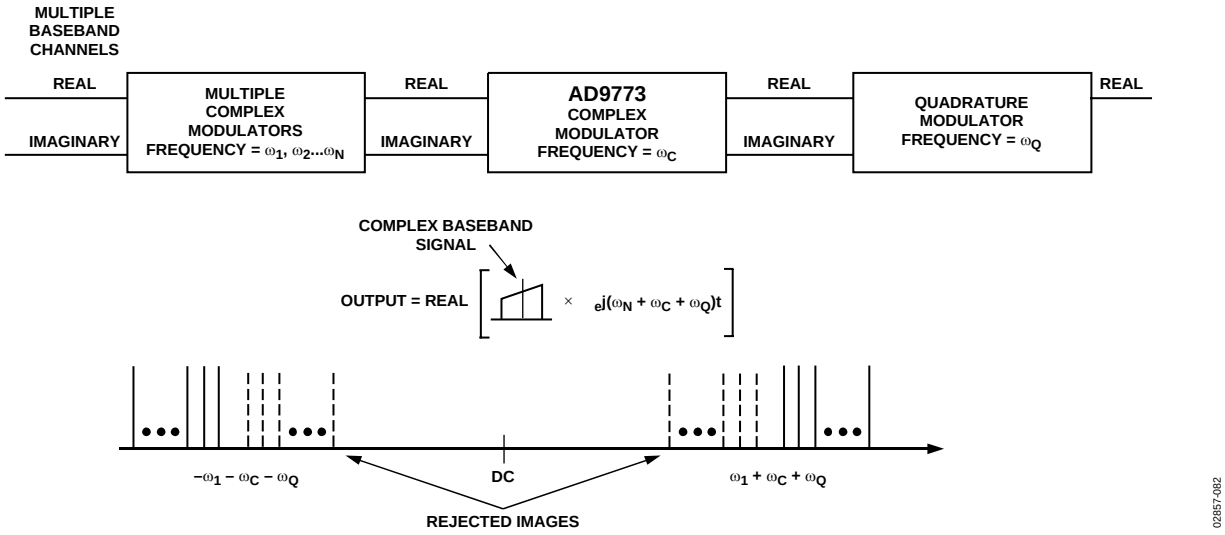


Figure 82. Image Rejection with Multicarrier Signals

The complex carrier synthesized in the AD9773 digital modulator is accomplished by creating two real digital carriers in quadrature. Carriers in quadrature cannot be created with the modulator running at $f_{DAC}/2$. As a result, complex modulation only functions with modulation rates of $f_{DAC}/4$ and $f_{DAC}/8$.

Regions A and B of Figure 83 to Figure 88 are the result of the complex signal described previously, when complex modulated in the AD9773 by $+e^{j\omega t}$. Regions C and D are the result of the complex signal described previously, again with positive frequency components only, modulated in the AD9773 by $-e^{j\omega t}$. The analog quadrature modulator after the AD9773 inherently modulates by $+e^{j\omega t}$.

Region A

Region A is a direct result of the upconversion of the complex signal near baseband. If viewed as a complex signal, only the images in Region A remain. The complex Signal A, consisting of positive frequency components only in the digital domain, has images in the positive odd Nyquist zones (1, 3, 5, …), as well as images in the negative even Nyquist zones. The appearance and rejection of images in every other Nyquist zone becomes more apparent at the output of the quadrature modulator. The A images appear on the real and the imaginary outputs of the AD9773, as well as on the output of the quadrature modulator, where the center of the spectral plot now represents the quadrature modulator LO and the horizontal scale now represents the frequency offset from this LO.

Region B

Region B is the image (complex conjugate) of Region A. If a spectrum analyzer is used to view the real or imaginary DAC outputs of the AD9773, Region B appears in the spectrum. However, on the output of the quadrature modulator, Region B is rejected.

Region C

Region C is most accurately described as a downconversion, as the modulating carrier is $-e^{j\omega t}$. If viewed as a complex signal, only the images in Region C remain. This image appears on the real and imaginary outputs of the AD9773, as well as on the output of the quadrature modulator, where the center of the spectral plot now represents the quadrature modulator LO and the horizontal scale represents the frequency offset from this LO.

Region D

Region D is the image (complex conjugate) of Region C. If a spectrum analyzer is used to view the real or imaginary DAC outputs of the AD9773, Region D appears in the spectrum. However, on the output of the quadrature modulator, Region D is rejected.

Figure 89 to Figure 96 show the measured response of the AD9773 and AD8345 given the complex input signal to the AD9773 in Figure 89. The data in these graphs was taken with a data rate of 12.5 MSPS at the AD9773 inputs. The interpolation rate of 4× or 8× gives a DAC output data rate of 50 MSPS or 100 MSPS. As a result, the high end of the DAC output spectrum in these graphs is the first null point for the SIN(x)/x roll-off, and the asymmetry of the DAC output images is representative of the SIN(x)/x roll-off over the spectrum. The internal PLL was enabled for these results. In addition, a 35 MHz third-order low-pass filter was used at the AD9773/AD8345 interface to suppress DAC images.

An important point can be made by looking at Figure 91 and Figure 93. Figure 91 represents a group of positive frequencies modulated by complex $+f_{DAC}/4$, while Figure 93 represents a group of negative frequencies modulated by complex $-f_{DAC}/4$. When looking at the real or imaginary outputs of the AD9773, as shown in Figure 91 and Figure 93, the results look identical. However, the spectrum analyzer cannot show the phase relationship of these signals. The difference in phase between the two signals becomes apparent when they are applied to the AD8345 quadrature modulator, with the results shown in Figure 92 and Figure 94.

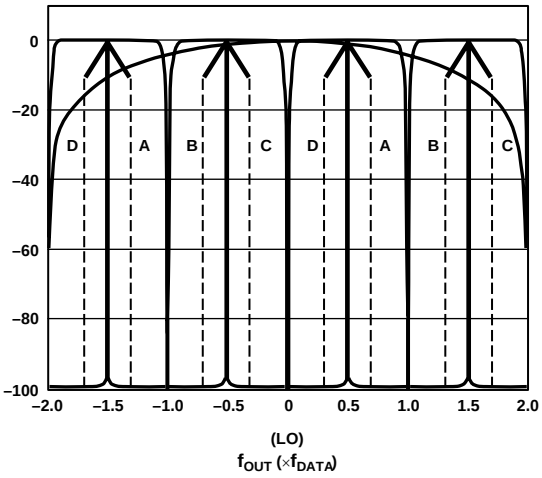


Figure 83. 2x Interpolation, Complex $f_{DAC}/4$ Modulation

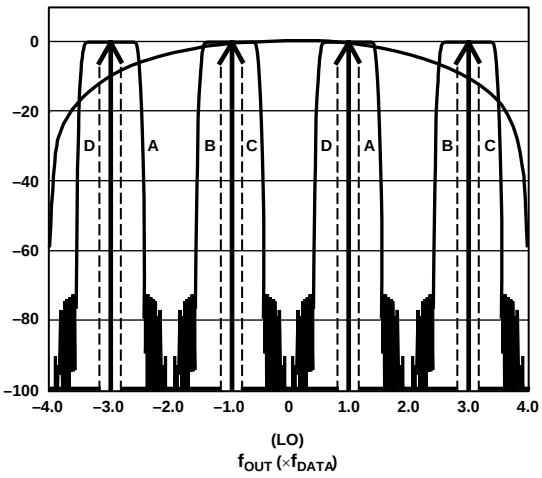


Figure 84. 4x Interpolation, Complex $f_{DAC}/4$ Modulation

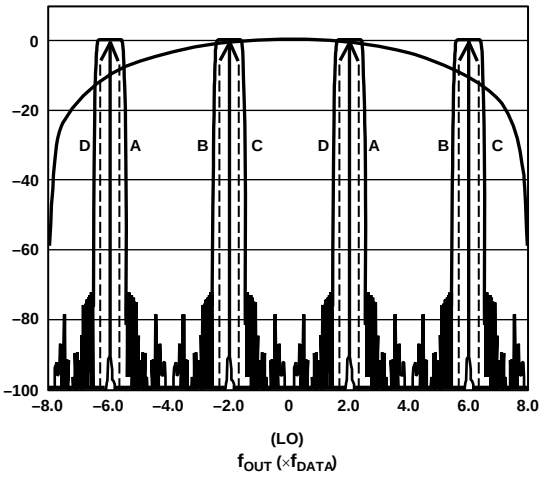


Figure 85. 8x Interpolation, Complex $f_{DAC}/4$ Modulation

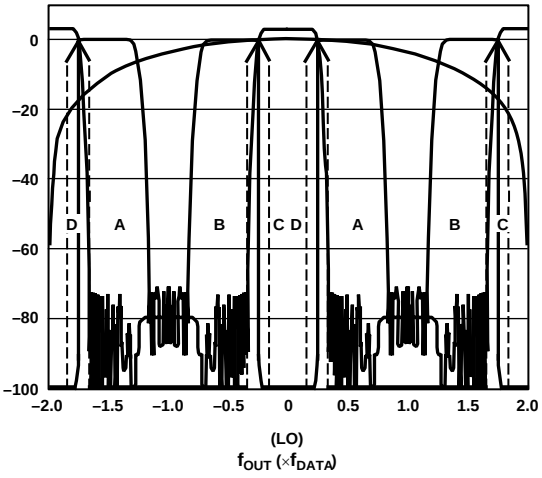


Figure 86. 2x Interpolation, Complex $f_{DAC}/8$ Modulation

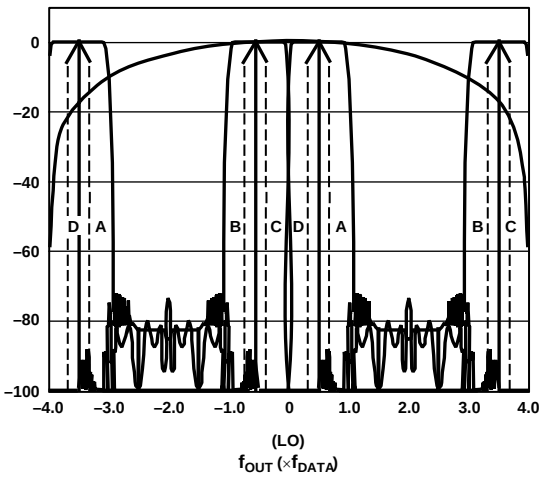


Figure 87. 4x Interpolation, Complex $f_{DAC}/8$ Modulation

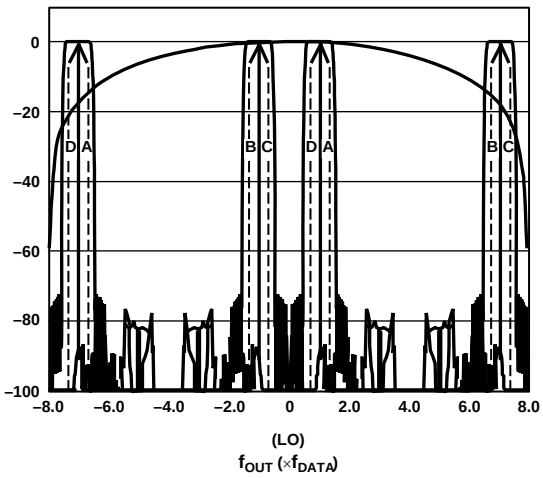


Figure 88. 8x Interpolation, Complex $f_{DAC}/8$ Modulation

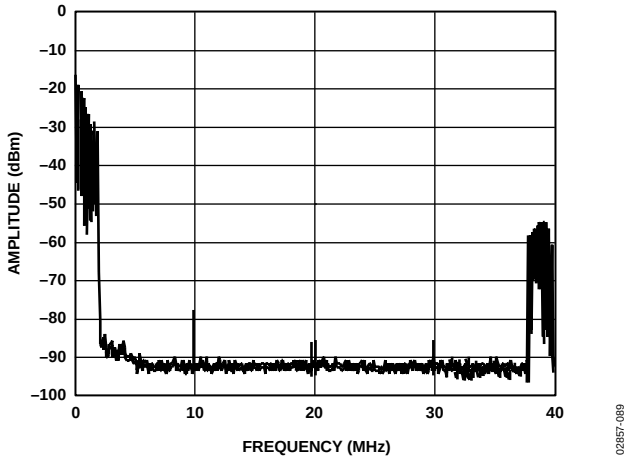


Figure 89. AD9773 Real DAC Output of Complex Input Signal Near Baseband (Positive Frequencies Only), Interpolation = 4x, No Modulation in AD9773

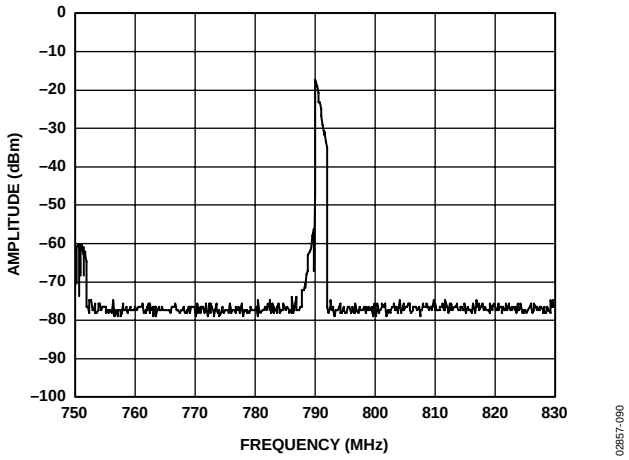


Figure 90. AD9773 Complex Output from Figure 89, Now Quadrature Modulated by AD8345 (LO = 800 MHz)

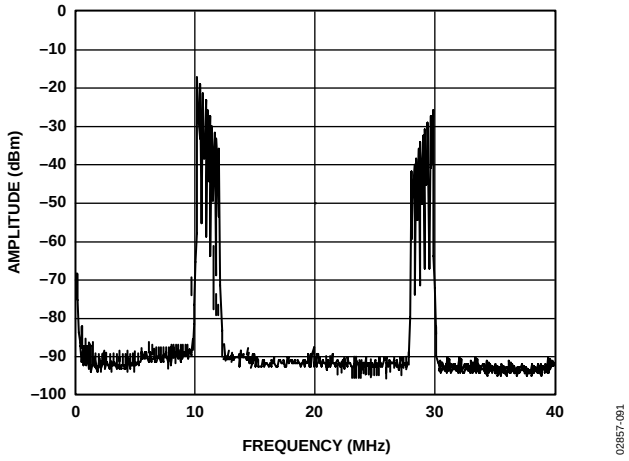


Figure 91. AD9773 Real DAC Output of Complex Input Signal Near Baseband (Positive Frequencies Only), Interpolation = 4x, Complex Modulation in AD9773 = $+f_{DAC}/4$

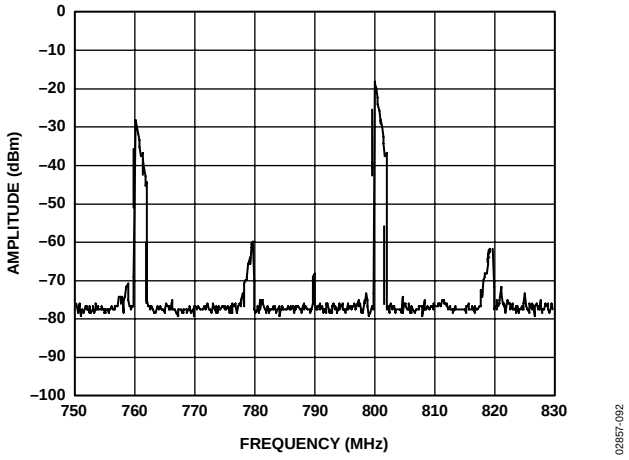


Figure 92. AD9773 Complex Output from Figure 91, Now Quadrature Modulated by AD8345 (LO = 800 MHz)

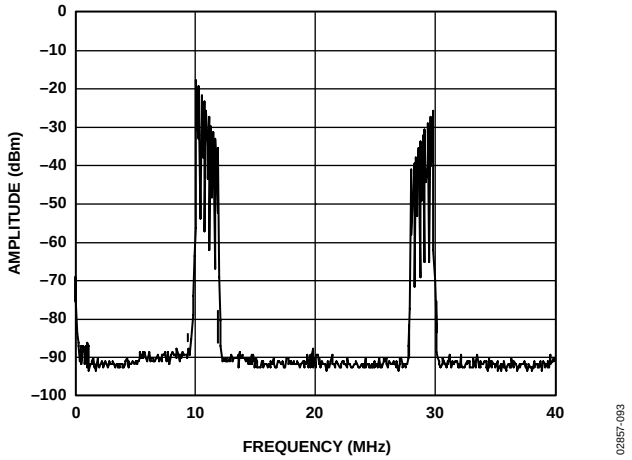


Figure 93. AD9773 Real DAC Output of Complex Input Signal Near Baseband (Negative Frequencies Only), Interpolation = 4x, Complex Modulation in AD9773 = $-f_{DAC}/4$

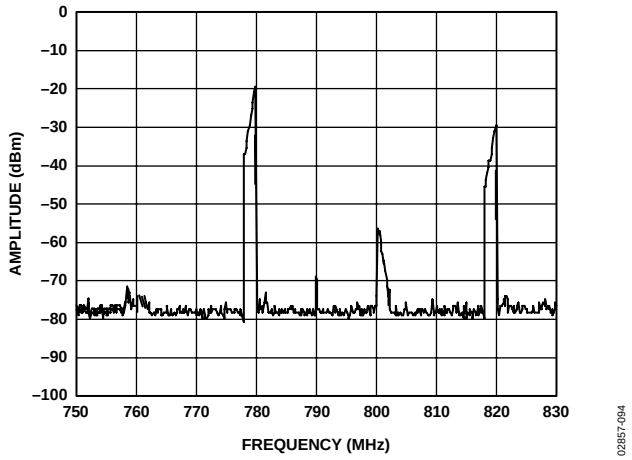


Figure 94. AD9773 Complex Output from Figure 93, Now Quadrature Modulated by AD8345 (LO = 800 MHz)

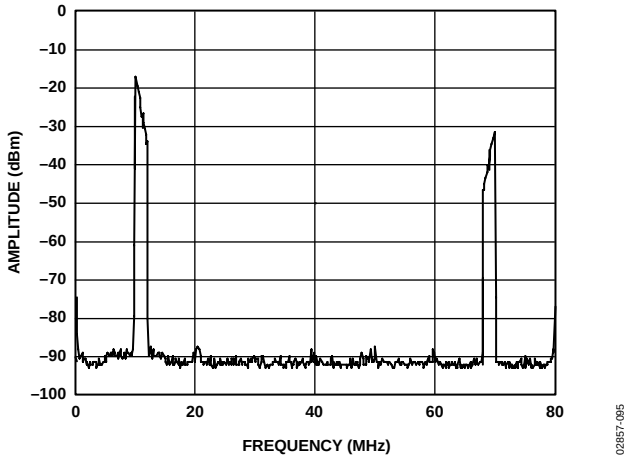


Figure 95. AD9773 Real DAC Output of Complex Input Signal Near Baseband (Positive Frequencies Only), Interpolation = 8x, Complex Modulation in AD9773 = $+f_{DAC}/8$

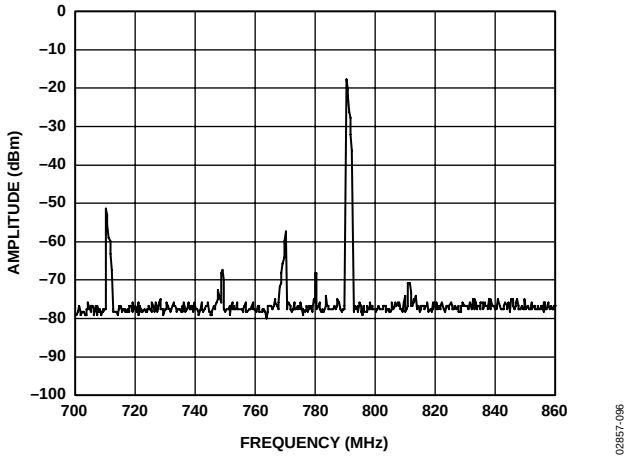


Figure 96. AD9773 Complex Output from Figure 95, Now Quadrature Modulated by AD8345 (LO = 800 MHz)

APPLYING THE OUTPUT CONFIGURATIONS

The following sections illustrate typical output configurations for the AD9773. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring optimum dynamic performance, a differential output configuration is suggested. A simple differential output can be achieved by converting I_{OUTA} and I_{OUTB} to a voltage output by terminating them to AGND via equal value resistors. This type of configuration may be useful when driving a differential voltage input device such as a modulator. If a conversion to a single-ended signal is desired and the application allows for ac coupling, an RF transformer may be useful, or if power gain is required, an op amp may be used. The transformer configuration provides optimum high frequency noise and distortion performance. The differential op amp configuration is suitable for applications requiring dc coupling, signal gain, and/or level shifting within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage results if I_{OUTA} and/or I_{OUTB} is connected to a load resistor, R_{LOAD}, referred to AGND. This configuration is most suitable for a single-supply system requiring a dc-coupled, ground-referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best DAC dc linearity as I_{OUTA} or I_{OUTB} are maintained at ground or virtual ground.

UNBUFFERED DIFFERENTIAL OUTPUT, EQUIVALENT CIRCUIT

In many applications, it may be necessary to understand the equivalent DAC output circuit. This is especially useful when designing output filters or when driving inputs with finite input impedances. Figure 97 illustrates the output of the AD9773 and the equivalent circuit. A typical application where this information may be useful is when designing an interface filter between the AD9773 and the Analog Devices AD8345 quadrature modulator.

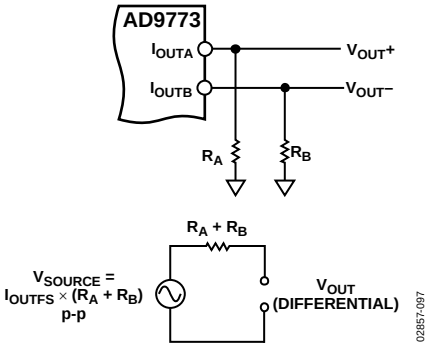


Figure 97. DAC Output Equivalent Circuit

For the typical situation, where I_{OUTFS} = 20 mA and R_A and R_B both equal 50 Ω, the equivalent circuit values become

V_{SOURCE} = 2 V p-p
R_{OUT} = 100 Ω

Note that the output impedance of the AD9773 DAC itself is greater than 100 kΩ and typically has no effect on the impedance of the equivalent output circuit.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 98. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's pass band. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (that is, even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes.

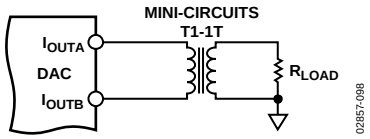


Figure 98. Transformer-Coupled Output Circuit

The center tap on the primary side of the transformer must be connected to AGND to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (that is, V_{OUTA} and V_{OUTB}) swing symmetrically around AGND and should be maintained within the specified output compliance range of the AD9773. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power dissipates across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion, as shown in Figure 99. This has the added benefit of providing signal gain as well. In Figure 99, the AD9773 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's fast slewing output from overloading the input of the op amp.

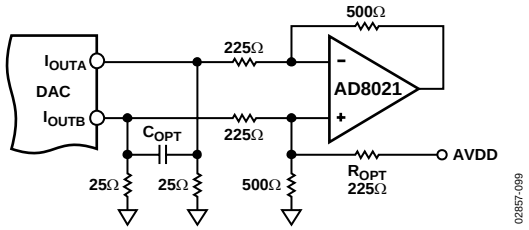


Figure 99. Op Amp-Coupled Output Circuit

The common-mode (and second-order distortion) rejection of this configuration is typically determined by the resistor matching. The op amp used must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier, such as the AD8021, capable of preserving the differential performance of the AD9773 while meeting other system level objectives (for example, cost, power) is recommended. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit. R_{OPT} is necessary only if level shifting is required on the op amp output. In Figure 99, AVDD, which is the positive analog supply for both the AD9773 and the op amp, is also used to level shift the differential output of the AD9773 to midsupply (for example, AVDD/2).

INTERFACING THE AD9773 WITH THE AD8345 QUADRATURE MODULATOR

The AD9773 architecture was defined to operate in a transmit signal chain using an image reject architecture. A quadrature modulator is also required in this application and should be designed to meet the output characteristics of the DAC as much as possible. The AD8345 from Analog Devices meets many of the requirements for interfacing with the AD9773. As with any DAC output interface, there are a number of issues that have to be resolved. The following sections list some of these major issues.

DAC Compliance Voltage/Input Common-Mode Range

The dynamic range of the AD9773 is optimal when the DAC outputs swing between ±1.0 V. The input common-mode range of the AD8345, at 0.7 V, allows optimum dynamic range to be achieved in both components.

Gain/Offset Adjust

The matching of the DAC output to the common-mode input of the AD8345 allows the two components to be dc-coupled, with no level shifting necessary. The combined voltage offset of the two parts can therefore be compensated via the AD9773 programmable offset adjust. This allows excellent LO cancellation at the AD8345 output. The programmable gain adjust allows for optimal image rejection as well.

The AD9773 evaluation board includes an AD8345 and recommended interface (Figure 105 and Figure 106). On the output of the AD9773, R9 and R10 convert the DAC output current to a voltage. R16 may be used to execute a slight common-mode shift if necessary. The (now voltage) signal is applied to a low-pass reconstruction filter to reject DAC images. The components installed on the AD9773 provide a 35 MHz cutoff but may be changed to fit the application. A balun (Mini-Circuits ADTL1-12) is used to cross the ground plane boundary to the AD8345. Another balun (Mini-Circuits ETC1-1-13) is used to couple the LO input of the AD8345. The interface requires a low ac impedance return path from the AD8345, so a single connection between the AD9773 and AD8345 ground planes is recommended.

The performance of the AD9773 and AD8345 in an image reject transmitter, reconstructing three WCDMA carriers, can be seen in Figure 100. The LO of the AD8345 in this application is 800 MHz. Image rejection (50 dB) and LO feedthrough (−78 dBFS) have been optimized with the programmable features of the AD9773. The average output power of the digital waveform for this test was set to −15 dBFS to account for the peak-to-average ratio of the WCDMA signal.

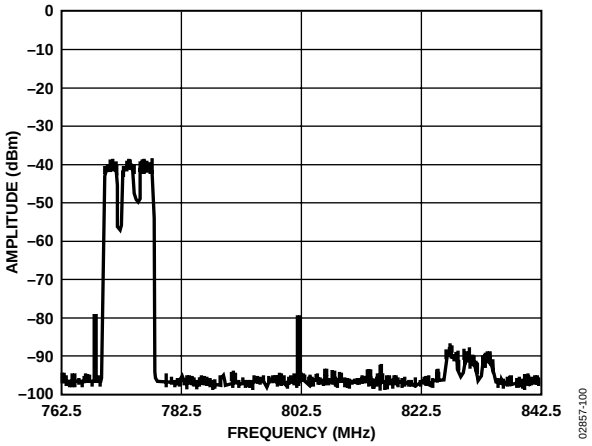


Figure 100. AD9773/AD8345 Synthesizing a Three-Carrier WCDMA Signal at an LO of 800 MHz

EVALUATION BOARD

The AD9773 evaluation board allows easy configuration of the various modes, programmable via the SPI port. Software is available for programming the SPI port from Windows 95®, Windows 98®, or Windows NT®/2000. The evaluation board also contains an AD8345 quadrature modulator and support circuitry that allows the user to optimally configure the AD9773 in an image reject transmit signal chain.

Figure 101 through Figure 104 describe how to configure the evaluation board in the one-port and two-port input modes with the PLL enabled and disabled. Refer to Figure 105 through Figure 114, the schematics, and the layout for the AD9773 evaluation board for the jumper locations described below. The AD9773 outputs can be configured for various applications by referring to the following instructions.

DAC SINGLE-ENDED OUTPUTS

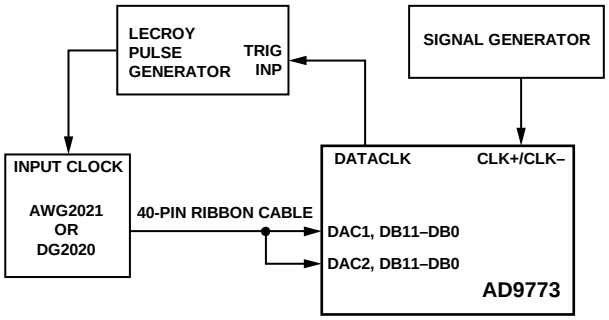
Remove transformers T2 and T3. Solder jumper link JP4 or JP28 to look at the DAC1 outputs. Solder jumper link JP29 or JP30 to look at the DAC2 outputs. Jumper 8 and Jumpers 13 to 17 should remain unsoldered. Jumpers JP35 to JP38 may be used to ground one of the DAC outputs while the other is measured single-ended. Optimum single-ended distortion performance is typically achieved in this manner. The outputs are taken from S3 and S4.

DAC DIFFERENTIAL OUTPUTS

Transformers T2 and T3 should be in place. Note that the lower band of operation for these transformers is 300 kHz to 500 kHz. Jumpers 4, 8, 13 to 17, and 28 to 30 should remain unsoldered. The outputs are taken from S3 and S4.

USING THE AD8345

Remove Transformers T2 and T3. Jumpers JP4 and Jumpers 28 to 30 should remain unsoldered. Jumpers 13 to 16 should be soldered. The desired components for the low-pass interface filters L6, L7, C55, and C81 should be in place. The LO drive is connected to the AD8345 via J10 and the balun T4; AD8345 output is taken from J9.



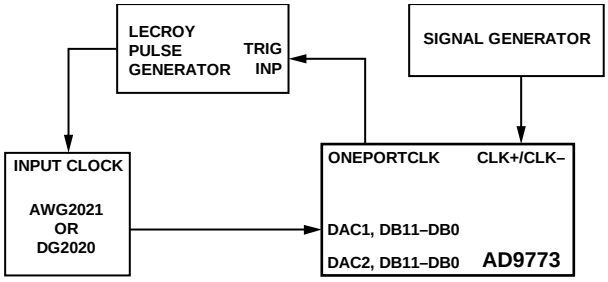
JUMPER CONFIGURATION FOR TWO-PORT MODE, PLL ON

	SOLDERED/IN	UNSOLDERED/OUT
JP1 –	×	
JP2 –		×
JP3 –	×	
JP5 –	×	
JP6 –		×
JP12 –		×
JP24 –		×
JP25 –	×	
JP26 –	×	
JP27 –		×
JP31 –		×
JP32 –		×
JP33 –		×

NOTES
1. TO USE PECL DRIVER (U8), SOLDER JP41 AND JP42 AND REMOVE TRANSFORMER T1.
2. IN TWO-PORT MODE, IF DATACLK/PLL_LOCK IS PROGRAMMED TO OUTPUT PIN 8, JP25 AND JP39 SHOULD BE SOLDERED. IF DATACLK/PLL_LOCK IS PROGRAMMED TO OUTPUT PIN 53, JP46 AND JP47 SHOULD BE SOLDERED. FOR MORE INFORMATION, SEE THE TWO-PORT DATA INPUT MODE SECTION.

02857-101

Figure 101. Test Configuration for AD9773 in Two-Port Mode with PLL Enabled, Signal Generator Frequency = Input Data Rate, DAC Output Data Rate = Signal Generator Frequency × Interpolation Rate



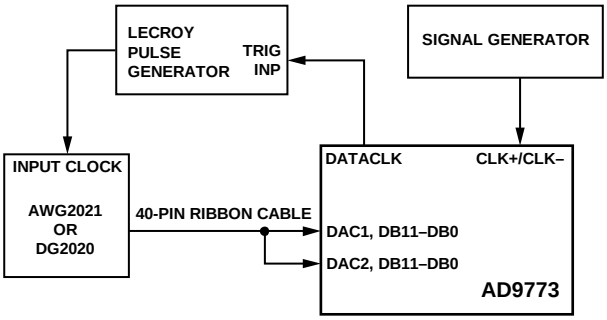
JUMPER CONFIGURATION FOR ONE-PORT MODE, PLL ON

	SOLDERED/IN	UNSOLDERED/OUT
JP1 –	×	
JP2 –		×
JP3 –	×	
JP5 –		×
JP6 –		×
JP12 –		×
JP24 –		×
JP25 –	×	
JP26 –		×
JP27 –	×	
JP31 –	×	
JP32 –		×
JP33 –		×

NOTES
1. TO USE PECL DRIVER (U8), SOLDER JP41 AND JP42 AND REMOVE TRANSFORMER T1.

02857-102

Figure 102. Test Configuration for AD9773 in One-Port Mode with PLL Enabled, Signal Generator Frequency = One-Half Interleaved Input Data Rate, ONEPORTCLK = Interleaved Input Data Rate, DAC Output Data Rate = Signal Generator Frequency × Interpolation Rate



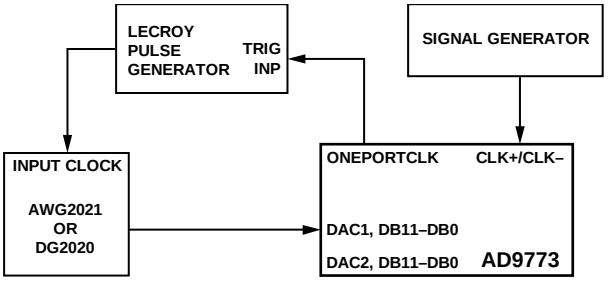
JUMPER CONFIGURATION FOR TWO-PORT MODE, PLL OFF

	SOLDERED/IN	UNSOLDERED/OUT
JP1 –	×	
JP2 –		×
JP3 –	×	
JP5 –	×	
JP6 –		×
JP12 –		×
JP24 –		×
JP25 –	×	
JP26 –	×	
JP27 –		×
JP31 –		×
JP32 –		×
JP33 –		×

NOTES
1. TO USE PECL DRIVER (U8), SOLDER JP41 AND JP42 AND REMOVE TRANSFORMER T1.
2. IN TWO-PORT MODE, IF DATACLK/PLL_LOCK IS PROGRAMMED TO OUTPUT PIN 8, JP25 AND JP39 SHOULD BE SOLDERED. IF DATACLK/PLL_LOCK IS PROGRAMMED TO OUTPUT PIN 53, JP46 AND JP47 SHOULD BE SOLDERED. FOR MORE INFORMATION, SEE THE TWO-PORT DATA INPUT MODE SECTION.

02857-103

Figure 103. Test Configuration for AD9773 in Two-Port Mode with PLL Disabled, DAC Output Data Rate = Signal Generator Frequency, DATACLK = Signal Generator Frequency/Interpolation Rate



JUMPER CONFIGURATION FOR ONE-PORT MODE, PLL OFF

	SOLDERED/IN	UNSOLDERED/OUT
JP1 –	×	
JP2 –		×
JP3 –	×	
JP5 –		×
JP6 –		×
JP12 –		×
JP24 –		×
JP25 –	×	
JP26 –		×
JP27 –	×	
JP31 –	×	
JP32 –		×
JP33 –		×

NOTES
1. TO USE PECL DRIVER (U8), SOLDER JP41 AND JP42 AND REMOVE TRANSFORMER T1.

02857-104

Figure 104. Test Configuration for AD9773 in One-Port Mode with PLL Disabled, DAC Output Data Rate = Signal Generator Frequency, ONEPORTCLK = Interleaved Input Data Rate = 2x Signal Generator Frequency/Interpolation Rate

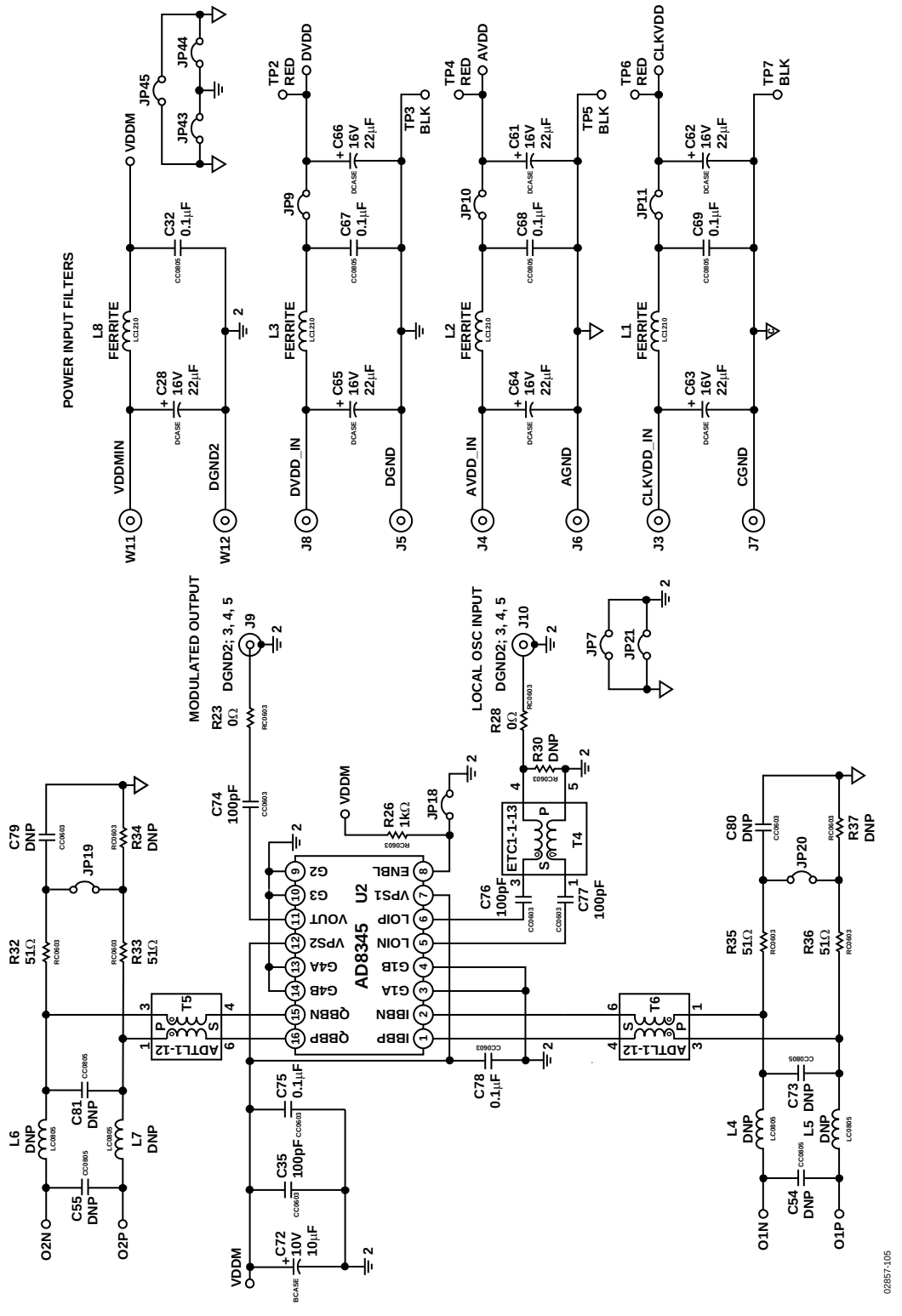


Figure 105. AD8345 Circuitry on AD9773 Evaluation Board

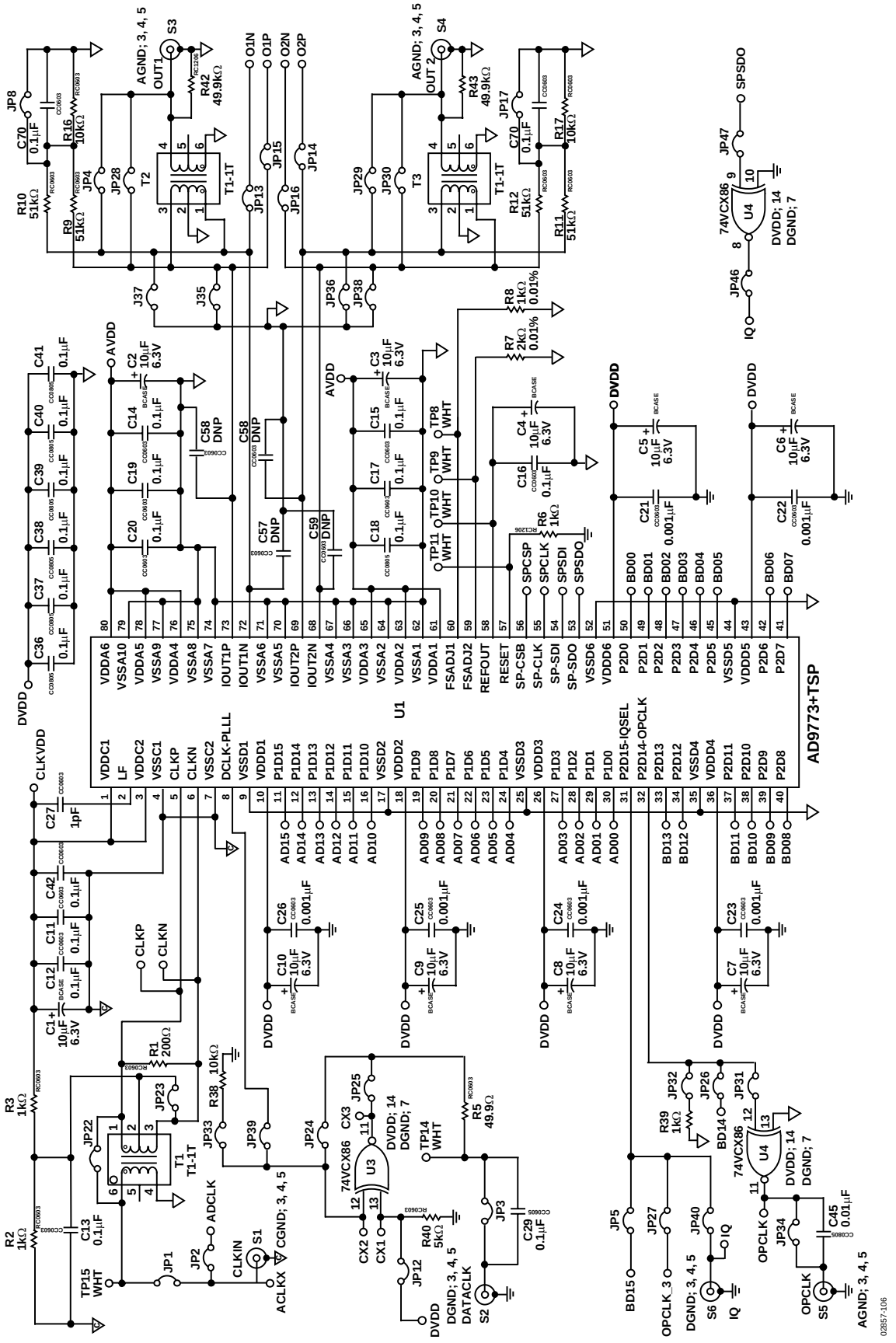
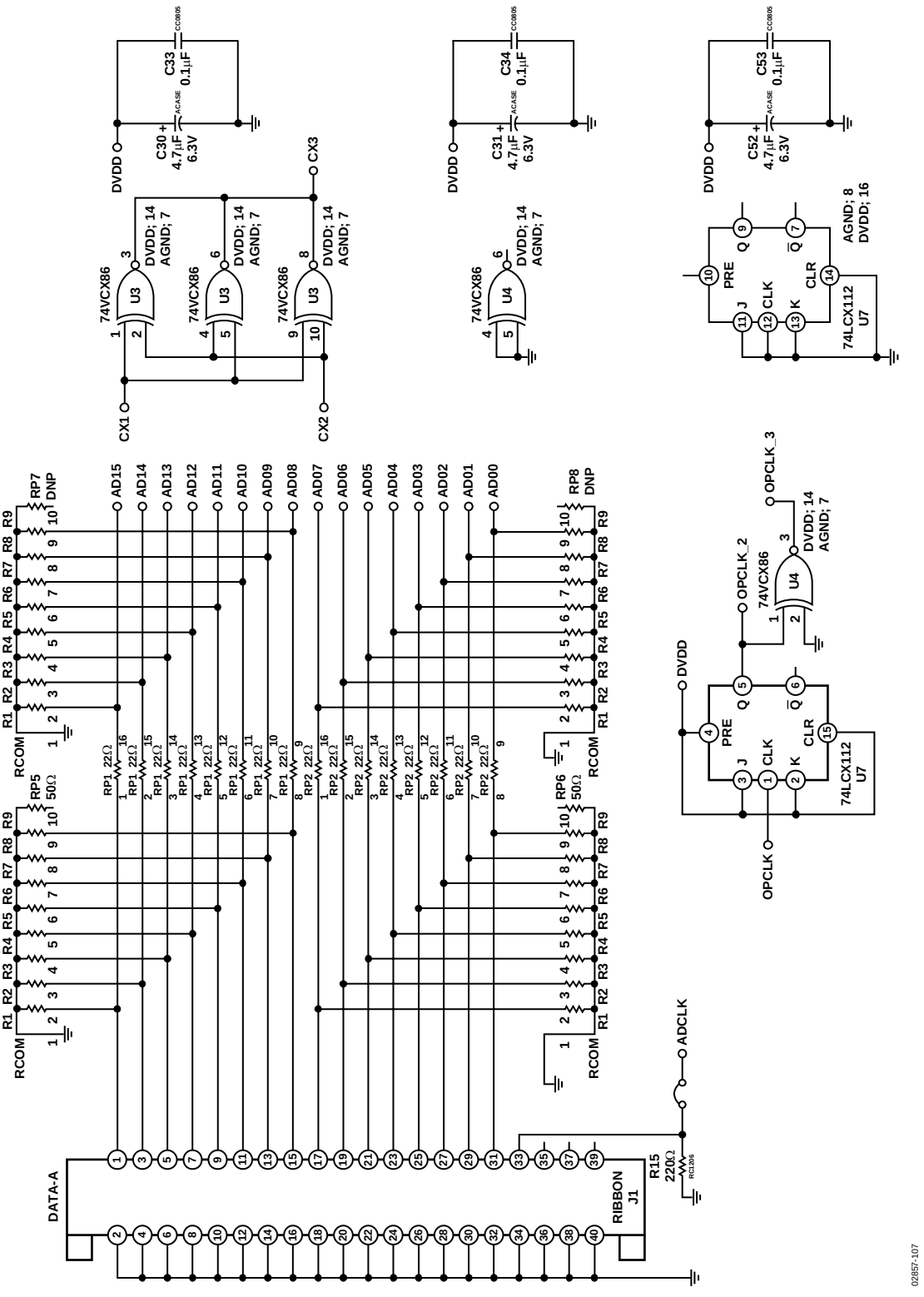


Figure 106. AD9773 Clock, Power Supplies, and Output Circuitry



02857-107

Figure 107. AD9773 Evaluation Board Input (A Channel) and Clock Buffer Circuitry

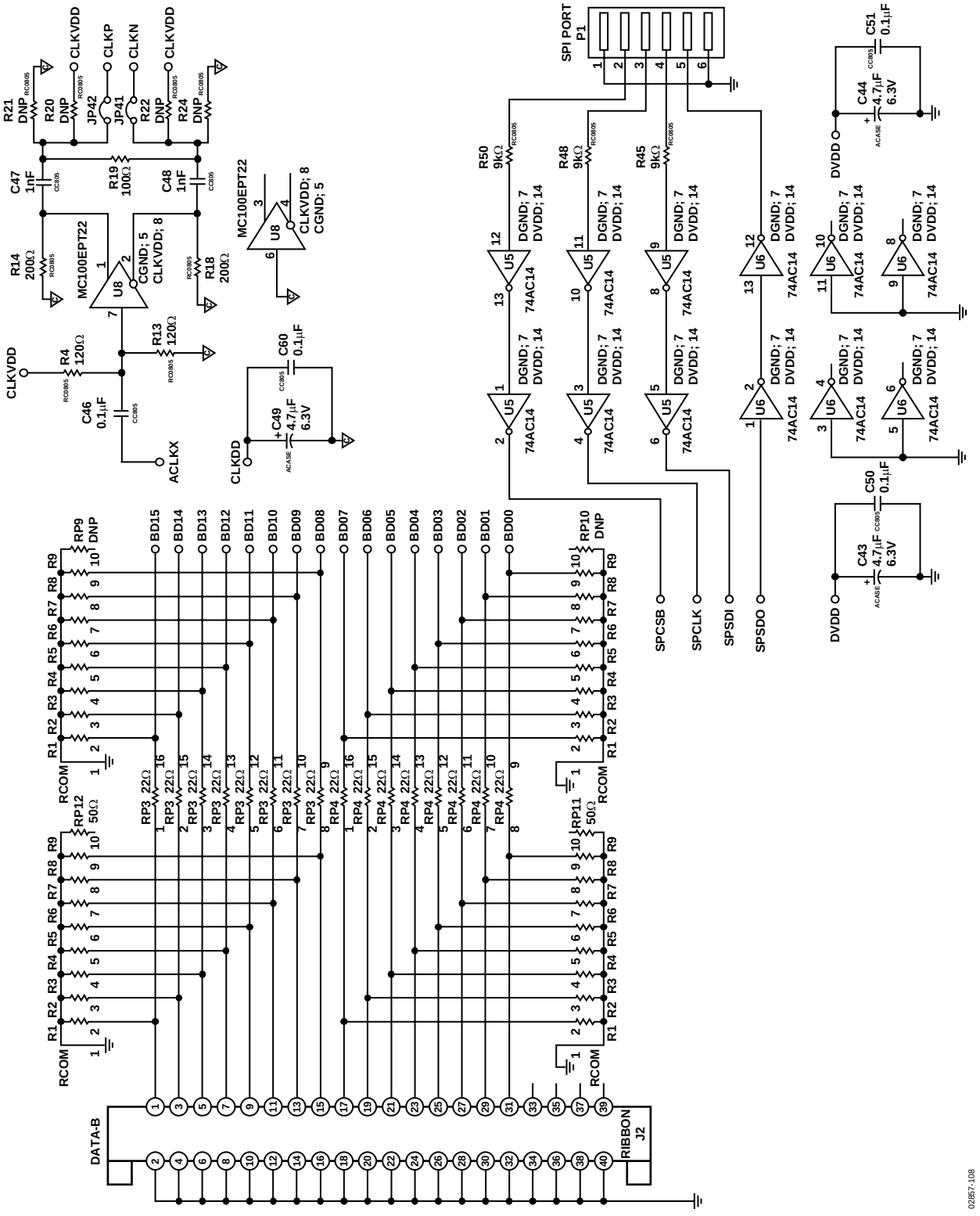


Figure 108. AD9773 Evaluation Board Input (B Channel) and SPI Port Circuitry

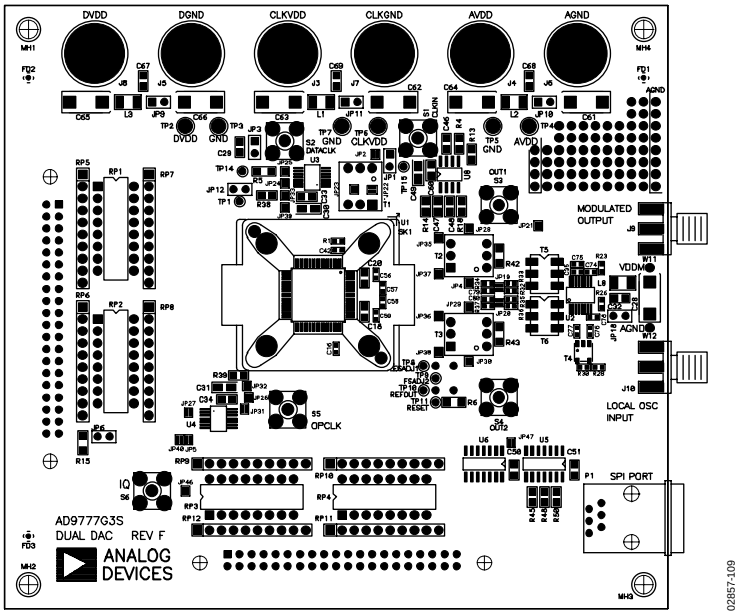


Figure 109. AD9773 Evaluation Board Components, Top Side

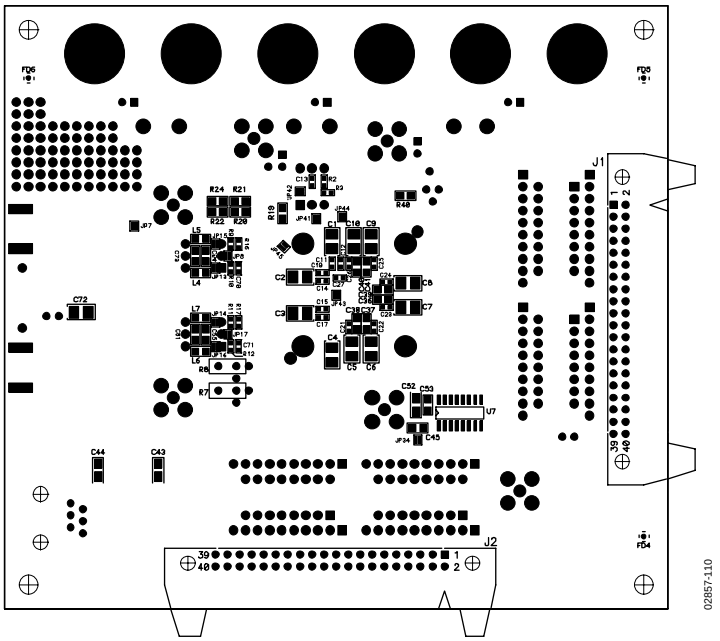


Figure 110. AD9773 Evaluation Board Components, Bottom Side

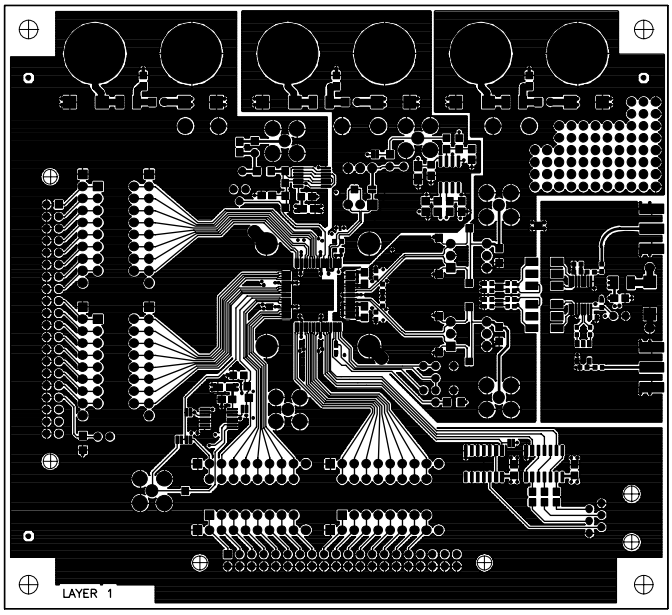


Figure 111. AD9773 Evaluation Board Layout, Layer One (Top)

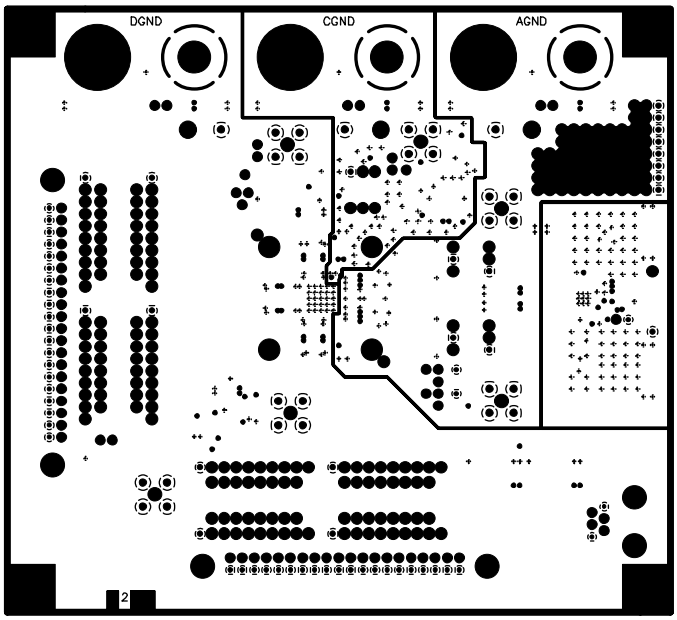


Figure 112. AD9773 Evaluation Board Layout, Layer Two (Ground Plane)

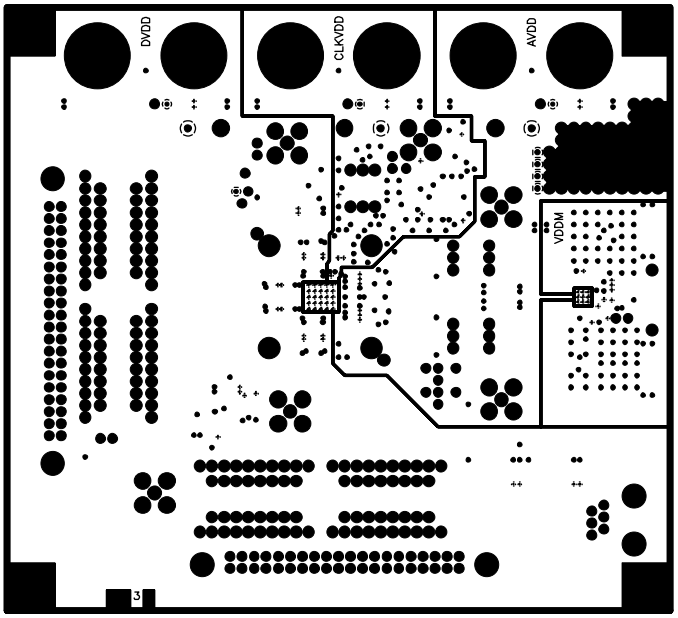


Figure 113. AD9773 Evaluation Board Layout, Layer Three (Power Plane)

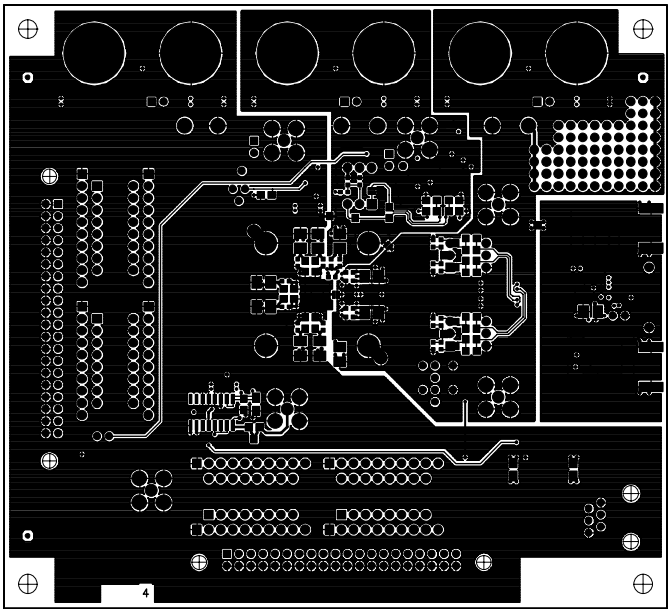


Figure 114. AD9773 Evaluation Board Layout, Layer Four (Bottom)

OUTLINE DIMENSIONS

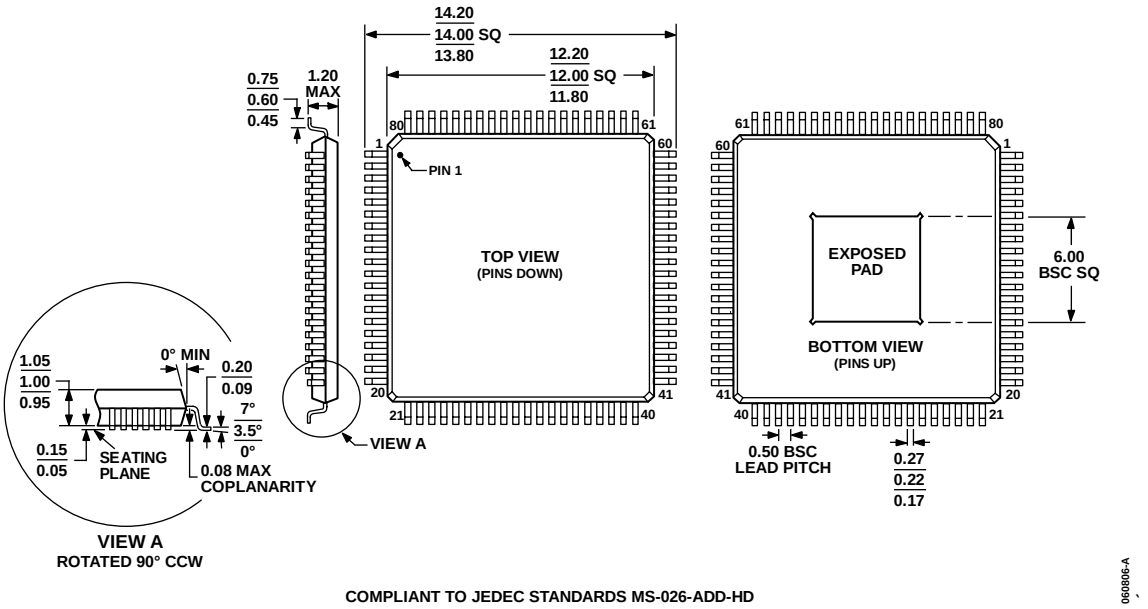


Figure 115. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9773BSV	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-1
AD9773BSVRL	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-1
AD9773BSVZ[1]	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-1
AD9773BSVZRL[1]	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-1
AD9773-EB		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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