Automotive uPOL MODUL

2A, High Efficiency uPOL Module

VUN12AD02-KM

FEATURES:

- High Density Fully Integration Module
- Maximum Output Current: 2A
- Input Voltage Range from 4V to 36V
- Output Voltage Range from 0.9V to 8V
- VIN Maximum Rating 42V
- Switching Frequency 430kHz
- Approaching 100% duty cycle
- Selectable PSM/FPWM at Light Load
- Enable Function
- Protections (UVLO, OTP, OCP:non-latching)
- Power Good Indicator
- Selectable Spread Spectrum Frequency
- Wettable Flank Packaging
- Compact Size: 6mm*6mm*3.5mm
- Pb-free for RoHS compliant
- MSL 2, 260C Reflow
- AECQ-100 certificate

GENERAL DESCRIPTION:

The uPOL Module is non-isolated dc-dc converter that can deliver up to 2A. The PWM switching regulator and high frequency power inductor are integrated in one hybrid package.

Some features can be adjusted by external pin include output voltage, soft-start time, non-latching over current protection, and selectable spread spectrum frequency modulation. Other features include enable function, power good indicator, and input under voltage locked-out capability.

The low profile and compact size package (6.0mm × 6.0mm x 3.5 mm) is suitable for automated assembly by standard surface mount equipment. The wettable flank packaging is available. The uPOL module is Pb-free and RoHS compliance.

APPLICATIONS:

- Automotive LED Lighting
- Instrument Cluster
- ADAS
- Infotainment

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

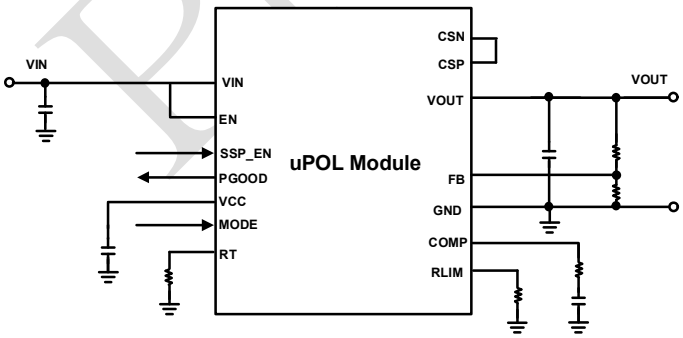


FIGURE.1 TYPICAL APPLICATION CIRCUIT

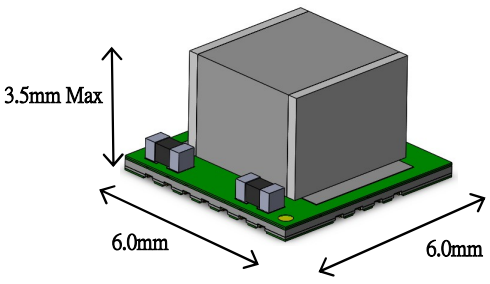


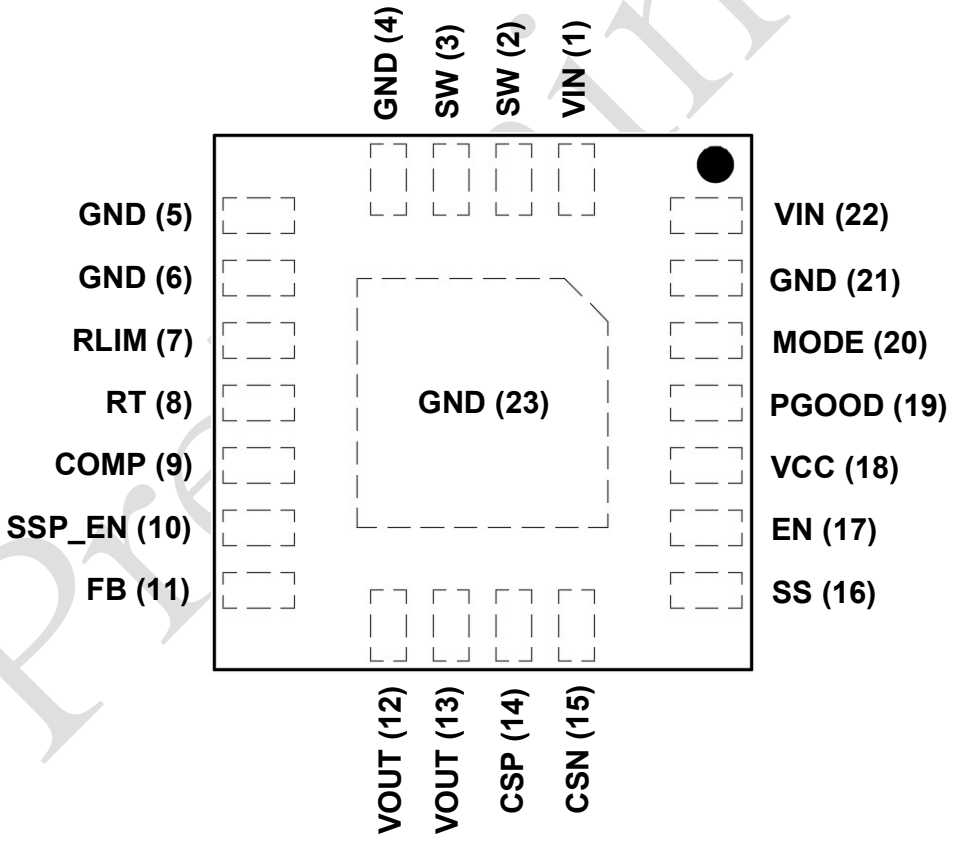
FIGURE.2 HIGH DENSITY uPOL MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
VUN12AD02-KM	-40 ~ +125	QFN	Level 2	-

Order Code	Packing	Quantity
VUN12AD02-KM	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

PIN CONFIGURATION:

Symbol	Pin No.	Description
VIN	1, 22	Power input pin.
SW	2, 3	Switch node.
GND	4, 5, 6, 21, 23	Power ground.
RLIM	7	Current limit setup pin.
RT	8	Switching frequency 430kHz with 120kohm setting
COMP	9	Compensation node.
SSP_EN	10	Spread spectrum enable input. Connect this pin to VCC to enable spread spectrum. Connect to ground to disable spread spectrum.
FB	11	Feedback voltage input.
VOUT	12, 13	Power output pin.
CSP	14	Must connect CSN to CSP short circuit directly
CSN	15	Must connect CSN to CSP short circuit directly
SS	16	Soft start pin
EN	17	Enable control input. A logic-high enables the converter; a logic-low disables the device into shutdown mode.
VCC	18	Linear regulator output. Add a 10uF, X7R ceramic capacitor from VCC to ground.
PGOOD	19	Open-drain power-good indication output.
MODE	20	Connect this pin to ground to enable power saving mode (PSM). Connect this pin to VCC to enable force PWM mode (FPWM).

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN, SW, EN, CSP, CSN		-0.3	-	42	V
Others		-0.3	-	6	V
Tc	Case Temperature of Inductor	-40	-	+150	°C
Tj	Junction Temperature, Main IC	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+150	°C
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.0	-	+36	V
VOUT	Adjuested Output Voltage	+0.9	-	+8	V
Ta	Ambient Tamperture	-40	-	+125	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient. (Note 1)	-	29.5	-	°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers 2oz. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN = 12V, VOUT = 5V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/16V/1210/X7R x 2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
V_{UVLO_TH}	VIN under voltage lockout threshold	VIN rising	-	3.8	-	V
$V_{UVLO\_TH\_HY}$	VIN under voltage lockout hysteresis		-	900	-	mV
$I_{S(IN)}$	Shutdown Current	VEN=0V	-	1.3	-	uA
$I_{Q1(IN)}$	Quiescent Current	VEN=2V, VFB = 0.82V, not switching	-	37	-	uA
$I_{Q2(IN)}$	Quiescent Current	VEN=2V, VOUT=5V, Load=0A, switching, MODE=VCC (FPWM)	-	12	-	mA
$I_{Q3(IN)}$	Quiescent Current	VEN=2V, VOUT=5V, Load=0A, switching, MODE=GND (PSM)	-	70	-	uA
■ Output Characteristics						
V_{FB}	Feedback Voltage	T_A = 25 ºC	0.792	0.8	0.808	V
V_{SW}	Switching Frequency	RT=120kΩ	-	430	-	kHz
SS	Frequency spread spectrum Range	Connect SSP_EN pin to VCC	-	6	-	%
I_{LIM}	High side switch current limit	RLIM=56kΩ	-	3.4	-	A
D_{min}	Minimum Duty Cycle	VOUT/VIN	-	4	-	%
V_{PGLH1_TH}	Power Good	VFB rising, PGOOD low to high	-	90	-	% V_{FB}
V_{PGHL1_TH}	Power Good	VFB rising, PGOOD high to low	-	120	-	% V_{FB}
V_{PGHL2_TH}	Power Good	VFB falling, PGOOD high to low	-	85	-	% V_{FB}
V_{PGLH2_TH}	Power Good	VFB falling, PGOOD low to high	-	117	-	% V_{FB}

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN = 12V, VOUT = 5V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/16V/1210/X7R x 2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
$V_{EN\_TH\_R}$	Rising threshold voltage		1.5	-	-	V
$V_{EN\_TH\_F}$	Falling threshold voltage		-	-	0.8	V
■ Fault Protection						
T_{OTP}	Over temperature protection		-	175	-	℃
T_{OTP_HY}	Over tempeerature protection Hysteresis		-	15	-	℃

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

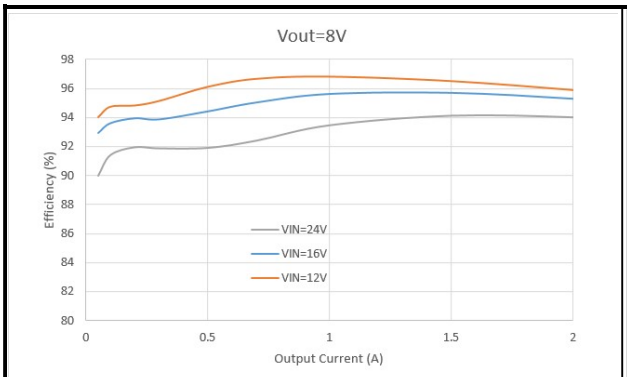


FIG.3 PSM EFFICIENCY V.S. Loading (VOUT=8V, IOUT=0 to 2A)

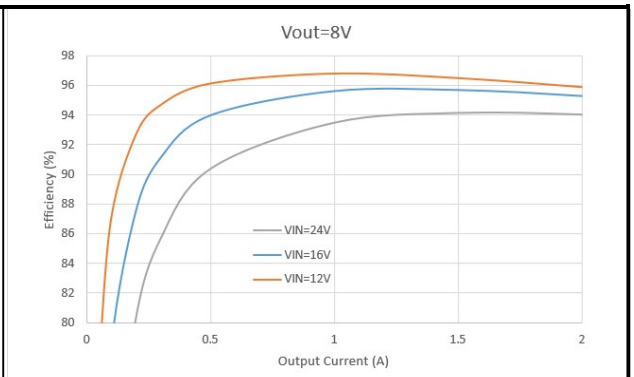


FIG.4 FPWM EFFICIENCY V.S. Loading (VOUT=8V, IOUT=0 to 2A)

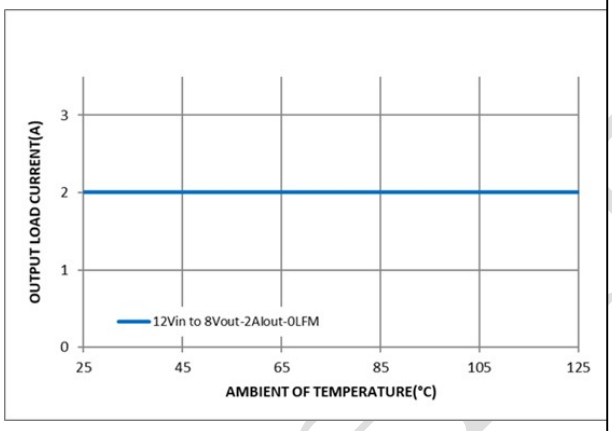


FIG.5 De-rating Curve (VIN=12V, VOUT=8V, IOUT=2A)

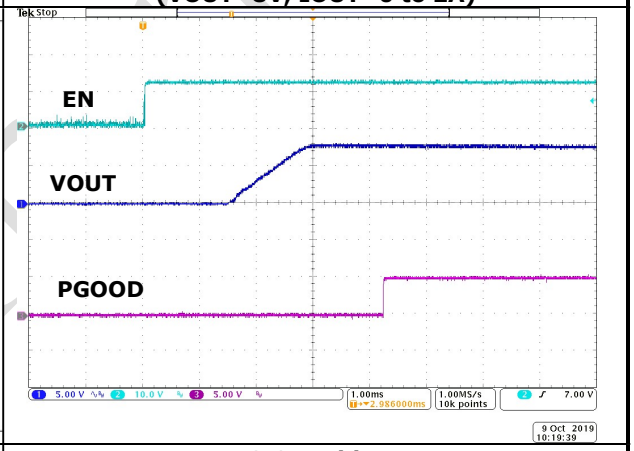


FIG.6 Enable on (VIN=12V, VOUT=8V, IOUT=0A)

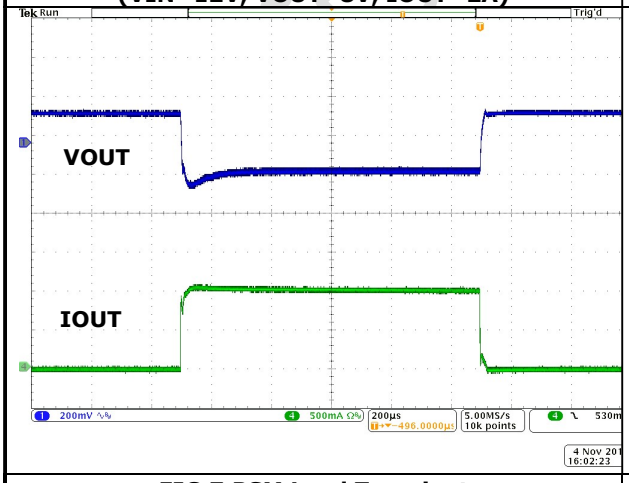


FIG.7 PSM Load Transient (VIN=12V, VOUT=8V, IOUT=0A to 1A)

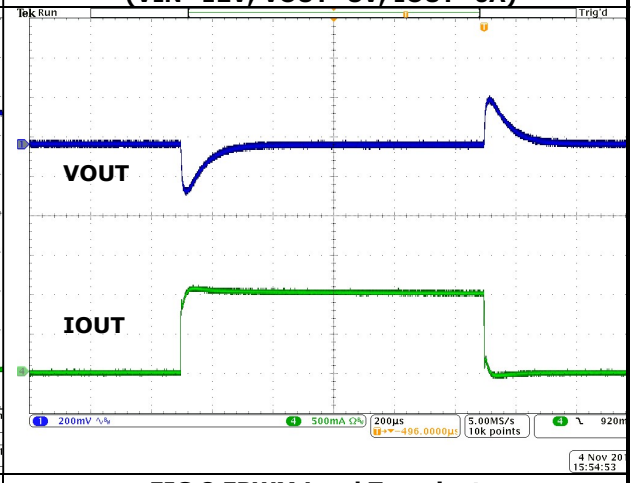


FIG.8 FPWM Load Transient (VIN=12V, VOUT=8V, IOUT=0A to 1A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

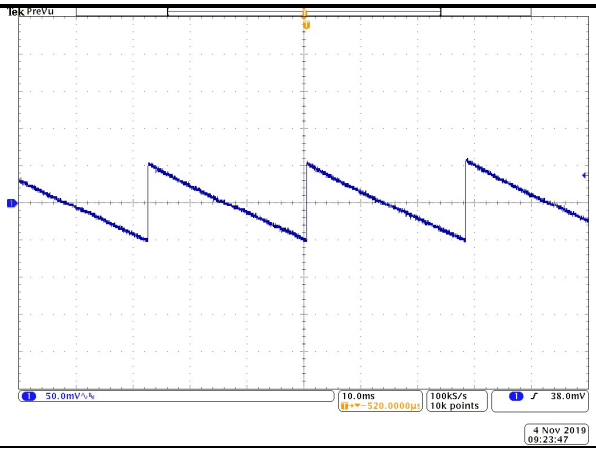


FIG.9 PSM VOUT Ripple
(VIN=12V, VOUT=8V, IOUT=0A)

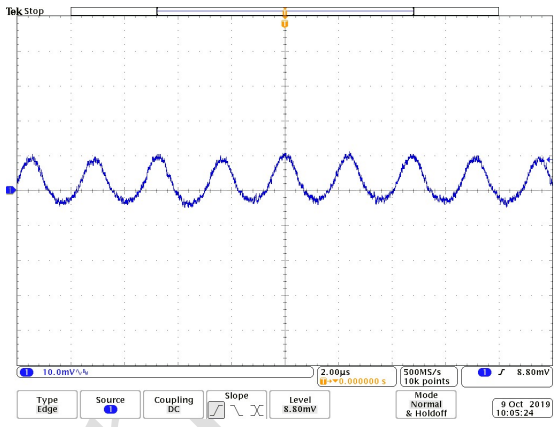


FIG.10 FPWM VOUT Ripple
(VIN=12V, VOUT=8V, IOUT=0A)

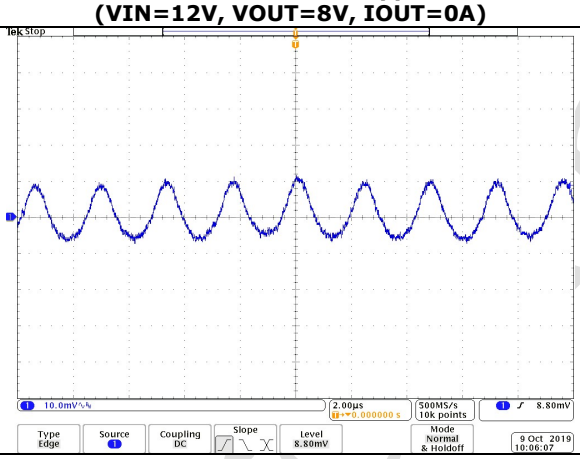


FIG.11 FPWM VOUT Ripple
(VIN=12V, VOUT=8V, IOUT=2A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

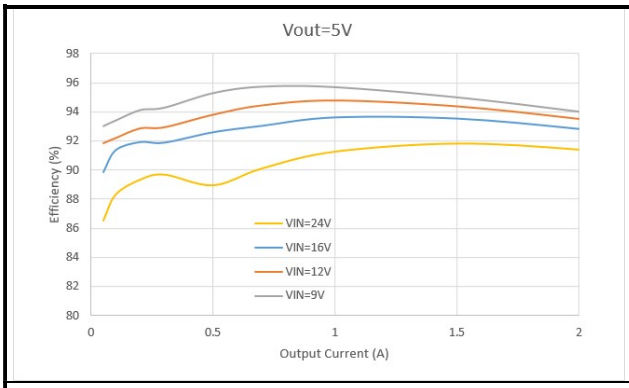


FIG.12 PSM EFFICIENCY V.S. Loading (VOUT=5V, IOUT=0 to 2A)

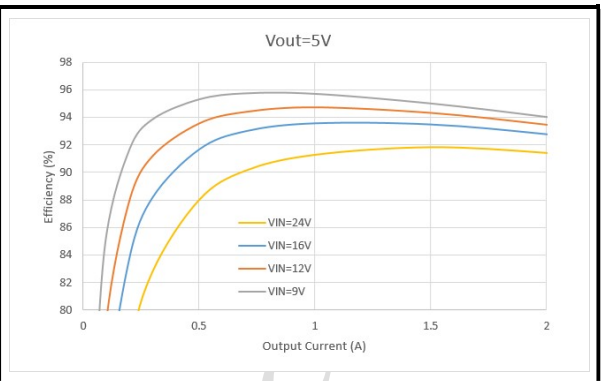


FIG.13 FPWM EFFICIENCY V.S. Loading (VOUT=5V, IOUT=0 to 2A)

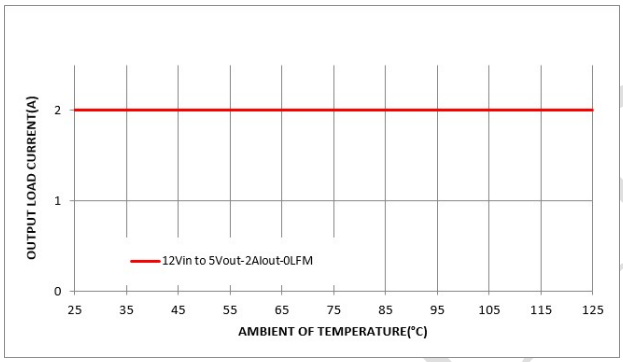


FIG.14 De-rating Curve (VIN=12V, VOUT=5V, IOUT=2A)

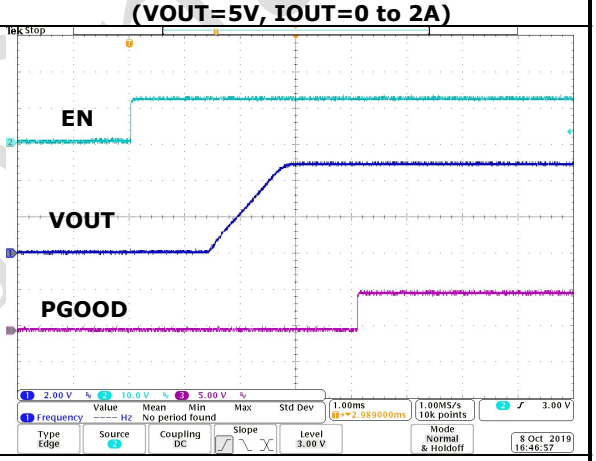


FIG.15 Enable on (VIN=12V, VOUT=5V, IOUT=0A)

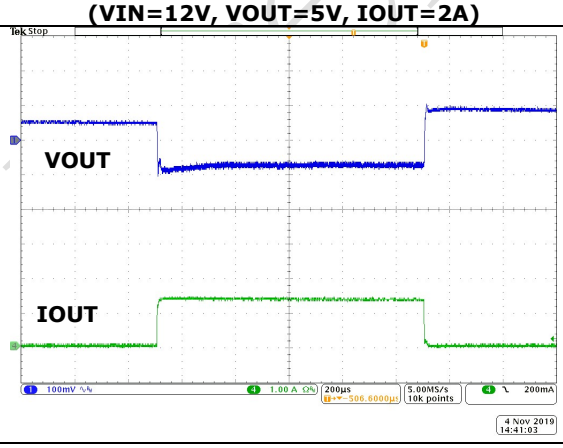


FIG.16 PSM Load Transient (VIN=12V, VOUT=5V, IOUT=0A to 1.5A)

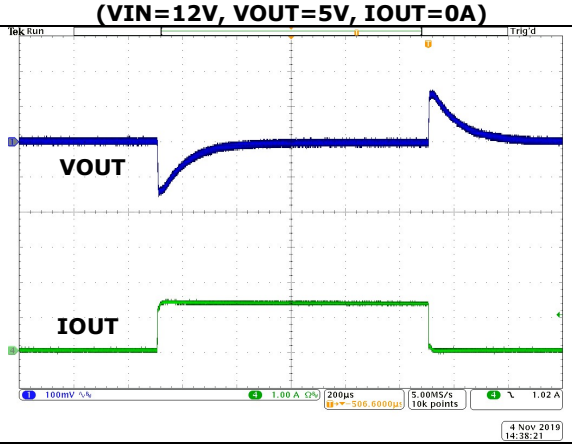


FIG.17 FPWM Load Transient (VIN=12V, VOUT=5V, IOUT=0A to 1.5A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

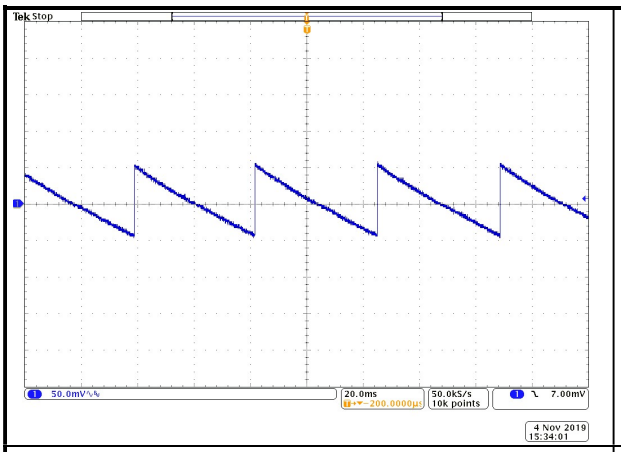


FIG.18 PSM VOUT Ripple
(VIN=12V, VOUT=5V, IOUT=0A)

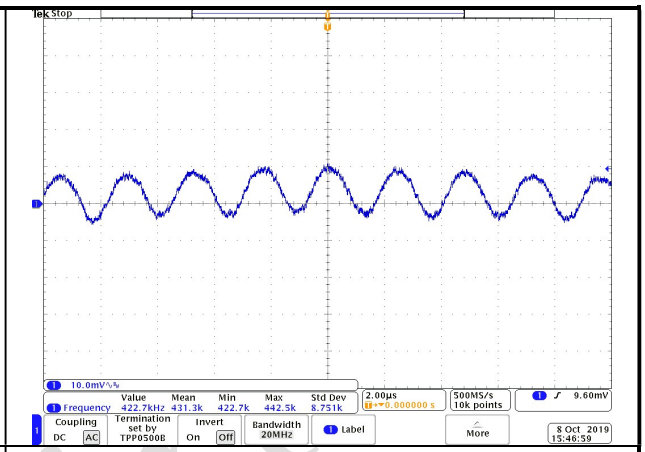


FIG.19 FPWM VOUT Ripple
(VIN=12V, VOUT=5V, IOUT=0A)

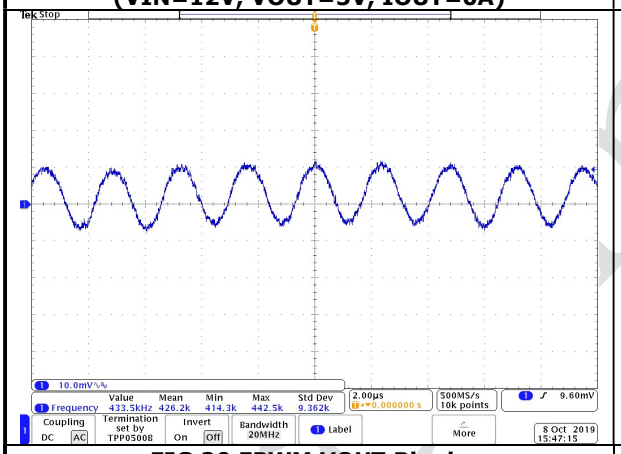


FIG.20 FPWM VOUT Ripple
(VIN=12V, VOUT=5V, IOUT=2A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

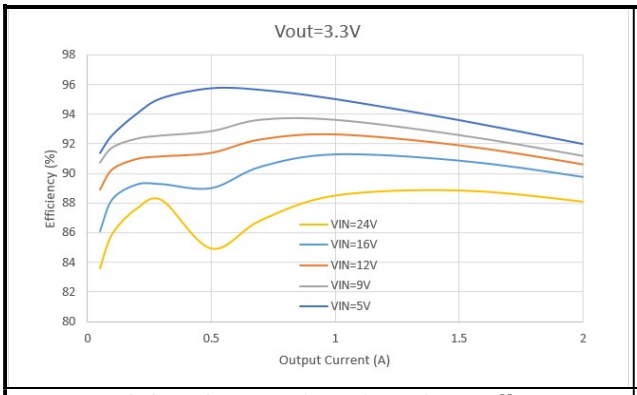


FIG.21 PSM EFFICIENCY V.S. Loading
(VOUT=3.3V, IOUT=0 to 2A)

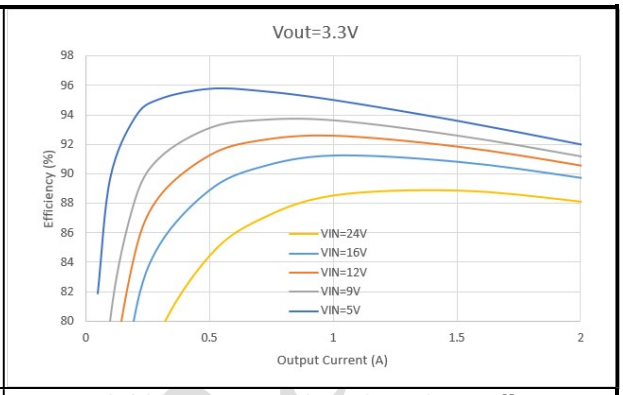


FIG.22 FPWM EFFICIENCY V.S. Loading
(VOUT=3.3V, IOUT=0 to 2A)

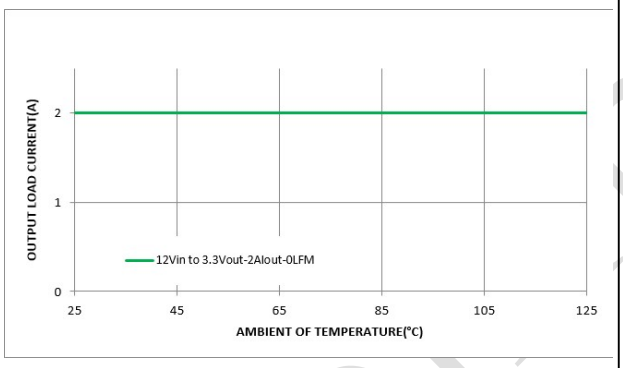


FIG.23 De-rating Curve
(VIN=12V, VOUT=3.3V, IOUT=2A)

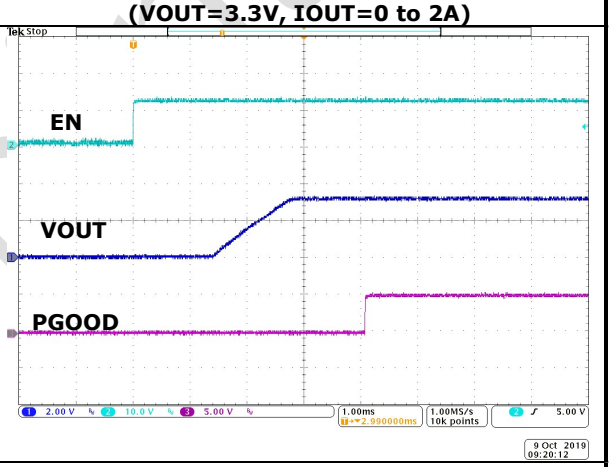


FIG.24 Enable on
(VIN=12V, VOUT=3.3V, IOUT=0A)

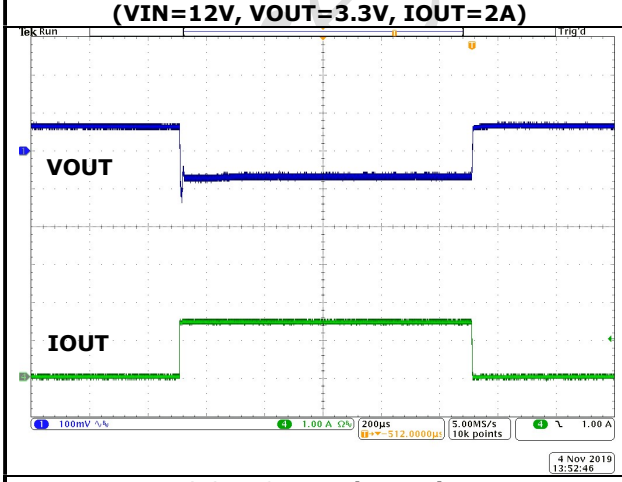


FIG.25 PSM Load Transient
(VIN=12V, VOUT=3.3V, IOUT=0A to 1.5A)

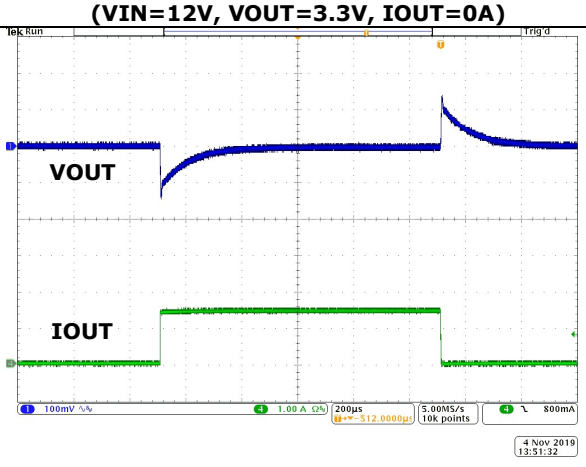


FIG.26 FPWM Load Transient
(VIN=12V, VOUT=3.3V, IOUT=0A to 1.5A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 4 layers 2oz.
VIN = 12V, Cin =4.7uF/50V/1206/X7R x 2, Cout = 22uF/50V/1210/X7R x 2.

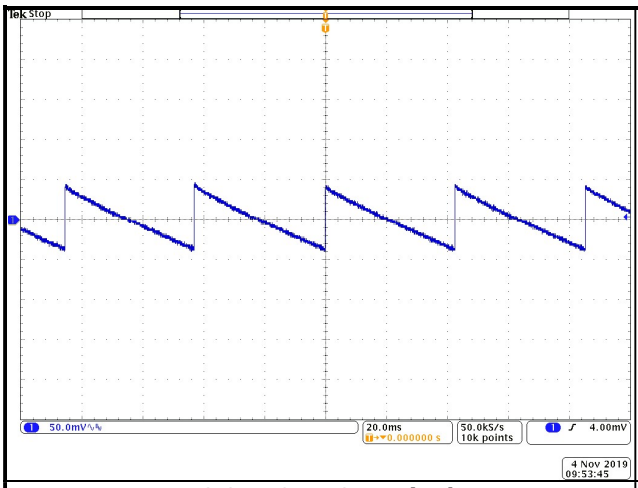


FIG.27 PSM VOUT Ripple
(VIN=12V, VOUT=3.3V, IOUT=0A)

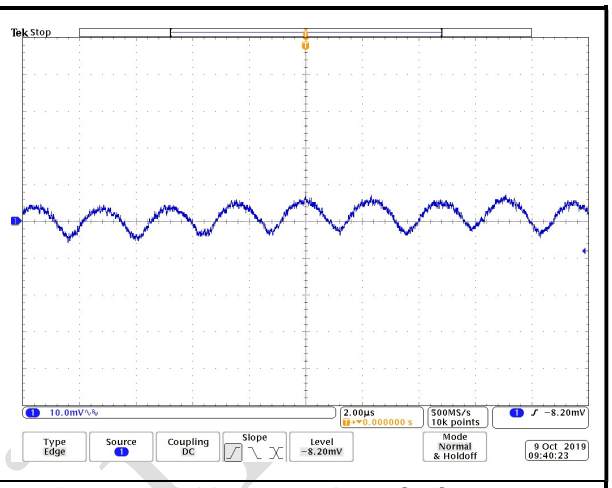


FIG.28 FPWM VOUT Ripple
(VIN=12V, VOUT=3.3V, IOUT=0A)

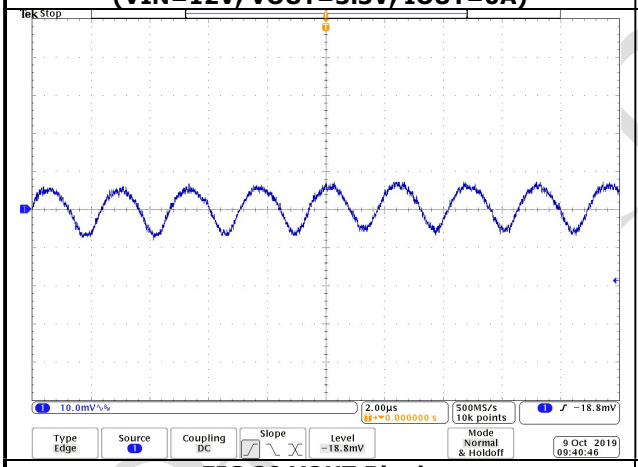


FIG.29 VOUT Ripple
(VIN=12V, VOUT=3.3V, IOUT=2A)

APPLICATIONS INFORMATION:

Reference Circuit for General Application:

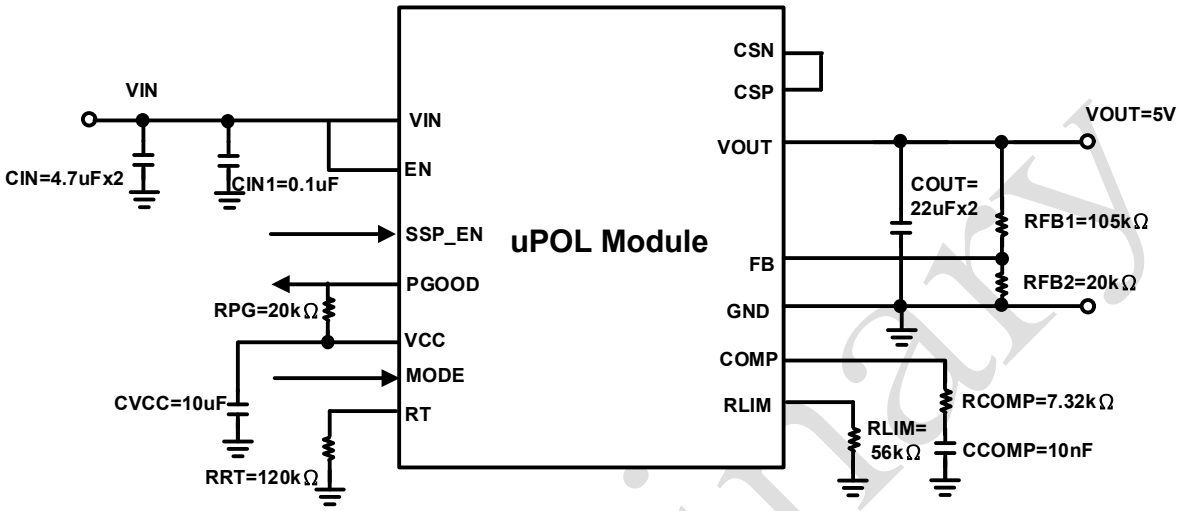


FIG.30 VOUT=5V

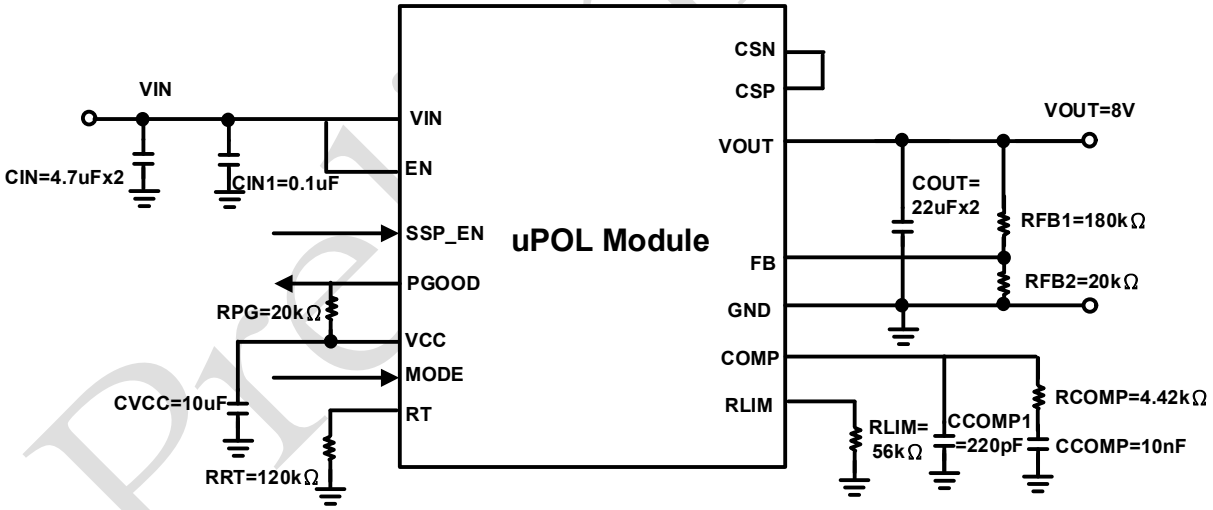


FIG.31 VOUT=8V

Output Voltage Setting:

The output voltage can be set by a resistive divider from the output to ground. The resistive divider allows the FB pin to sense a fraction of the output voltage as following figure. The output voltage is set according to the following equation where the reference voltage VFB is typical 0.8V.

$$V_{OUT} = \left(1 + \frac{RFB1}{RFB2} \right) \times V_{FB}$$

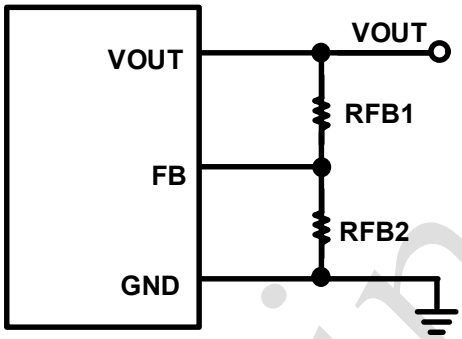


FIG.32 Output Voltage Setting

Minimum Duty Cycle:

The module has the limitation for the minimum duty cycle (Duty_min) 4%, For example, when VOUT is set to 1V, the maximum VIN is 25V.

$$\text{VIN maximum} = \frac{VOUT}{Duty\_min}$$

Inductor Peak Current Limit Setting

The current limit of high-side MOSFET switch is adjustable by an external resistor connected to the RLIM pin. The recommended resistor value is ranging from 42.2kΩ (for typ.4.4A) to 56kΩ (for typ. 3.4A). When the inductor current reaches the current limit threshold, the COMP voltage will be clamped to limit the inductor current. Inductor current ripple also should be considered into current limit setting. The current limit value is set according to the following approximate equation:

$$R_{LIM}(k\Omega) = \frac{178.8}{I_{LIM} - 0.2531} - 1$$

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The external voltage source can be an external voltage supply below 5.5V, VCC or the output of the module if the output voltage is regulated under 5.5V. It is recommended to connect a 20kΩ between external voltage source to PGOOD pin.

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply VIN directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to VIN by adding a resistor REN and a capacitor CEN, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V). To prevent the device being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (REN1 and REN2) can be used to externally set the input under-voltage lockout threshold, as following figure.

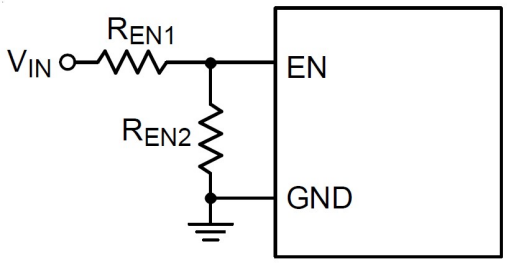


FIG.33 Resistive Divider for Under-Voltage Lockout Threshold Setting

Soft-Start

There is a 10nF capacitor inside the module for soft-start. In normal condition, just keep SS pin floating. The external capacitor CSS between SS pin and GND can increase the soft-start time. An internal current source Iss (6uA) charges an SS pin capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft start interval. The typical soft start time which is VOUT rise from zero to 90% of setting value is calculated as following equation :

$$Tss\ (s) = \frac{0.8}{Iss} \times (\ C_{ss\_external} + 10n\ )$$

Output Under-Voltage Protection

The module includes output under-voltage protection against over-load or short-circuited condition by constantly monitoring the feedback voltage VFB. If VFB drops below the under-voltage protection threshold (typically 50% of the internal reference voltage), the module will turn off the switches then the inductor current drop to zero and enter the hiccup mode to discharge the CSS. During hiccup mode, the device remains shut down. After the SS pin voltage discharges to less than 150mV (typically), the module attempts to re-start up again.

Compensation Network

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. For Vout=0.9V~6V application, follow the Fig.25 compensation network. For VOUT=6V~8V application, follow Fig.26 compensation network.

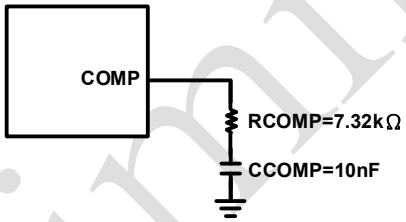


FIG.34 VOUT=0.9V~6V Compensation Network

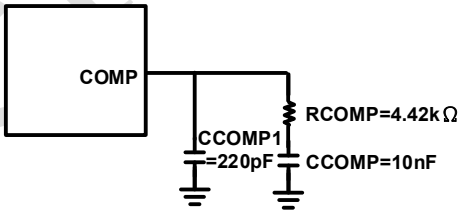


FIG.35 VOUT=6V~8V Compensation Network

APPLICATIONS INFORMATION:

Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as following figure. Then Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The module is designed for using when the case temperature is below 140°C regardless the change of output current, input/output voltage or ambient temperature.

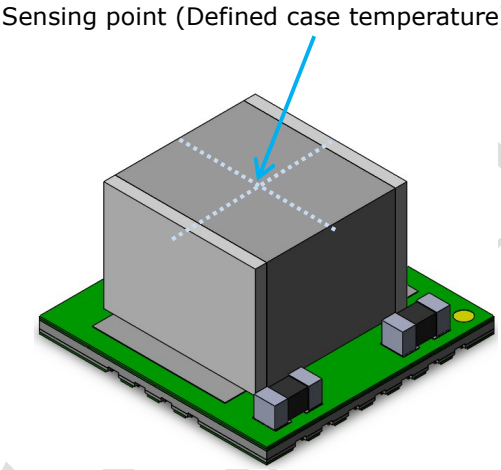


FIG 36. Case Temperature Sensing Point

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Following figure shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

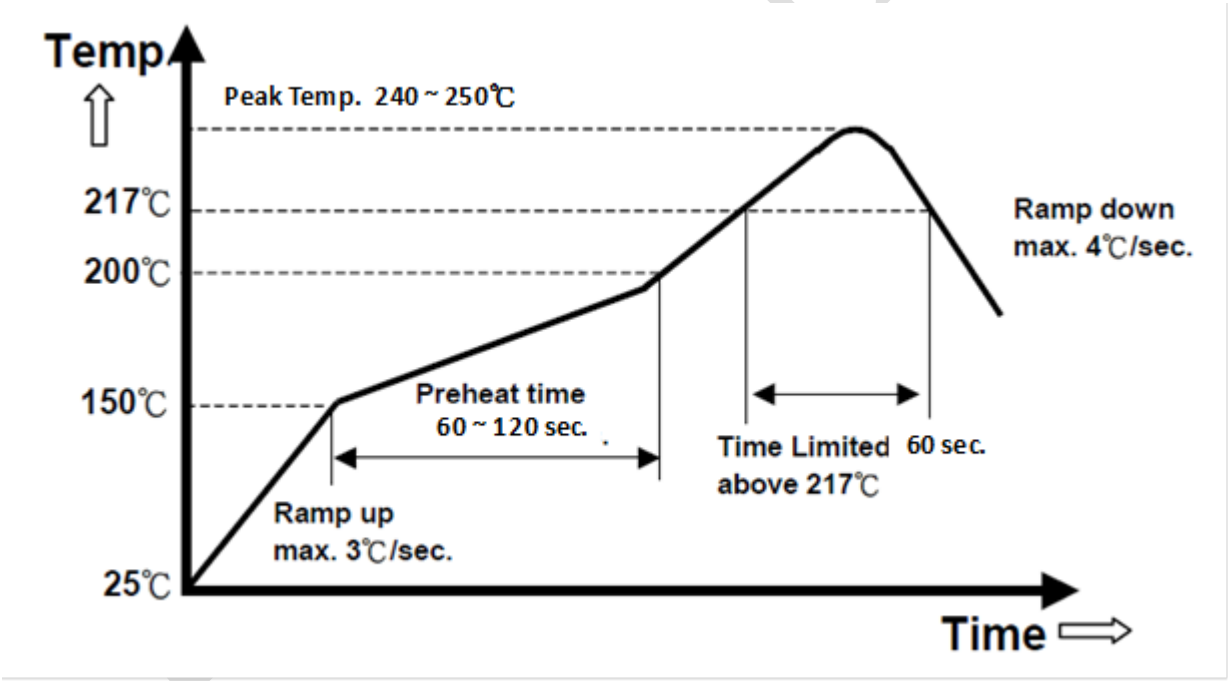
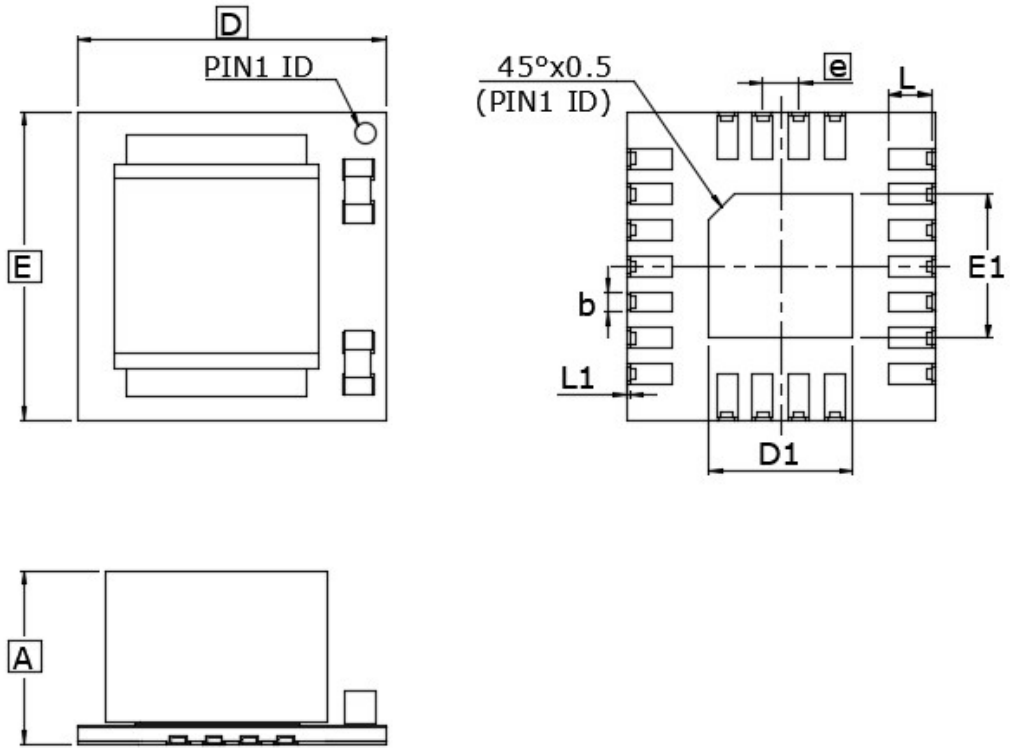


FIG.37 Recommendation Reflow Profile

PACKAGE OUTLINE DRAW:

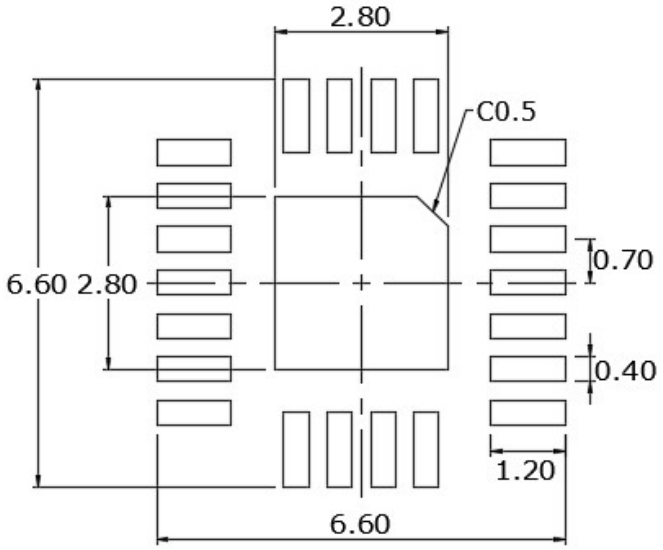
Unit:mm



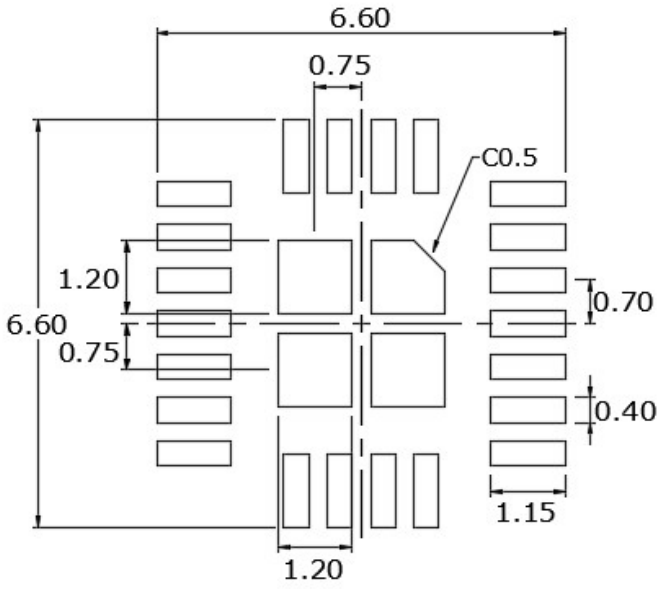
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	3.30	3.50
D	5.90	6.00	6.10
D1	2.70	2.80	2.90
E	5.90	6.00	6.10
E1	2.70	2.80	2.90
e	0.60	0.70	0.80
b	0.30	0.40	0.50
L	0.70	0.80	0.90
L1	0.00	0.10	0.20

LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN

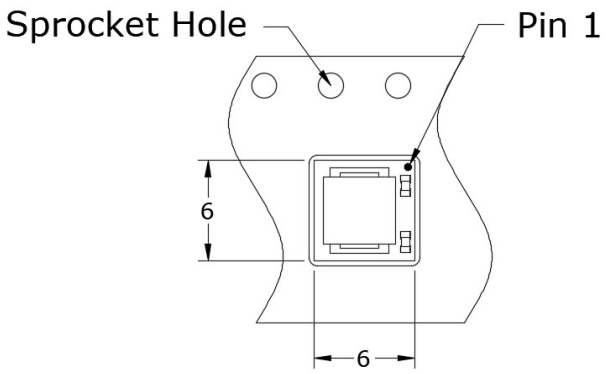


RECOMMENDED STENCIL PATTERN
BASED ON 0.1mm THICKNESS STENCIL(Reference only)
(Recommended solder paste coverage 55~100%)

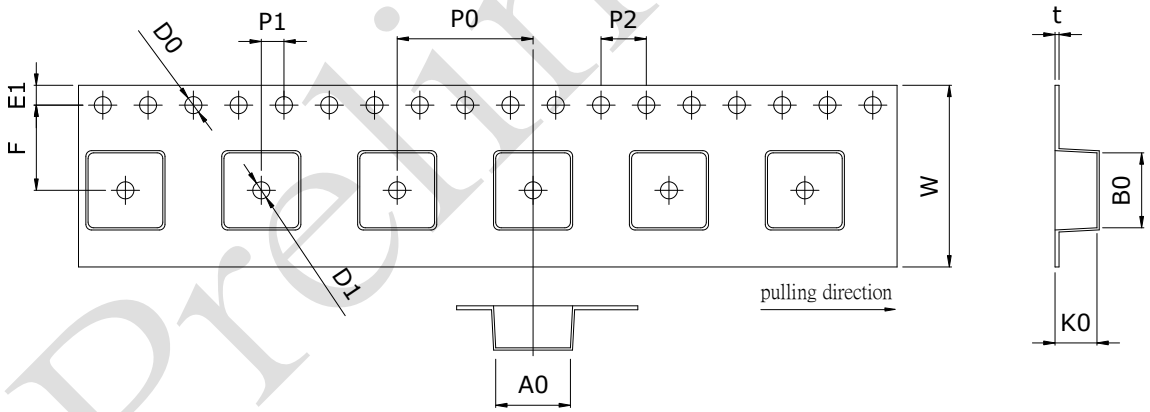
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

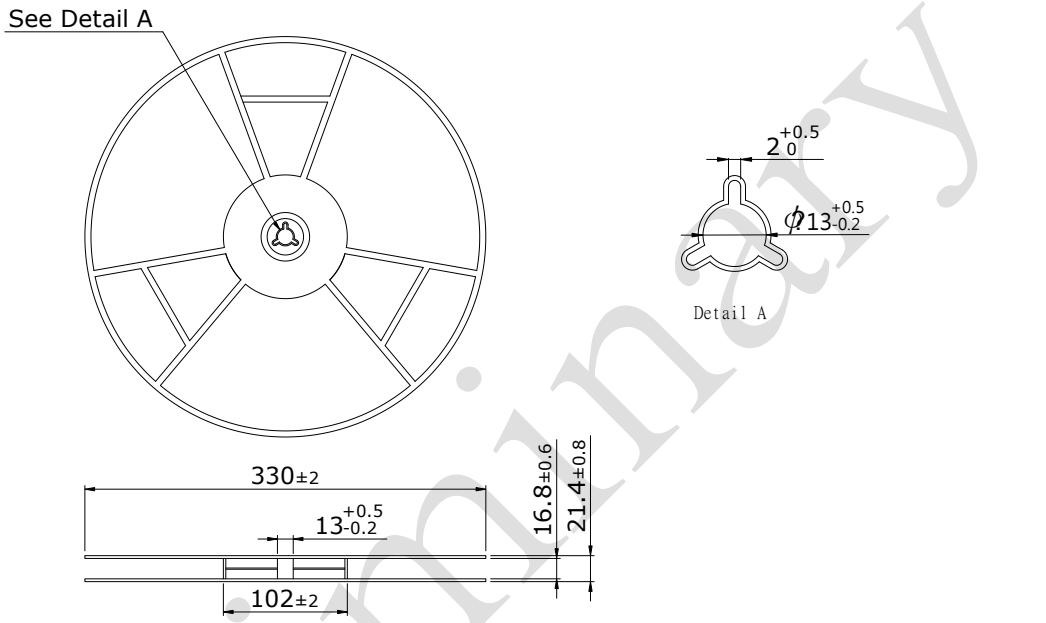


A0	6.60 ± 0.10	E1	1.75 ± 0.10
B0	6.60 ± 0.10	K0	3.70 ± 0.10
F	7.50 ± 0.10	P0	12.00 ± 0.10
W	16.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.5 +0.1/-0.0	P2	4.00 ± 0.10
D1	φ1.5 Min.	t	0.35 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

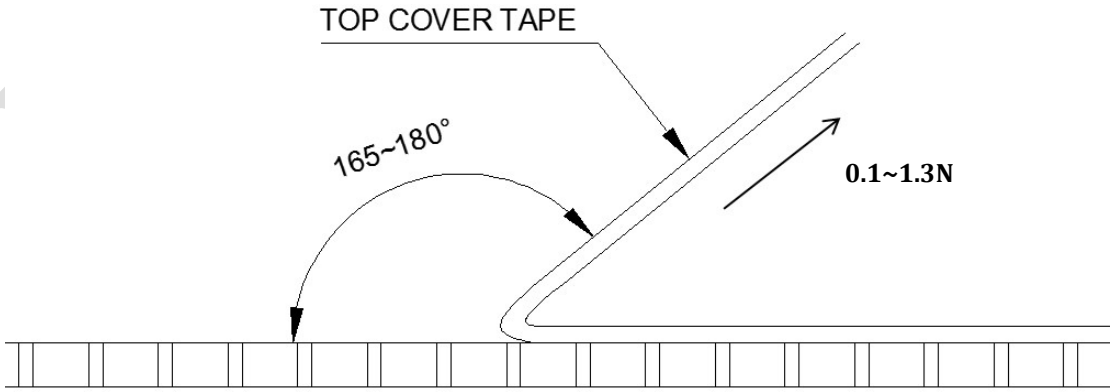
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



REVISION HISTORY

Date	Revision	Changes
2019.09.03	P00	Release the preliminary spec
2019.10.25	P01	Modify preliminary spec and add the application information
2019.11.04	P02	Modify preliminary spec and application information