3-A DUAL NON-SYNCHRONOUS CONVERTER WITH INTEGRATED HIGH-SIDE MOSFET AND EXTERNAL COMPENSATION

FEATURES

- **4.5-V to 28-V Input Range**
- **Output Voltage 0.8 V to 90% of Input Voltage**
- **Output Current Up to 3 A**
- **Two Fixed Switching Frequency Versions:**
  - **TPS55383: 300 kHz**
  - **TPS55386: 600 kHz**
- **Three Selectable Levels of Overcurrent Protection (Output 2)**
- **0.8-V 1.75% Voltage Reference**
- **2.1-ms Internal Soft Start**
- **Dual PWM Outputs 180° Out-of-Phase**
- **Ratiometric or Sequential Startup Modes**
- **Configurable as Dual Output or Two-Channel Single Output Multiphase for 6 amp Capability**
- **85-mΩ Internal High-Side MOSFETs**
- **Current Mode Control with External Compensation**
- **Pulse-by-Pulse Overcurrent Protection**
- **Thermal Shutdown Protection at +148°C**
- **16-Pin PowerPAD™ HTSSOP package**

APPLICATIONS

- **Set Top Box**
- **Digital TV**
- **Power for DSP**
- **Consumer Electronics**

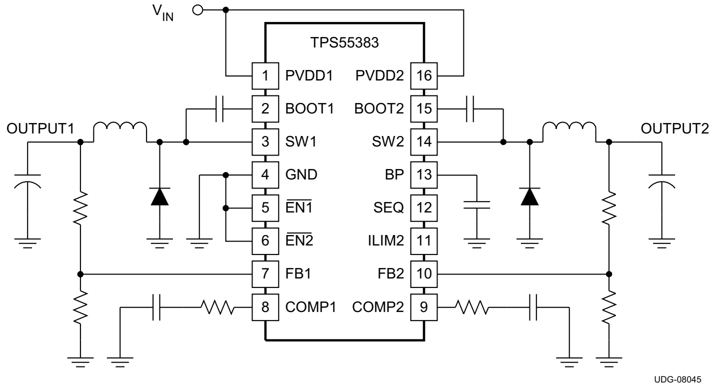
CONTENTS

DESCRIPTION

The TPS55383 and TPS55386 are dual output, non-synchronous buck converters capable of supporting 3-A output applications that operate from a 4.5-V to 28-V input supply voltage, and require output voltages between 0.8 V and 90% of the input voltage.

With an internally-determined operating frequency and soft start time, these converters provide many features with a minimum of external components. The outputs of the two error amplifiers are accessible allowing user optimization of the feedback loop under a wide range of output filter characteristics. Channel 1 overcurrent protection is set at 4.5 A, while Channel 2 overcurrent protection level is selected by connecting a pin to ground, to BP, or left floating. The setting levels are used to allow for scaling of external components for applications that do not need the full load capability of both outputs.

The outputs may be enabled independently, or configured to allow either ratiometric or sequential startup sequencing. Additionally, the two outputs may be powered from different sources.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

DEVICE NUMBER	OPERATING FREQUENCY (kHz)	PACKAGE	MEDIA	UNITS (Pieces)
TPS55383PWP	300	Plastic 16-Pin HTSSOP	Tube	90
TPS55383PWPR			Tape and Reel	2000
TPS55386PWP	600		Tube	90
TPS55386PWPR			Tape and Reel	2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Input voltage range	PVDD1, PVDD2, $\overline{EN1}$, $\overline{EN2}$	30	V
	BOOT1, BOOT2	V_{SW}+ 7	
	SW1, SW2	–2 to 30	
	SW1, SW2 transient (< 50ns)	–3 to 31	
	BP	6.5	
	SEQ, ILIM2	–0.3 to 6.5	
	COMP1, COMP2	–0.3 to 3.5	
	FB1, FB2	–0.3 to 3	
	SW1, SW2 output current	7	A
	BP load current	35	mA
T_{stg}	Storage temperature	–55 to +165	°C
T_J	Operating temperature	–40 to +150	
	Soldering temperature	+260	

(1) Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{PVDD2}	Input voltage		4.5	28	V
T_J	Operating junction temperature		–40	+125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	UNIT
Human body model	2k	V
CDM	1.5k	
Machine Model	250	

PACKAGE DISSIPATION RATINGS(1)(2)(3)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-THERMAL PAD (°C/W)	T_A = +25°C POWER RATING (W)	T_A = +85°C POWER RATING (W)
Plastic 16-Pin HTSSOP (PWP)	2.07(4)	1.6	1.0

(1) For more information on the PWP package, refer to TI Technical Brief (SLMA002A).
(2) TI device packages are modeled and tested for thermal performance using printed circuit board designs outlined in JEDEC standards JESD 51-3 and JESD 51-7.
(3) For application information, see the *Power Derating* section.
(4) $T_{J\text{-}A}$ = +40°C/W.

ELECTRICAL CHARACTERISTICS

$-40°C \leq T_J \leq +125°C$, $V_{PVDD1} = V_{PVDD2} = 12$ V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (PVDD)							
V_{PVDD1}	Input voltage range			4.5		28	V
V_{PVDD2}							
IDD_{SDN}	Shutdown		$V_{\overline{EN1}} = V_{\overline{EN2}} = V_{PVDD2}$		70	150	µA
IDD_Q	Quiescent, non-switching		V_{FB} = 0.9 V, Outputs OFF		1.8	3.0	mA
IDD_{SW}	Quiescent, while-switching		SW node unloaded; Measured as BP sink current		5		
V_{UVLO}	Minimum turn-on voltage		PVDD2 only	3.8	4.1	4.4	V
$V_{UVLO(hys)}$	Hysteresis				400	600	mV
t_{START}(1)(2)	Time from startup to softstart begin		C_{BP} = 10 µF, $\overline{EN1}$ and $\overline{EN2}$ go low simultaneously		2		ms
ENABLE ($\overline{EN}$)							
$V_{\overline{EN1}}$, $V_{\overline{EN2}}$	Enable threshold			0.9	1.2	1.5	V
	Enable threshold hysteresis(1)				50		mV
$I_{\overline{EN1}}$. $I_{\overline{EN2}}$	Enable pull-up current		$V_{\overline{EN1}} = V_{\overline{EN2}} = 0$ V		6	12	µA
$t_{\overline{EN}}$(1)	Time from enable to soft-start begin		Other EN pin = GND		10		µs
BP REGULATOR (BP)							
BP	Regulator voltage		8 V < P_{VDD2} < 28 V	5	5.25	5.6	V
BP_{LDO}	Dropout voltage		P_{VDD2} = 4.5 V; switching, no external load on BP		400	550	mV
I_{BP}(1)	Regulator external load					2	mA
I_{BPS}	Regulator short circuit		4.5 V < P_{VDD2} < 28 V	10	20	30	
OSCILLATOR							
f_{SW}	Switching frequency	TPS55383		255	310	375	kHz
		TPS55386		510	630	750	
t_{DEAD}(1)	Clock dead time				140		ns
ERROR AMPLIFIER (EA) and VOLTAGE REFERENCE (REF)							
$V_{FB1,}$ V_{FB2}	Feedback input voltage		0°C < T_J < +85°C	786	800	812	mV
			–40°C < T_J < +125°C	784		812	
$I_{FB1,}$ I_{FB2}	Feedback input bias current				3	50	nA
g_M1, g_M2(1)	Error Amplifier transconductance			220	315	420	µS
f_{p1}, f_{p2}(1)	Error Amplifier dominant pole frequency			5	6		kHz
$I_{SINK(COMP1)}$, $I_{SINK(COMP2)}$	Error Amplifier sink current capability		$V_{FB1} = V_{FB2}$ = 0.9V, V_{COMP} = 2 V	15	30	40	µA
$I_{SRC(COMP1)}$, $I_{SRC(COMP2)}$	Error Amplifier source current capability		$V_{FB1} = V_{FB2}$ = 0.7V, V_{COMP} = 0 V	15	30	40	µA
SOFT START (SS)							
T_{SS1}, T_{SS2}	Soft start time			1.5	2.1	2.7	ms

(1) Ensured by design. Not production tested.

(2) When both outputs are started simultaneously, a 20-mA current source charges the BP capacitor. Faster times are possible with a lower BP capacitor value. More information can be found in the *Input UVLO and Startup* section.

ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ T_J ≤ +125°C, V_{PVDD1} = V_{PVDD2} = 12 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION							
I_{CL1}	Current limit Channel 1			3.6	4.5	5.6	A
I_{CL2}	Current limit Channel 2		V_{ILIM2} = V_{BP}	3.6	4.5	5.6	
			V_{ILIM2} = (floating)	2.4	3.0	3.6	
			V_{ILIM2} = GND	1.15	1.50	1.75	
V_{UV1} V_{UV2}	Low-level output threshold to declare a fault		Measured at feedback pin.		670	730	mV
T_{HICCUP} (3)	Hiccup timeout				10		ms
$t_{ON1(oc)}$ (3) $t_{ON2(oc)}$ (3)	Minimum overcurrent pulse width				90	150	ns
BOOTSTRAP							
R_{BOOT1}, R_{BOOT2}	Bootstrap switch resistance		From BP to BOOT1 or BP to BOOT2, I_{EXT} = 50 mA		18		Ω
OUTPUT STAGE (Channel 1 and Channel 2)							
$R_{DS(on)}$ (3)	MOSFET on resistance plus bond wire resistance		T_J = +25°C, V_{PVDD2} = 8 V		85		mΩ
			–40°C < T_J < +125°C, V_{PVDD2} = 8 V		85	165	
$t_{ON(min)}$ (3)	Minimum controllable pulse width		I_{SWx} peak current > 1 A (4)		100	200	ns
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0.9 V			0	%
D_{MAX}	Maximum Duty Cycle	TPS55383	f_{SW} = 300 kHz	90	95		%
		TPS55386	f_{SW} = 600 kHz	85	90		%
I_{SW}	Switching node leakage current (sourcing)		Outputs OFF		2	12	µA
THERMAL SHUTDOWN							
T_{SD} (3)	Shutdown temperature				148		°C
$T_{SD(hys)}$ (3)	Hysteresis				20		

(3) Ensured by design. Not production tested.
(4) See Figure 14 for I_{SWx} peak current <1 A.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT (NON-SWITCHING)
vs
JUNCTION TEMPERATURE

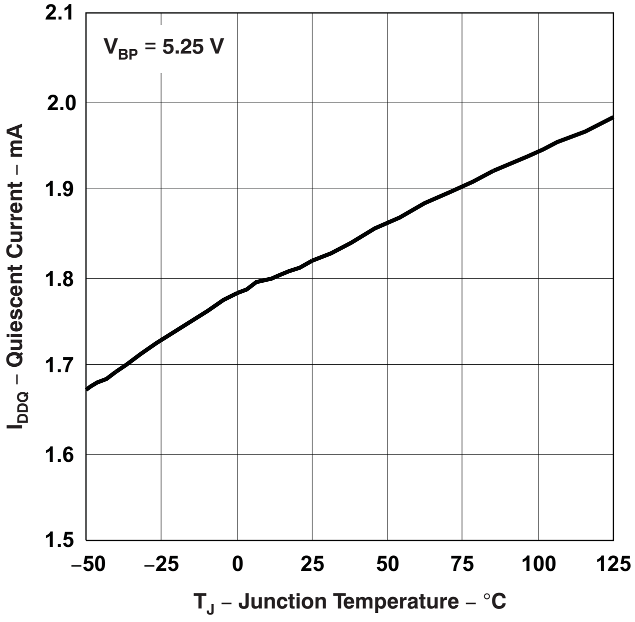


Figure 1.

SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

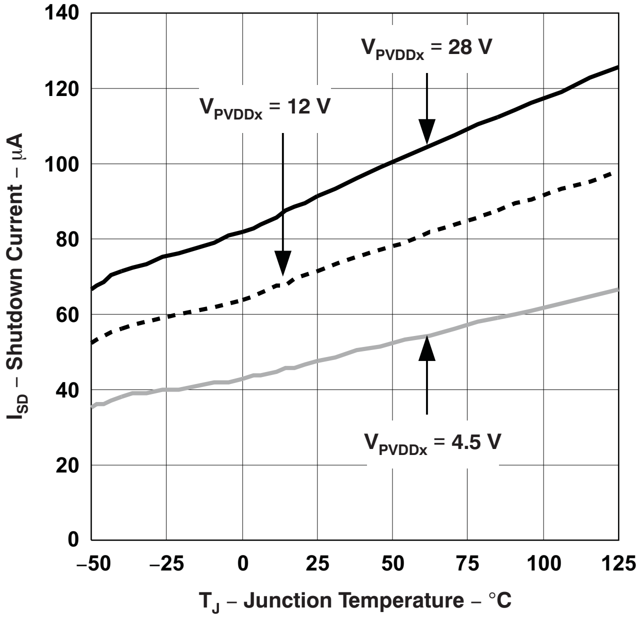


Figure 2.

UNDERVOLTAGE LOCKOUT THRESHOLD
vs
JUNCTION TEMPERATURE

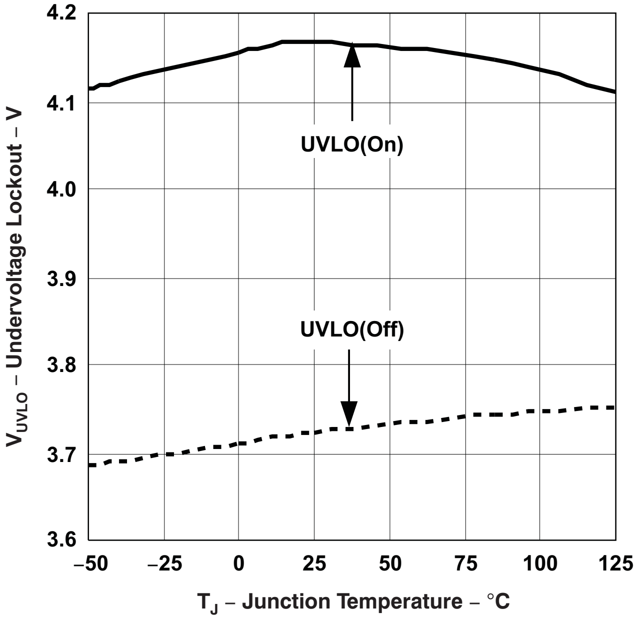


Figure 3.

ENABLE THRESHOLDS
vs
JUNCTION TEMPERATURE

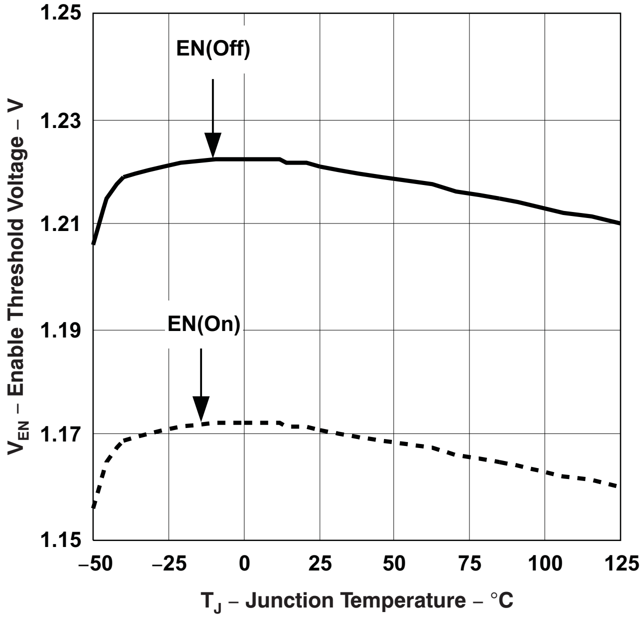


Figure 4.

TYPICAL CHARACTERISTICS (continued)

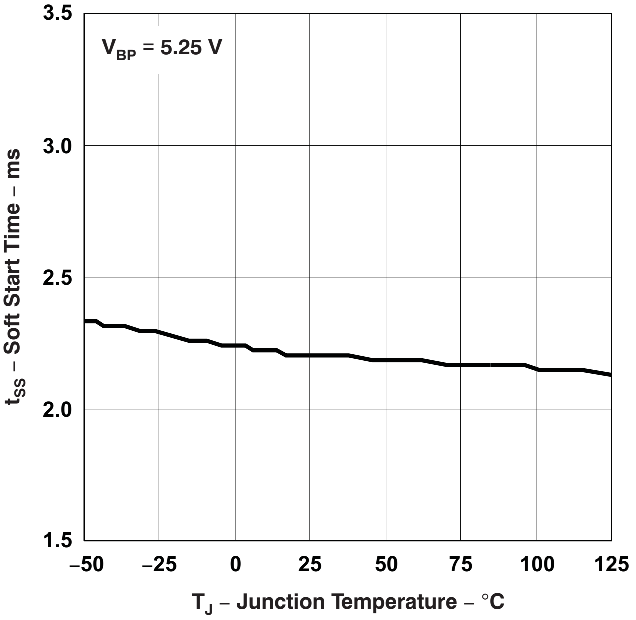

SOFT START TIME
vs
JUNCTION TEMPERATURE

Figure 5.

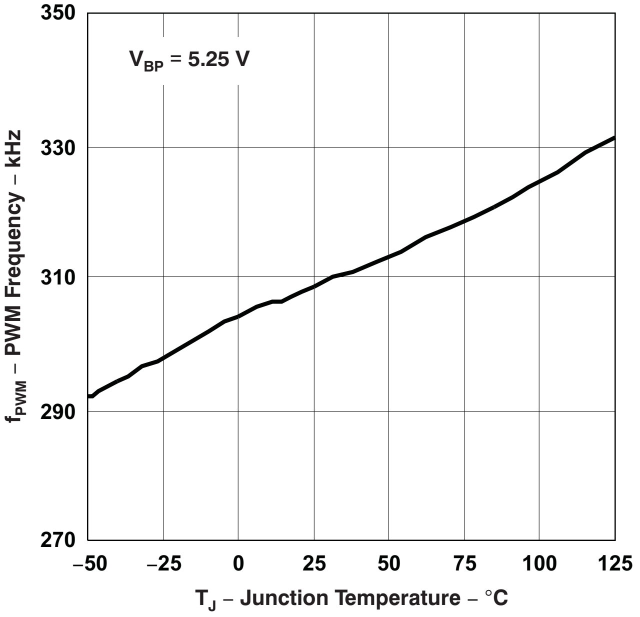

SWITCHING FREQUENCY (300 kHz)
vs
JUNCTION TEMPERATURE

Figure 6.

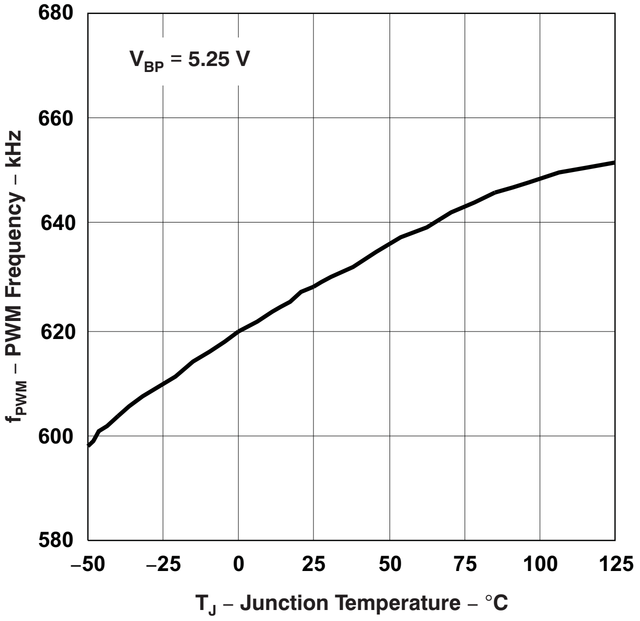

SWITCHING FREQUENCY (600 kHz)
vs
JUNCTION TEMPERATURE

Figure 7.

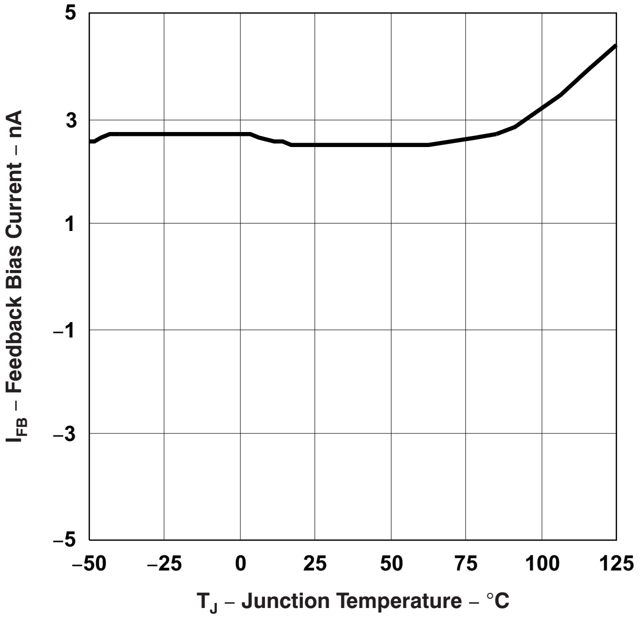

FEEDBACK BIAS CURRENT
vs
JUNCTION TEMPERATURE

Figure 8.

TYPICAL CHARACTERISTICS (continued)

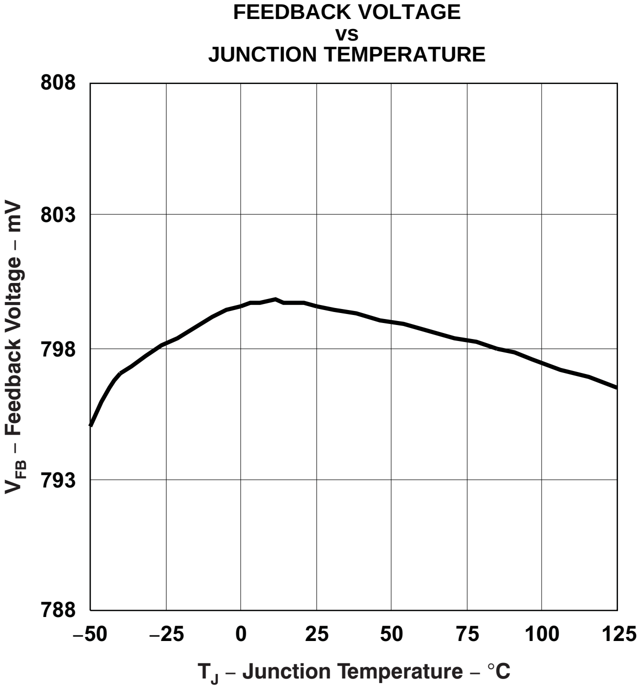


Figure 9.

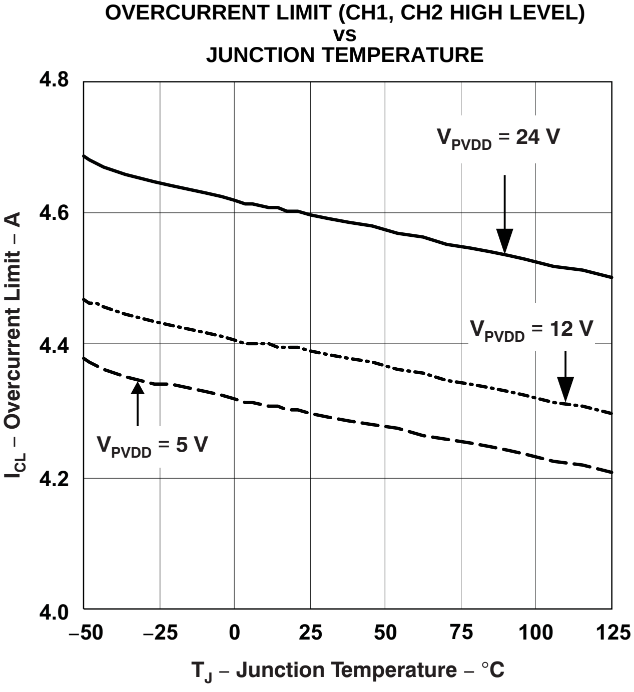


Figure 10.

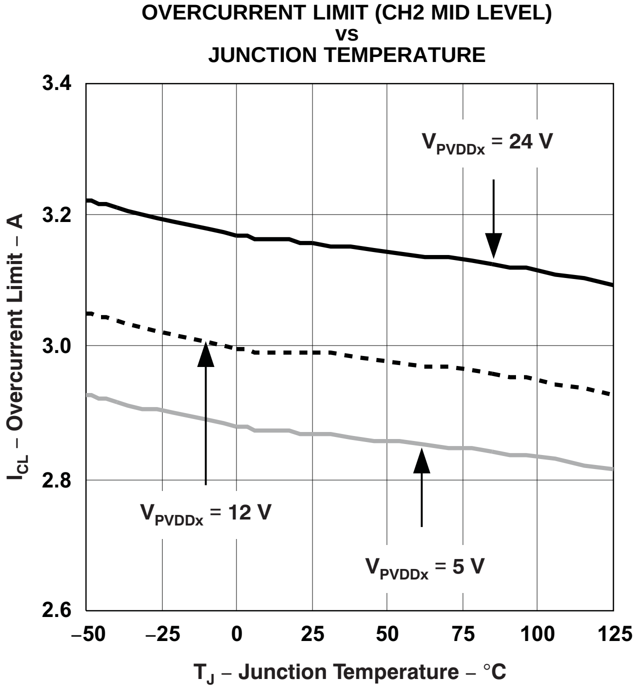


Figure 11.

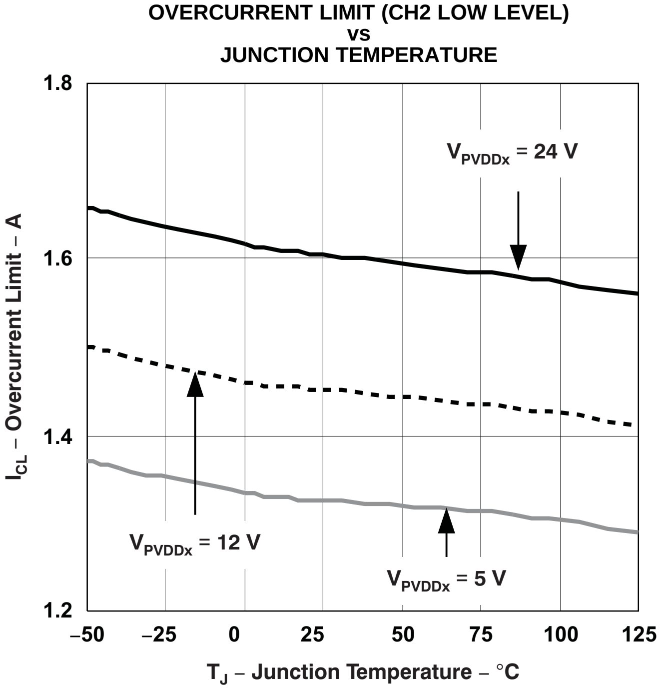


Figure 12.

TYPICAL CHARACTERISTICS (continued)

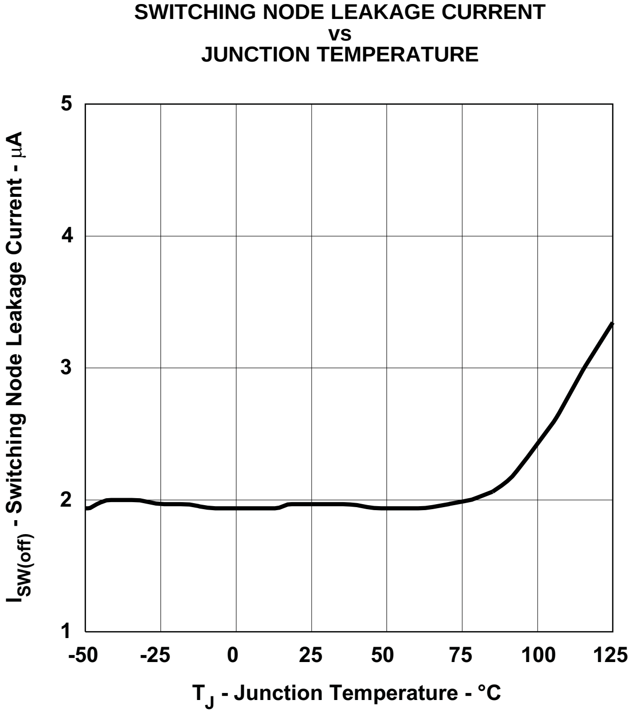


Figure 13.

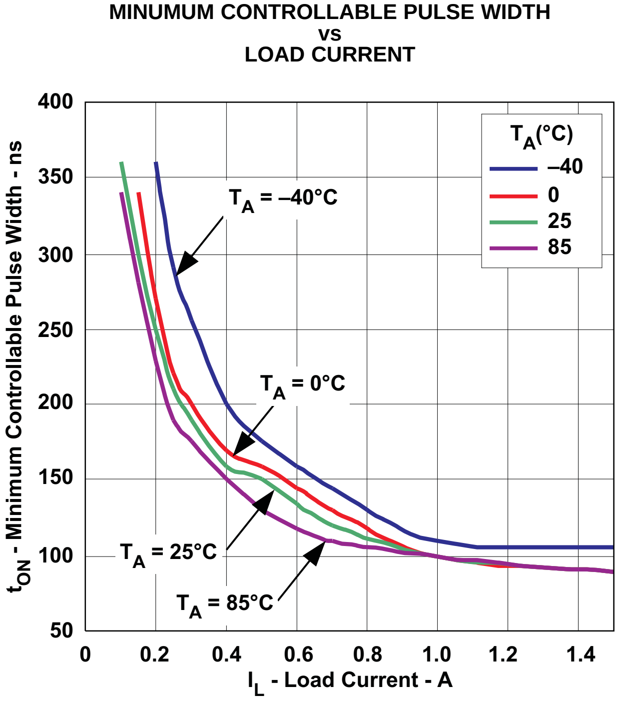


Figure 14.

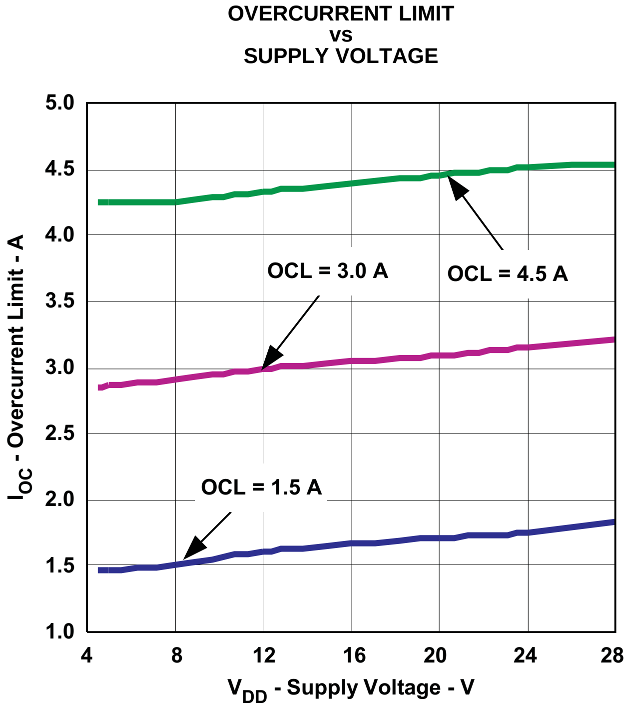
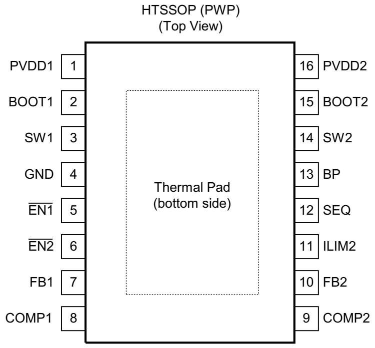


Figure 15.

DEVICE INFORMATION

PIN CONNECTIONS



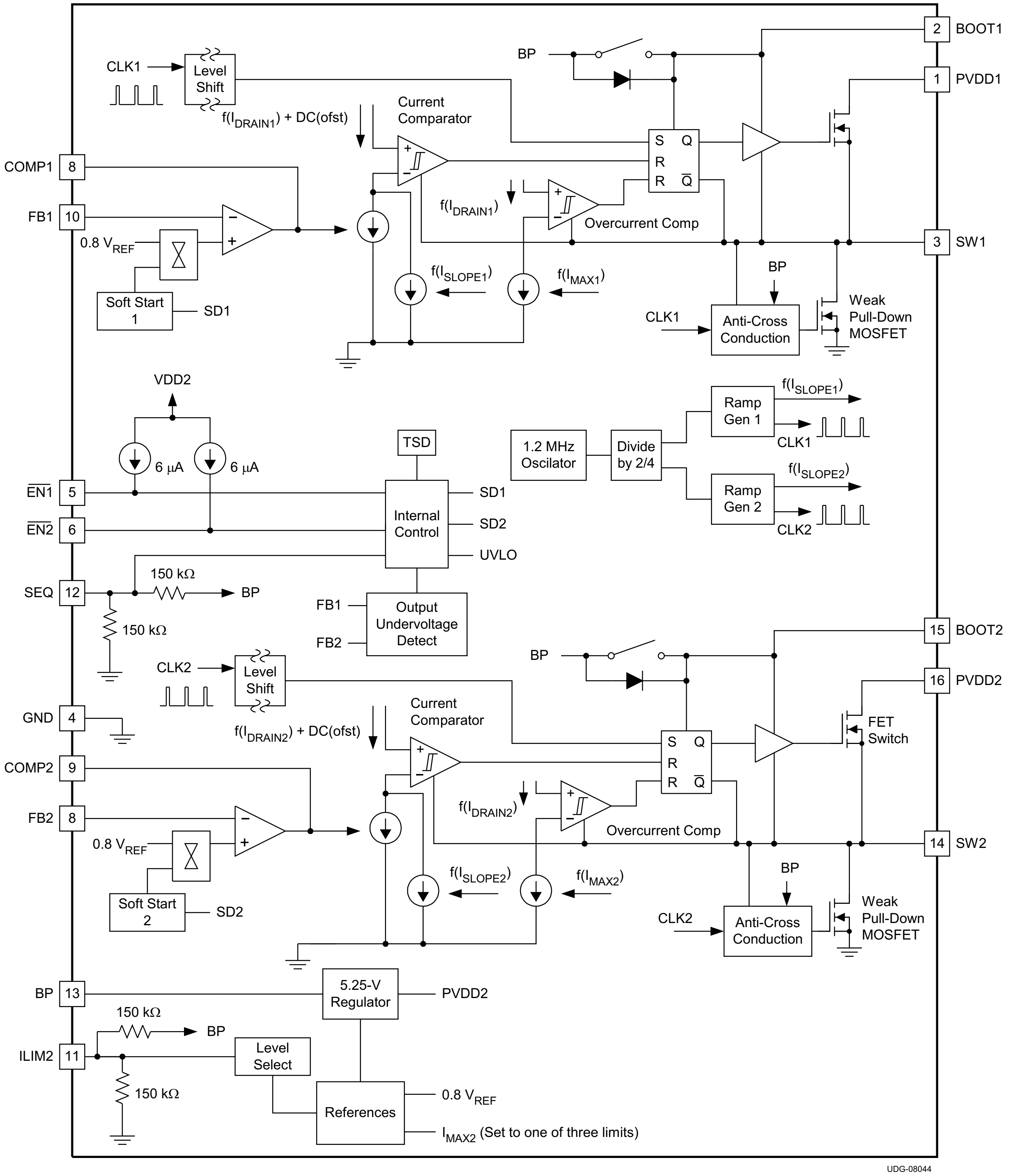
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT1	2	I	Input supply to the high side gate driver for Output 1. Connect a 22-nF to 82-nF capacitor from this pin to SW1. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor.
BOOT2	15	I	Input supply to the high side gate driver for Output 2. Connect a 22-nF to 82-nF capacitor from this pin to SW2. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor.
BP	13	-	Regulated voltage to charge the bootstrap capacitors. Bypass this pin to GND with a low ESR (4.7-µF to 10-µF X7R or X5R) ceramic capacitor.
COMP1	8	O	Output of Error Amplifier for Output 1. A series connected R-C network from this pin to GND serves to compensate the feedback loop. See Feedback Loop Compensation Component Selection for further information.
COMP2	9	O	Output of Error Amplifier for Output 2. A series connected R-C network from this pin to GND serves to compensate the feedback loop. See Feedback Loop Compensation Component Selection for further information.
$\overline{\text{EN1}}$	5	I	Active low enable input for Output 1. If the voltage on this pin is greater than 1.55 V, Output 1 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output 1 and allows soft start of Output 1 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for "always ON" operation.
$\overline{\text{EN2}}$	6	I	Active low enable input for Output 2. If the voltage on this pin is greater than 1.55 V, Output 2 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output 2 and allows soft start of Output 2 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for "always ON" operation.
FB1	7	I	Voltage feedback pin for Output 1. The internal transconductance error amplifier adjusts the PWM for Output 1 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from Output 1 to ground, with the center connection tied to this pin, determines the value of the regulated output voltage. Compensation for the feedback loop is provided externally to the device. See Feedback Loop Compensation Component Selection section for further information.
FB2	10	I	Voltage feedback pin for Output 2. The internal transconductance error amplifier adjusts the PWM for Output 2 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from Output 2 to ground, with the center connection tied to this pin, determines the value of the regulated Output voltage. Compensation for the feedback loop is provided externally to the device. See Feedback Loop Compensation Component Selection section for further information.
GND	4	-	Ground pin for the device. Connect directly to Thermal Pad.
ILIM2	11	I	Current limit adjust pin for Output 2 only. This function is intended to allow a user with asymmetrical load currents (Output 1 load current much greater than Output 2 load current) to optimize component scaling of the lower current output while maintaining proper component derating in a overcurrent fault condition. The discrete levels are available as shown in Table 2, *Current Limit Threshold Adjustment for Output 2*. Note: An internal 2-resistor divider (150-kΩ each) connects BP to ILIM2 and to GND.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
PVDD1	1	I	Power input to the Output 1 high side MOSFET only. This pin should be locally bypassed to GND with a low ESR ceramic capacitor of 10-µF or greater.
PVDD2	16	I	The PVDD2 pin provides power to the device control circuitry, provides the pull-up for the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins and provides power to the Output 2 high-side MOSFET. This pin should be locally bypassed to GND with a low ESR ceramic capacitor of 10-µF or greater. The UVLO function monitors PVDD2 and enables the device when PVDD2 is greater than 4.1 V.
SEQ	12	I	This pin configures the output startup mode. If the SEQ pin is connected to BP, then when Output 2 is enabled, Output 1 is allowed to start after Output 2 has reached regulation; that is, sequential startup where Output 1 is slave to Output 2. If $\overline{\text{EN2}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie $\overline{\text{EN1}}$ to ground. If the SEQ pin is connected to GND, then when Output 1 is enabled, Output 2 is allowed to start after Output 1 has reached regulation; that is, sequential startup where Output 2 is slave to Output 1. If $\overline{\text{EN1}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie $\overline{\text{EN2}}$ to ground. If left floating, Output 1 and Output 2 start ratio-metrically when both outputs are enabled at the same time. They will soft start at a rate determined by their final output voltage and enter regulation at the same time. If the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins are allowed to operate independently, then the two outputs also operate independently NOTE: An internal two resistor (150-kΩ each) divider connects BP to SEQ and to GND. See the Sequence States table.
SW1	3	O	Source (switching) output for Output 1 PWM. A snubber is recommended to reduce ringing on this node. See SW Node Ringing for further information.
SW2	14	O	Source (switching) output for Output 2 PWM. A snubber is recommended to reduce ringing on this node. See SW Node Ringing for further information.
Thermal Pad	-	-	This pad must be tied externally to a ground plane and the GND pin.

BLOCK DIAGRAM



APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The TPS55383 and TPS55386 are dual output, non-synchronous converters. Each PWM channel contains an externally-compensated error amplifier, current mode pulse width modulator (PWM), switch MOSFET, enable, and fault protection circuitry. Common to the two channels are the internal voltage regulator, voltage reference, clock oscillator, and output voltage sequencing functions.

NOTE:

> Unless otherwise noted, the term *TPS5538x* applies to both the TPS55383 and TPS55386. Also, unless otherwise noted, a label with a lowercase *x* appended implies the term applies to both outputs of the two modulator channels. For example, the term $\overline{ENx}$ implies both $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$. Unless otherwise noted, all parametric values given are typical. Refer to the *Electrical Characteristics* for minimum and maximum values. Calculations should be performed with tolerance values taken into consideration.

Voltage Reference

The bandgap cell common to both outputs is trimmed to 800 mV.

Oscillator

The oscillator frequency is internally fixed at two times the SWx node switching frequency. The two outputs are internally configured to operate on alternating switch cycles (that is, 180° out-of-phase).

Input Undervoltage Lockout (UVLO) and Startup

When the voltage at the PVDD2 pin is less than 4.1 V, a portion of the internal bias circuitry is operational, and all other functions are held OFF. All of the internal MOSFETs are also held OFF. When the PVDD2 voltage rises above the UVLO turn-on threshold, the state of the enable pins determines the remainder of the internal startup sequence. If either output is enabled ($\overline{\text{ENx}}$ pulled low), the BP regulator turns on, charging the BP capacitor with a 20-mA current. When the BP pin is greater than 4 V, PWM is enabled and soft start begins, depending on the SEQ mode of operation and the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ settings.

Note that the internal regulator and control circuitry are powered from PVDD2. The voltage on PVDD1 may be higher or lower than PVDD2. (See the *Dual Supply Operation* section.)

Enable and Timed Turn On of the Outputs

Each output has a dedicated (active low) enable pin. If left floating, an internal current source pulls the pin to PVDD2. By grounding, or by pulling the $\overline{\text{ENx}}$ pin to below approximately 1.2 V with an external circuit, the associated output is enabled and soft start is initiated.

If both enable pins are left in the *high* state, the device operates in a shutdown mode, where the BP regulator is shut down and minimal functions are active. The total standby current from both PVDD pins is approximately 70 µA at 12-V input supply.

An R-C connected to an $\overline{\text{ENx}}$ pin may be used to delay the turn-on of the associated output after power is applied to PVDDx (see Figure 16). After power is applied to PVDD2, the voltage on the $\overline{\text{ENx}}$ pin slowly decays towards ground. Once the voltage decays to approximately 1.2 V, then the output is enabled and the startup sequence begins. If it is desired to enable the outputs of the device immediately upon the application of power to PVDD2, then omit these two components and tie the $\overline{\text{ENx}}$ pin to GND directly.

If an R-C circuit is used to delay the turn-on of the output, the resistor value must be much less than 1.2 V / 6 µA or 200 kΩ. A suggested value is 51 kΩ. This resistor value allows the $\overline{\text{ENx}}$ voltage to decay below the 1.2-V threshold while the 6-µA bias current flows.

The capacitor value required to delay the startup time (after the application of PVDD2) is shown in Equation 1.

$$C = \frac{t_{DELAY}}{R \times \ell n\left(\frac{V_{IN} - 2 \times I_{\overline{ENx}} \times R}{V_{TH} - I_{\overline{ENx}} \times R}\right)} \text{farads} \quad (1)$$

where:

- R and C are the timing components
- V_{TH} is the 1.2-V enable threshold voltage
- $I_{\overline{ENx}}$ is the 6 µA enable pin biasing current

Additional enable pin functionality is dictated by the state of the SEQ pin. (See the *Output Voltage Sequencing* section.)

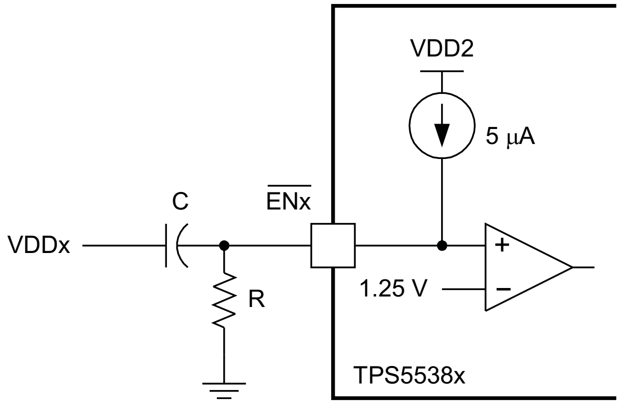


Figure 16. Startup Delay Schematic

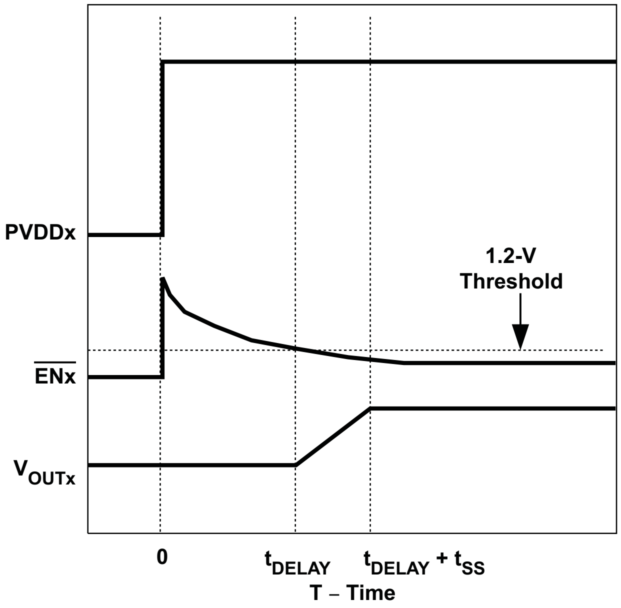


Figure 17. Startup Delay with R-C on Enable

DESIGN HINT

If delayed output voltage startup is not necessary, simply connect $\overline{EN1}$ and $\overline{EN2}$ to GND. This configuration allows the outputs to start immediately on valid application of PVDD2.

If $\overline{ENx}$ is allowed to go *high* after the Outputx has been in regulation, the upper MOSFET shuts off, and the output decays at a rate determined by the output capacitor and the load. The internal pulldown MOSFET remains in the OFF state. (See the *Bootstrap for N-Channel MOSFET* section.)

Output Voltage Sequencing

The TPS5538x allows single-pin programming of output voltage startup sequencing. During power-on, the state of the SEQ pin is detected. Based on whether the pin is tied to BP, to GND, or left floating, the outputs function as described in Table 1.

Table 1. Sequence States

SEQ PIN STATE	MODE	$\overline{\text{EN1}}$	$\overline{\text{EN2}}$
BP	Sequential, Output 2 then Output 1	Ignored by the device.when $V_{\overline{EN2}}$ < enable threshold voltage	Active
		Tie $\overline{\text{EN1}}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN2}}$ > enable threshold voltage	
		Tie $\overline{\text{EN1}}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN2}}$ > enable threshold voltage	
GND	Sequential, Output 1 then Output 2	Active	Ignored by the device.when $V_{\overline{EN1}}$ < enable threshold voltage
			Tie $\overline{\text{EN2}}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN1}}$ > enable threshold voltage
			Tie $\overline{\text{EN2}}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN1}}$ > enable threshold voltage
(floating)	Independent or Ratiometric, Output 1 and Output 2	Active. $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ must be tied together for Ratio-metric startup.	Active. $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ must be tied together for Ratio-metric startup.

If the SEQ pin is connected to BP, then when Output 2 is enabled, Output 1 is allowed to start approximately 400 µs after Output 2 has reached regulation; that is, sequential startup where Output 1 is slave to Output 2. If $\overline{\text{EN2}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

If the SEQ pin is connected to GND, then when Output 1 is enabled, Output 2 is allowed to start approximately 400 µs after Output 1 has reached regulation; that is, sequential startup where Output 2 is slave to Output 1. If $\overline{\text{EN1}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

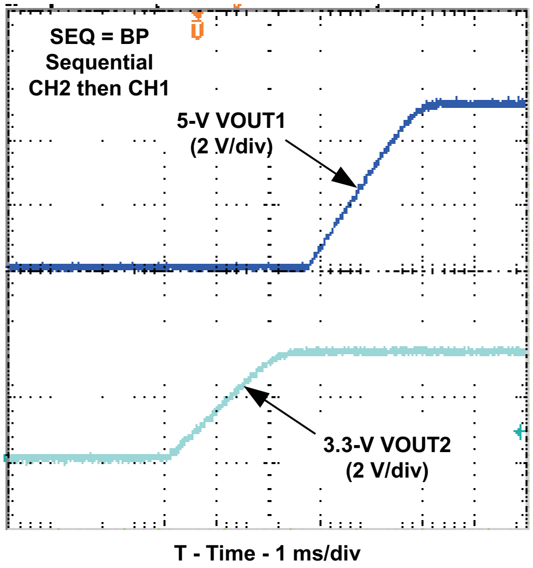


Figure 18. SEQ Pin TIed to BP

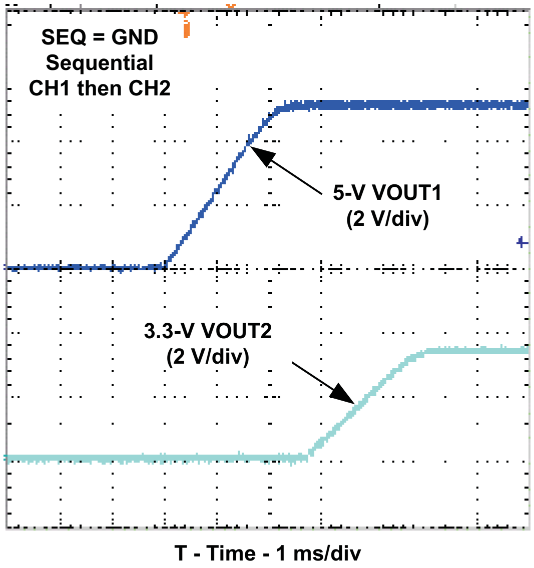


Figure 19. SEQ Pin Tied to GND

NOTE:

An R-C network connected to the $\overline{\text{ENx}}$ pin may be used in addition to the SEQ pin in sequential mode to delay the startup of the first output voltage. This approach may be necessary in systems with a large number of output voltages and elaborate voltage sequencing requirements. See *Enable and Timed Turn On of the Outputs.*

If the SEQ pin is left floating, Output 1 and Output 2 each start ratiometrically when both outputs are enabled at the same time. Output 1 and Output 2 soft start at a rate that is determined by the respective final output voltages and enter regulation at the same time. If the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins are allowed to operate independently, then the two outputs also operate independently.

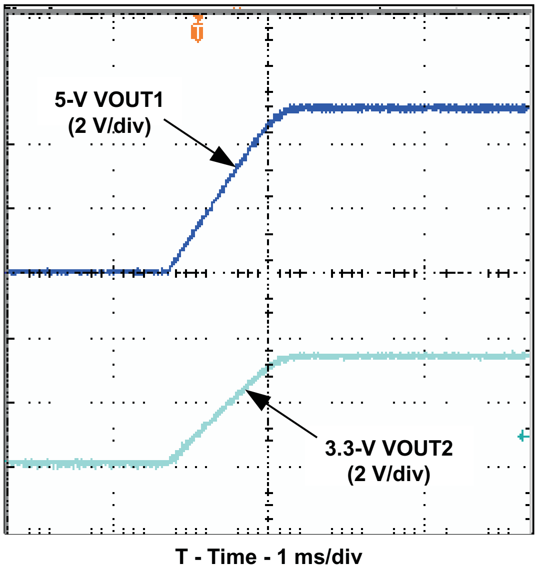


Figure 20. SEQ Pin Floating

Soft Start

Each output has a dedicated soft-start circuit. The soft-start voltage is an internal digital reference ramp to one of two noninverting inputs of the error amplifier. The other input is the (internal) precision 0.8-V reference. The total ramp time for the FB voltage to charge from 0 V to 0.8 V is about 2.1 ms. During a soft-start interval, the TPS5538x output slowly increases the voltage to the noninverting input of the error amplifier. In this way, the output voltage ramps up slowly until the voltage on the noninverting input to the error amplifier reaches the internal 0.8-V reference voltage. At that time, the voltage at the noninverting input to the error amplifier remains at the reference voltage.

During the soft-start interval, pulse-by-pulse current limiting is in effect. If an overcurrent pulse is detected, six PWM pulses are skipped to allow the inductor current to decay before another PWM pulse is applied. (See the *Output Overload Protection* section.) There is no pulse skipping if a current limit pulse is not detected.

DESIGN HINT

If the rate of rise of the input voltage (PVDDx) is such that the input voltage is too low to support the desired regulation voltage by the time soft-start has completed, then the output UV circuit may trip and cause a *hiccup* in the output voltage. In this case, use a timed delay startup from the $\overline{\text{ENx}}$ pin to delay the startup of the output until the PVDDx voltage has the capability of supporting the desired regulation voltage. See *Operating Near Maximum Duty Cycle* and *Maximum Output Capacitance* for related information.

Output Voltage Regulation

Each output has a dedicated feedback loop comprised of a voltage setting divider, an error amplifier, a pulse width modulator, and a switching MOSFET. The regulation output voltage is determined by a resistor divider connecting the output node, the FBx pin, and GND (see Figure 21). Assuming the value of the upper voltage setting divider is known, the value of the lower divider resistor for a desired output voltage is calculated by Equation 2.

$$R2 = R1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \tag{2}$$

where

- V_{REF} is the internal 0.8-V reference voltage

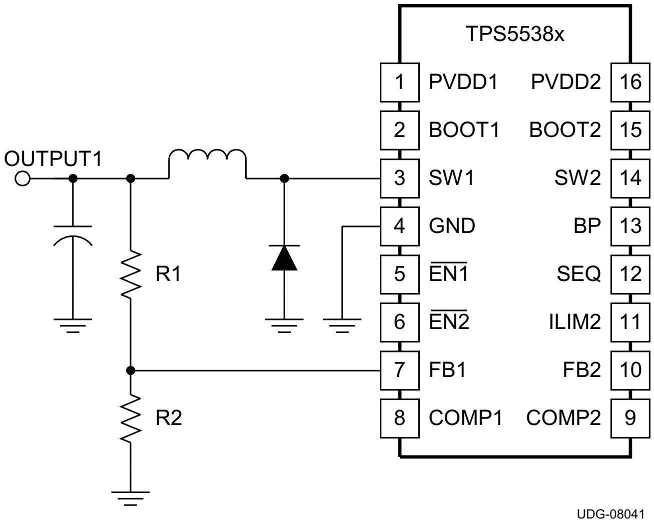


Figure 21. Voltage Setting Divider Network for Channel 1

DESIGN HINT

There is a leakage current of up to 12 µA out of the SW pin when a single output of the TPS5538x is disabled. Keeping the series impedance of R1 + R2 less than 50 kΩ prevents the output from floating above the referece voltage while the controller output is in the OFF state.

Feedback Loop Compensation Component Selection

In the feedback signal path, the output voltage setting divider is followed by an internal g_M-type error amplifier with a typical transconductance of 315 µS. An external series connected R-C circuit from the g_M amplifier output (COMPx pin) to ground serves as the compensation network for the converter. The signal from the error amplifier output is then buffered and combined with a slope compensation signal before it is mirrored to be referenced to the SW node. Here, it is compared with the current feedback signal to create a pulse-width-modulated (PWM) signal-fed to drive the upper MOSFET switch. A simplified equivalent circuit of the signal control path is depicted in Figure 22.

NOTE:

Noise coupling from the SWx node to internal circuitry of BOOTx may impact narrow pulse width operation, especially at load currents less than 1 A. See SW Node Ringing for further information on reducing noise on the SWx node.

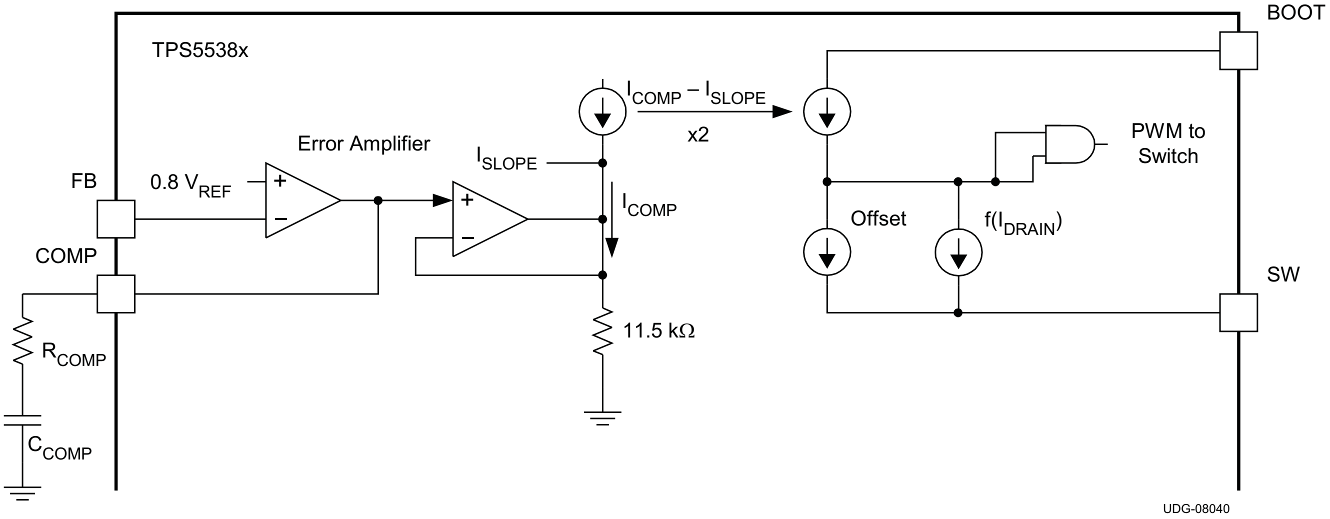


Figure 22. Feedback Loop Equivalent Circuit

A more conventional small-signal equivalent block diagram is shown in Figure 23. Here, the full closed-loop signal path is shown. Because the TPS5538x contains internal slope compensation, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability.

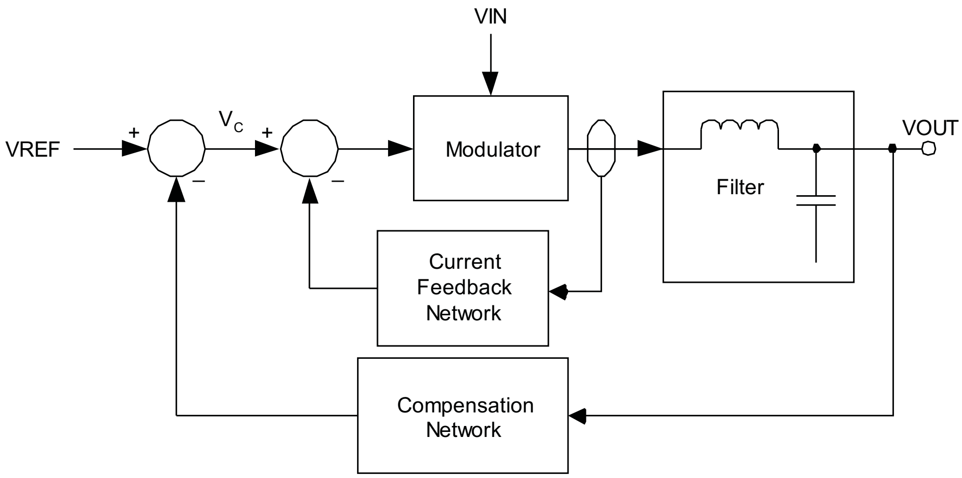


Figure 23. Small Signal Equivalent Block Diagram

Inductor Selection

Calculate the inductance value so that an output ripple current between 300 mA and 900 mA results. Lower ripple current results in discontinuous mode (DCM) operation at a lower DC load current, while higher ripple current generally allows for higher closed loop bandwidth.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{OUT}} \tag{3}$$

NOTE:

For wide input range converters, highest input voltage results in the highest ripple current.

NOTE:

The load current at which the overcurrent protection (OCP) engages is dependent on the amount of ripple current, because it is the peak current in the switch that is monitored. See Output Overload Protection.

Maximum Output Capacitance

With internal pulse-by-pulse current limiting and a fixed soft-start time, there is a maximum output capacitance which may be used before startup problems begin to occur. If the output capacitance is large enough so that the device enters a current-limit protection mode during startup, then there is a possibility that the output never reaches regulation. Instead, the TPS5538x simply shuts down and attempts a restart as if the output were short-circuited to ground. The maximum output capacitance (including bypass capacitance distributed at the load) is given by Equation 4:

$$C_{OUT(max)} = \frac{t_{SS}}{V_{OUT}} \left(I_{CLx} - \left(\frac{1}{2} \times I_{RIPPLE} \right) - I_{LOAD} \right) \tag{4}$$

Minimum Output Capacitance

Ensure the value of capacitance selected for closed-loop stability is compatible with the requirements of *Soft Start*.

Compensation For The Feedback Loop

To determine the components necessary for compensating the feedback loop, the controller frequency response characteristics must be understood and the desired crossover frequency selected. The best results are obtained if 10% of the switching frequency is used as this closed loop crossover frequency. In some cases, up to 20% of the switching frequency is also possible.

With the output filter components selected, the next step is to calculate the DC gain of the modulator. For the TPS55386:

$$Fm_{TPS55386} = \frac{600000}{\left[19.7 \times e^{\left(1.5 \times 10^{6} \times t_{ON}\right)} + 50 \times 10^{-6} \times \left(\frac{V_{IN} - V_{OUT}}{L} \right) \right]} \tag{5}$$

The gain of the TPS55383 modulator is approximated by:

$$Fm_{TPS55383} = \frac{300000}{\left[19.7 \times e^{\left(5.6 \times 10^{5} \times t_{ON}\right)} + 50 \times 10^{-6} \times \left(\frac{V_{IN} - V_{OUT}}{L}\right)\right]} \tag{6}$$

The overall DC gain of the of the converter control-to-output transfer function is approximated by:

$$fc = \frac{V_{IN} \times Fm \times 2 \times 10^{-4}}{\left(1 + \left(\frac{V_{IN} \times Fm \times 50 \times 10^{6}}{R_{LOAD}}\right)\right)} \tag{7}$$

The next step is to find the desired gain of the error amplifier at the desired crossover frequency. Assuming a single pole roll off, evaluate the following expression at the desired crossover frequency.

$$K_{EA} = -20 \times \log\left(\frac{fc}{1 + 2\pi \times f_{CO} \times R_{LOAD} \times C_{OUT}}\right) \tag{8}$$

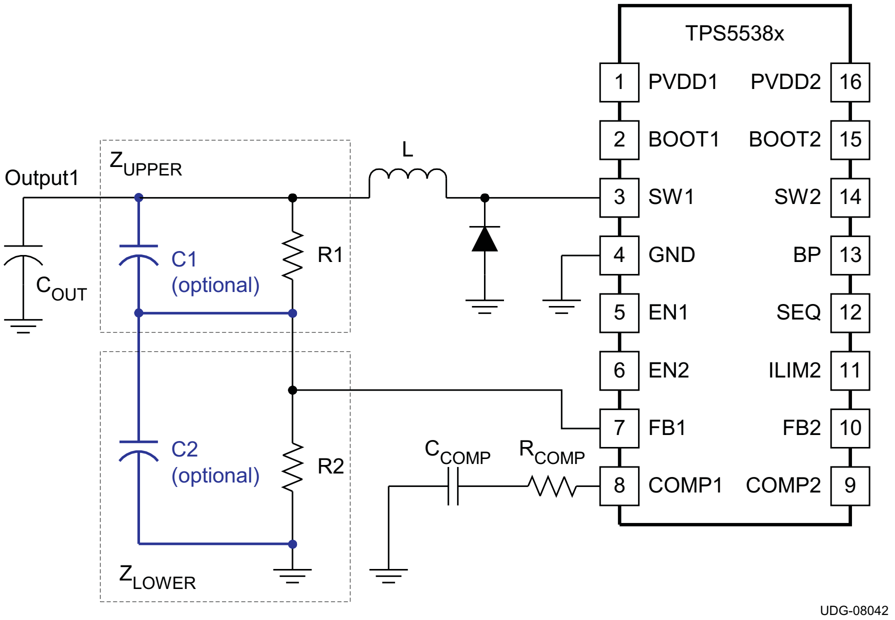


Figure 24. Loop Compensation Components

If operating at wide duty cycles (over 50%), a capacitor may be necessary across the upper resistor of the voltage setting divider. (Ref Figure 24) If duty cycles are less than 50%, this capacitor may be omitted.

$$C1 = \frac{\sqrt{L \times C_{OUT}}}{R1} \tag{9}$$

If a high ESR capacitor is used in the output filter, a zero appears in the loop response that could lead to instability. To compensate, a small capacitor is placed in parallel with the lower voltage setting divider resistor (Ref Figure 24). The value of the capacitor is determined such that a pole is placed at the same frequency as the ESR zero. If low ESR capacitors are used, this capacitor may be omitted.

$$C2 = C_{OUT} \times \frac{R_{ESR} \times (R2 + R1)}{R2 \times R1} \tag{10}$$

Next, calculate the value of the error amplifier gain setting resistor and capacitor.

$$R_{COMP} = \frac{10^{\frac{K_{EA}}{20}} \times (Z_{LOWER} + Z_{UPPER})}{g_M \times Z_{LOWER}} \tag{11}$$

$$C_{COMP} = \frac{1}{2\pi \times f_{POLE} \times R_{COMP}} \tag{12}$$

where

$$f_{POLE} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \tag{13}$$

NOTE:

Once the filter and compensation component values have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

Bootstrap for the N-Channel MOSFET

A bootstrap circuit provides a voltage source higher than the input voltage and of sufficient energy to fully enhance the switching MOSFET each switching cycle. The PWM duty cycle is limited to a maximum of 90%, allowing an external bootstrap capacitor to charge through an internal synchronous switch (between BP and BOOTx) during every cycle. When the PWM switch is commanded to turn ON, the energy used to drive the MOSFET gate is derived from the voltage on this capacitor.

To allow the bootstrap capacitor to charge each switching cycle, an internal pulldown MOSFET (from SW to GND) is turned ON for approximately 140 ns at the beginning of each switching cycle. In this way, if, during light load operation, there is insufficient energy for the SW node to drive to ground naturally, this MOSFET forces the SW node toward ground and allow the bootstrap capacitor to charge.

Because this is a charge transfer circuit, care must be taken in selecting the value of the bootstrap capacitor. It must be sized such that the energy stored in the capacitor on a per cycle basis is greater than the gate charge requirement of the MOSFET being used.

DESIGN HINT

For the bootstrap capacitor, use a ceramic capacitor with a value between 22 nF and 82 nF.

NOTE:

For 5-V input applications, connect PVDDx to BP directly. This connection bypasses the internal control circuit regulator and provides maximum voltage to the gate drive circuitry. In this configuration, shutdown mode $IDD_{SDN}$is the same as quiescent IDD_Q.

Operating Near Maximum Duty Cycle

If the TPS5538x operates at maximum duty cycle, and if the input voltage is insufficient to support the output voltage (at full load or during a load current transient), then there is a possibility that the output voltage will fall from regulation and trip the output UV comparator. If this should occur, the TPS5538x protection circuitry declares a fault and enter a shut down-and-restart cycle.

DESIGN HINT

Ensure that under ALL conditions of line and load regulation, there is sufficient duty cycle to maintain output voltage regulation.

To calculate the operating duty cycle, use Equation 14.

$$\delta = \frac{V_{OUT} + V_{DIODE}}{V_{IN} + V_{DIODE}} \tag{14}$$

where

- V_{DIODE} is the forward voltage drop of the rectifier diode

Light Load Operation

There is no special circuitry for pulse skipping at light loads. The normal characteristic of a nonsynchronous converter is to operate in the *discontinuous conduction mode* (DCM) at an average load current less than one-half of the inductor peak-to-peak ripple current. Note that the amplitude of the ripple current is a function of input voltage, output voltage, inductor value, and operating frequency, as shown in Equation 15.

$$I_{DCM} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times \delta \times T_S \tag{15}$$

During discontinuous mode operation the commanded pulse width may become narrower than the capability of the converter to resolve. To maintain the output voltage within regulation, skipping switching pulses at light load conditions is a natural by-product of that mode. This condition may occur if the output capacitor is charged to a value greater than the output regulation voltage and there is insufficient load to discharge the capacitor. A by-product of pulse skipping is an increase in the peak-to-peak output ripple voltage.

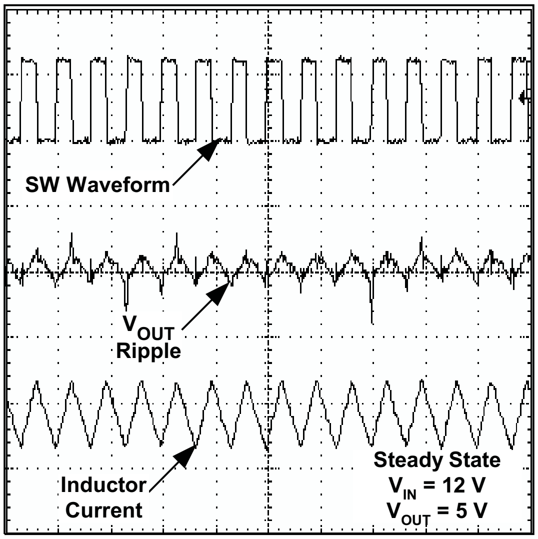


Figure 25. Steady State

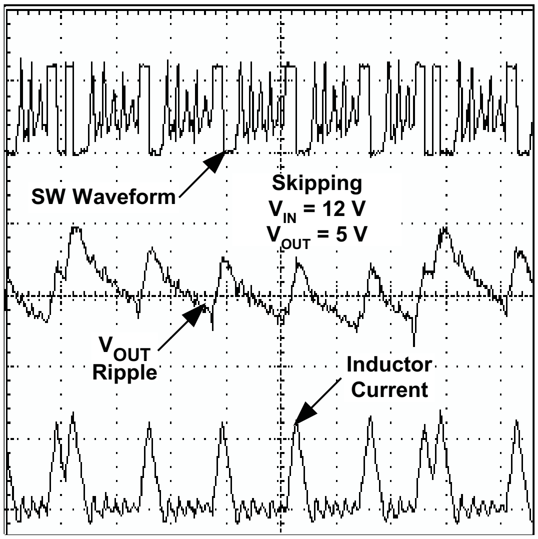


Figure 26. Skipping

DESIGN HINT

If additional output capacitance is required to reduce the output voltage ripple during DCM operation, be sure to recheck the Maximum Output Capacitance section.

SW Node Ringing

A portion of the control circuitry is referenced to the SW node. To ensure jitter-free operation, it is necessary to decrease the voltage waveform ringing at the SW node to less than 5-V peak and of a duration of less than 30-ns. In addition to following good printed circuit board (PCB) layout practices, there are a couple of design techniques for reducing ringing and noise.

SW Node Snubber

Voltage ringing at the SW node is caused by fast switching edges and parasitic inductance and capacitance. If the ringing results in excessive voltage on the SW node, or erratic operation of the converter, an R-C snubber may be used to dampen the ringing and ensure proper operation over the full load range.

DESIGN HINT

> A series-connected R-C snubber (C = between 330 pF and 1 nF, R = 10 Ω) connected from SW to GND reduces the ringing on the SW node.

Bootstrap Resistor

A small resistor in series with the bootstrap capacitor reduces the turn-on time of the internal MOSFET, thereby reducing the rising edge ringing of the SW node.

DESIGN HINT

> A resistor with a value between 1 Ω and 3 Ω may be placed in series with the bootstrap capacitor to reduce ringing on the SW node.

DESIGN HINT

> Placeholders for these components should be placed on the initial prototype PCBs in case they are needed.

Output Overload Protection

In the event of an overcurrent during soft-start on either output (such as starting into an output short), pulse-by-pulse current limiting and PWM frequency division are in effect for that output until the internal soft-start timer ends. At the end of the soft-start time, a UV fault is declared. During this fault, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This process ensures that both outputs discharge to GND in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup* mode timeout before attempting to restart. *Frequency Division* describes a condition when an overcurrent pulse is detected and six clock cycles are skipped before a next PWM pulse is initiated, effectively dividing the operating frequency by six and preventing excessive current build up in the inductor.

In the event of an overcurrent condition on either output after the output reaches regulation, pulse-by-pulse current limit is in effect for that output. In addition, an output undervoltage (UV) comparator monitors the FBx voltage (that follows the output voltage) to declare a fault if the output drops below 85% of regulation. During this fault condition, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This design ensures that both outputs discharge to GND, in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup* mode timeout before attempting to restart.

The overcurrent threshold for Output 1 is set nominally at 4.5 A. The overcurrent level of Output 2 is determined by the state of the ILIM2 pin. The ILIM setting of Output 2 is not latched in place and may be changed during operation of the converter.

Table 2. Current Limit Threshold Adjustment for Output 2

ILIM2 Connection	OCP Threshold for Output 2
BP	4.5 A nominal setting
(floating)	3.0 A nominal setting
GND	1.5 A nominal setting

DESIGN HINT

The OCP threshold refers to the peak current in the internal switch. Be sure to add one-half of the peak inductor ripple current to the dc load current in determining how close the actual operating point is to the OCP threshold.

Dual Supply Operation

It is possible to operate a TPS5538x from two supply voltages. If this application is desired, then the sequencing of the supplies must be such that PVDD2 is above the UVLO voltage before PVDD1 begins to rise. This level requirement ensures that the internal regulator and the control circuitry are in operation before PVDD1 supplies energy to the output. In addition, Output 1 must be held in the disabled state ($\overline{\text{EN1}}$ high) until there is sufficient voltage on PVDD1 to support Output 1 in regulation. (See the *Operating Near Maximum Duty Cycle* section.)

The preferred sequence of events is:

1. PVDD2 rises above the input UVLO voltage
2. PVDD1 rises with Output 1 disabled until PVDD1 rises above level to support Output 1 regulation.

   With these two conditions satisfied, there is no restriction on PVDD2 to be greater than, or less than PVDD1.

DESIGN HINT

An R-C delay on $\overline{\text{EN1}}$ may be used to delay the startup of Output 1 for a long enough period of time to ensure that PVDD1 can support Output 1 load.

Cascading Supply Operation

It is possible to source PVDD1 from Output 2 as depicted in Figure 27 and Figure 28. This configuration may be preferred if the input voltage is high, relative to the voltage on Output 1.

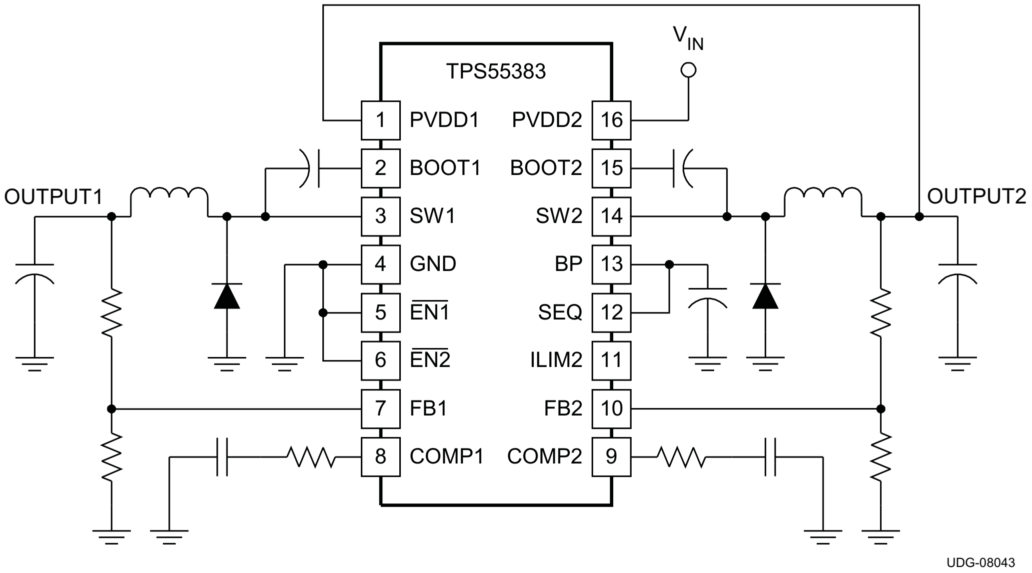


Figure 27. Schematic Showing Cascading PVDD1 from Output 2

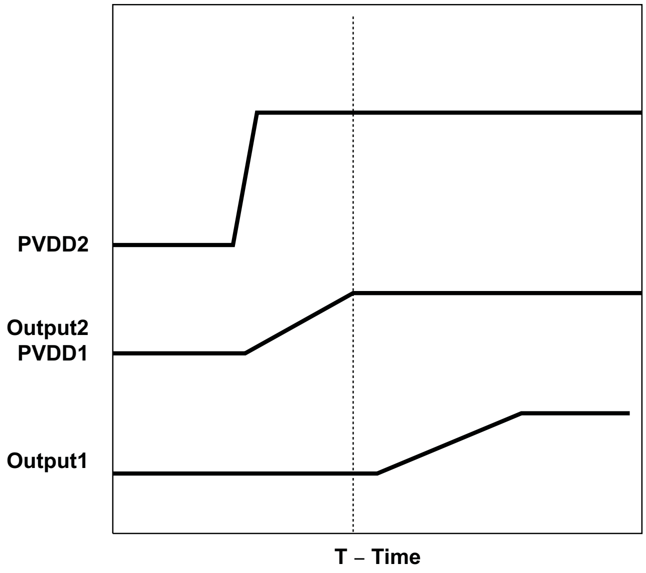


Figure 28. Waveforms Resulting from Cascading PVDD1 from Output 2

In this configuration, the following conditions must be maintained:

1. Output 2 must be of a voltage high enough to maintain regulation of Output 1 under all load conditions.
2. The sum of the current drawn by Output 2 load plus the current into PVDD1 must be less than the overload protection current level of Output 2.
3. The method of output sequencing must be such that the voltage on Output 2 is sufficient to support Output 1 before Output 1 is enabled. This requrement may be accomplished by:
   a. a delay of the enable function
   b. selecting sequential sequencing of Output 1 starting after Output 2 is in regulation

Multiphase Operation

The TPS5538x may be configured to operate as a two-channel multiphase converter capable of delivering up to 6 A. Figure 29 indicates the recommended pin connections. In this configuration, FB2 must be tied to BP for the maximum current configuration and the two output filter inductors must be the same value. Calculate R_{COMP} and C_{COMP} as outlined for a single channel output, then use one-half the R_{COMP} value and two times the C_{COMP} value as the compensation components. Contact the factory for further support.

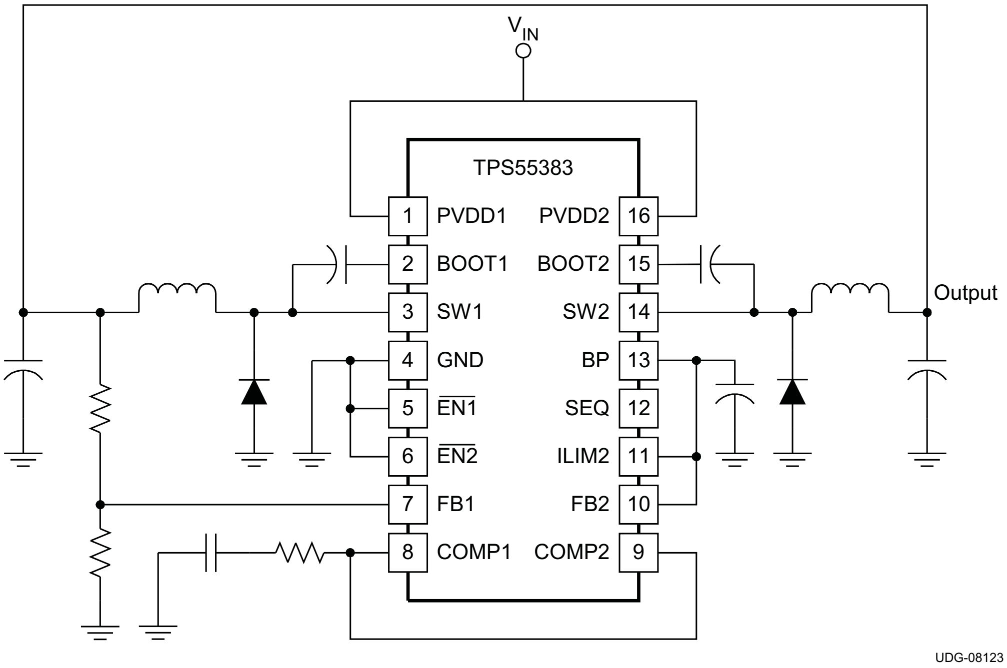


Figure 29. Multiphase Operation Schematic

Bypass and FIltering

As with any integrated circuit, supply bypassing is important for jitter-free operation. To improve the noise immunity of the converter, ceramic bypass capacitors must be placed as close to the package as possible.

1. PVDD1 to GND: Use a 10-µF ceramic capacitor
2. PVDD2 to GND: Use a 10-µF ceramic capacitor
3. BP to GND: Use a 4.7-µF to 10-µF ceramic capacitor

Overtemperature Protection and Junction Temperature Rise

The overtemperature thermal protection limits the maximum power to be dissipated at a given operating ambient temperature. In other words, at a given device power dissipation, the maximum ambient operating temperature is limited by the maximum allowable junction operating temperature. The device junction temperature is a function of power dissipation, and the thermal impedance from the junction to the ambient. If the internal die temperature should reach the thermal shutdown level, the TPS5538x shuts off both PWMs and remains in this state until the die temperature drops below the hysteresis value, at which time the device restarts.

The first step to determine the device junction temperature is to calculate the power dissipation. The power dissipation is dominated by the two switching MOSFETs and the BP internal regulator. The power dissipated by each MOSFET is composed of conduction losses and output (switching) losses incurred while driving the external rectifier diode. To find the conduction loss, first find the RMS current through the upper switch MOSFET.

$$I_{RMS(outputx)} = \sqrt{D \times \left(\left(I_{OUTPUTx}\right)^2 + \left(\frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)} \tag{16}$$

where

- D is the duty cycle
- $I_{OUTPUTx}$ is the dc output current
- $\Delta I_{OUTPUTx}$ is the peak ripple current in the inductor for Outputx

Notice the impact of the operating duty cycle on the result.

Multiplying the result by the $R_{DS(on)}$ of the MOSFET gives the conduction loss.

$$P_{D(cond)} = I_{RMS(outputx)}{}^{2} \times R_{DS(on)} \tag{17}$$

The switching loss is approximated by:

$$P_{D(SW)} = \left[\frac{(V_{IN})^{2} \times C_{J} \times f_{S}}{2}\right] \tag{18}$$

where

- where C_J is the prallel capacitance of the rectifier diode and snubber (if any)
- f_S is the switching frequency

The total power dissipation is found by summing the power loss for both MOSFETs plus the loss in the internal regulator.

$$P_{D} = P_{D(cond)output1} + P_{D(SW)output1} + P_{D(cond)output2} + P_{D(SW)output2} + V_{IN} \times Iq \tag{19}$$

The temperature rise of the device junction depends on the thermal impedance from junction to the mounting pad (See the *Package Dissipation Ratings* table), plus the thermal impedance from the thermal pad to ambient. The thermal impedance from the thermal pad to ambient depends on the PCB layout (PowerPAD interface to the PCB, the exposed pad area) and airflow (if any). See the *PCB Layout Guidelines, Additional References* section.

The operating junction temperature is shown in Equation 20.

$$T_{J} = T_{A} + P_{D} \times \left(\theta_{TH(pkg)} + \theta_{TH(pad-amb)}\right) \tag{20}$$

Power Derating

The TPS5538x delivers full current at ambient temperatures up to +85°C if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level. At higher ambient temperatures, the device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 30 illustrates the power derating for elevated ambient temperature under various airflow conditions. Note that these curves assume that the PowerPAD is properly soldered to the recommended thermal pad. (See the *References* section for further information.)

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

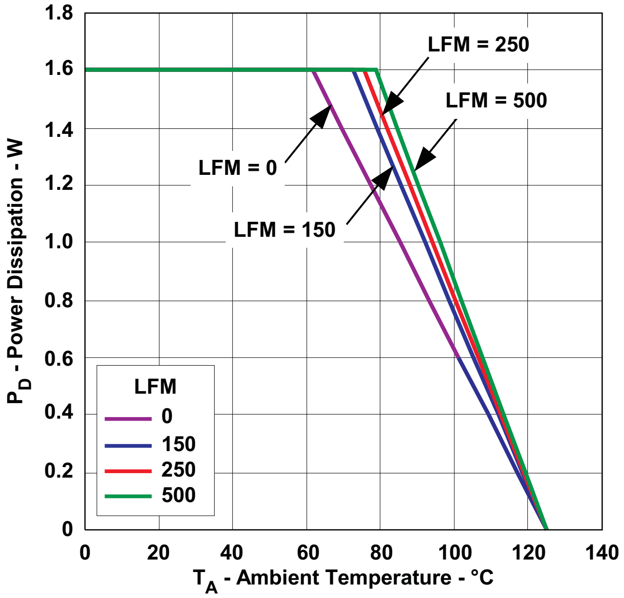


Figure 30. Power Derating Curves

PowerPAD Package

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD package. Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) work well when 1-oz. copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. (See the *Additional References* section.)

PCB Layout Guidelines

The layout guidelines presented here are illustrated in the PCB layout examples given in Figure 31 and Figure 32.

- Power pad must be connected to low current ground with available surface copper to dissipate heat. Recommend extending ground land beyond device package area.
- Connect the GND pin to the PowerPAD through a 10-mil (.010 in, or 0.0254 mm) wide trace.
- Place the ceramic input capacitors close to PVDD1 and PVDD2; Connect ceramic input capacitor ground to PowerPad with min 50mil wide trace.
- Maintain tight loop of wide traces from SW1 or SW2 through switch node, inductor, output capacitor and rectifier diode. Avoid using vias in this loop.
- Use wide ground connection from input capacitor to rectifier diode as close to power path as possible. Recommend directly under diode and switch node.
- Locate bootstrap capacitor close to BOOT pin to minimize gate drive loop.
- Locate feedback and compensation components over GND and away from switch node and rectifier diode to input capacitor ground connection.
- Locate snubber components close to rectifier diode with minimize loop area.
- Locate BP bypass capacitor very close to device. Recommend minimal loop area.
- Locate output ceramic capacitor close to inductor output terminal between inductor and electrolytic capacitors if used.

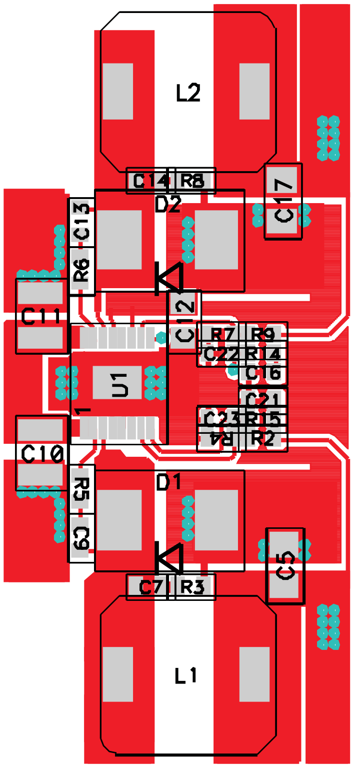


Figure 31. Top Layer Copper Layout and Component Placement

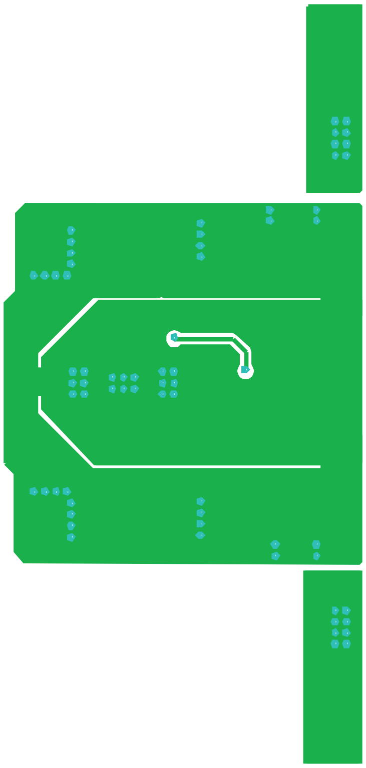


Figure 32. Bottom Layer Copper Layout

DESIGN EXAMPLES

Example 1: Detailed Design of a 12-V to 5-V and 3.3-V Converter

DESIGN EXAMPLE 1 GENERAL DESCRIPTION

The following example illustrates a design process and component selection for a 12-V to 5-V and 3.3-V dual non-synchronous buck regulator using the TPS55386 converter. *Design Example*, and *List of Materials* is found at the end of this section.

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input Voltage		9.6	12.0	13.2	V
I_{IN}	Input Current	V_{IN} = Nom, I_{OUT1} = I_{OUT2} = Max		2.4	2.6	A
	No Load Input Current	V_{IN} = Nom, I_{OUT} = 0 A		12	20	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = Min to Max	4.0	4.2	4.4	V
OUTPUT CHARACTERISTICS						
V_{OUT1}	Output Voltage 1	V_{IN} = Nom, I_{OUT} = Nom	4.80	5.0	5.20	V
V_{OUT2}	Output Voltage 2	V_{IN} = Nom, I_{OUT} = Nom	3.20	3.3	3.40	V
	Line Regulation	V_{IN} = Min to Max			1%	
	Load Regulation	I_{OUT} = Min to Max			1%	
V_{OUT_ripple}	Output Voltage Ripple	V_{IN} = Nom, I_{OUT} = Max			50	mVpp
I_{OUT1}	Output Current 1	V_{IN} = Min to Max	0		3.0	A
I_{OUT2}	Output Current 2	V_{IN} = Min to Max	0		3.0	A
I_{OCP1}	Output Over Current Channel 1	V_{IN} = Nom, VOUT = V_{OUT1}–5%	3.3	4.2	5.2	A
I_{OCP2}	Output Over Current Channel 2	V_{IN} = Nom, VOUT = V_{OUT2}–5%	3.3	4.2	5.2	A
	Transient Response					
	ΔVout from load transient	ΔI_{OUT} = 1 A at 3 A/µs		200		mV
	Settling Time	To 1% of Vout		1		ms
SYSTEM CHARACTERISTICS						
f_{SW}	Switching Frequency		500	600	700	kHz
η_{pk}	Peak Efficiency	V_{IN} = Nom, I_{OUT1} = I_{OUT2}		93%		
η	Full Load Efficiency	VI_{N} = Nom, I_{OUT1} = I_{OUT2} = Max		86%		
Top	Operating Temperature Range	V_{IN} = Min to Max, I_{OUT} = Min to Max	0	25	60	°C

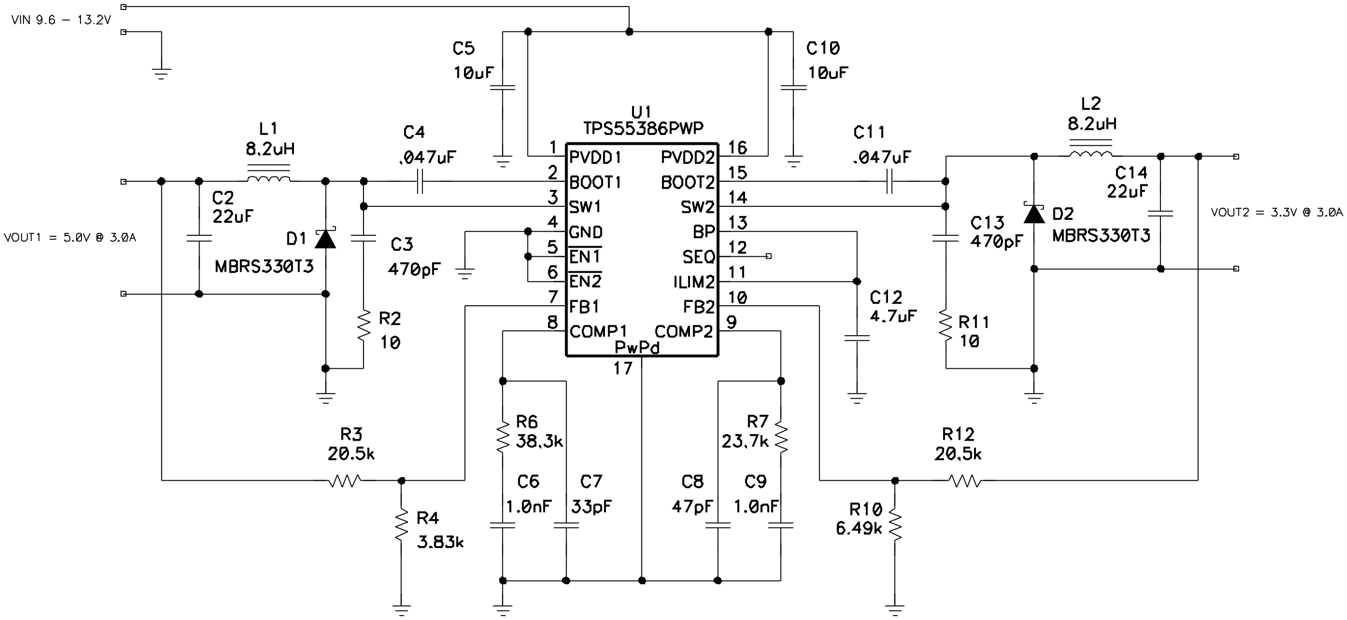


Figure 33. Design Example Schematic

The bill of materials for this application is shown below in Table 3. The efficiency, line and load regulation measurements from boards built using this design are shown in Figure 34 and Figure 35.

DESIGN EXAMPLE 1 STEP-BY-STEP DESIGN PROCEDURE

Duty Cycle Estimation

The duty cycle of the main switching FET of each channel is estimated by:

$$D_{MAX1} \approx \frac{V_{OUT1} + V_{FD}}{V_{IN(min)} + V_{FD}} = \frac{5.0 + 0.4}{9.6 + 0.4} = 0.540 \tag{21}$$

$$D_{MAX2} \approx \frac{V_{OUT2} + V_{FD}}{V_{IN(min)} + V_{FD}} = \frac{3.3 + 0.4}{9.6 + 0.4} = 0.370 \tag{22}$$

$$D_{MIN1} \approx \frac{V_{OUT1} + V_{FD}}{V_{IN(max)} + V_{FD}} = \frac{5.0 + 0.4}{13.2 + 0.4} = 0.397 \tag{23}$$

$$D_{MIN2} \approx \frac{V_{OUT2} + V_{FD}}{V_{IN(max)} + V_{FD}} = \frac{3.3 + 0.4}{13.2 + 0.4} = 0.272 \tag{24}$$

Inductor Selection

The peak-to-peak ripple is to be limited to 25% of the max output current, so that

$$I_{Lrip(max)} = 0.25 \times I_{OUT(max)} = 0.25 \times 3.0\,A = 0.750\,A \tag{25}$$

The minimum inductor size is estimated by:

$$L_{min1} \approx \frac{V_{IN(max)} - V_{OUT1}}{I_{Lrip1(max)}} \times D_{min1} \times \frac{1}{f_{SW}} = \frac{13.2 - 5.0}{0.75\,A} \times 0.397 \times \frac{1}{600\,kHz} = 7.23\,\mu H \tag{26}$$

$$L_{min2} \approx \frac{V_{IN(max)} - V_{OUT2}}{I_{Lrip2(max)}} \times D_{min2} \times \frac{1}{f_{SW}} = \frac{13.2 - 3.3}{0.75\,A} \times 0.272 \times \frac{1}{600\,kHz} = 6.0\,\mu H \tag{27}$$

The standard inductor value of 8.2 µH is selected for both Channel 1 and Channel 2. The resulting ripple currents are estimated by:

$$I_{RIPPLE1} \approx \frac{V_{IN(max)} - V_{OUT1}}{L_1} \times D_{min1} \times \frac{1}{f_{SW}} = \frac{13.2 - 5.0}{8.2\,\mu H} \times 0.397 \times \frac{1}{600\,kHz} = 0.661A \tag{28}$$

$$I_{RIPPLE2} \approx \frac{V_{IN(max)} - V_{OUT2}}{L_2} \times D_{min2} \times \frac{1}{f_{SW}} = \frac{13.2 - 3.3}{8.2\,\mu H} \times 0.272 \times \frac{1}{600\,kHz} = 0.547\,A \tag{29}$$

RMS current through the inductor is approximated by:

$$I_{L1(rms)} = \sqrt{\left(I_{L1(avg)}\right)^2 + {}^{1}\!/_{12}\left(I_{RIPPLE1}\right)^2} \approx \sqrt{\left(I_{OUT1(max)}\right)^2 + {}^{1}\!/_{12}\left(I_{RIPPLE1}\right)^2} = \sqrt{(3.0)^2 + {}^{1}\!/_{12}(0.661)^2}\,A = 3.0\,A \tag{30}$$

$$I_{L2(rms)} = \sqrt{\left(I_{L2(avg)}\right)^2 + {}^{1}\!/_{12}\left(I_{RIPPLE2}\right)^2} \approx \sqrt{\left(I_{OUT2(max)}\right)^2 + {}^{1}\!/_{12}\left(I_{RIPPLE2}\right)^2} = \sqrt{(3.0)^2 + {}^{1}\!/_{12}(0.547)^2}\,A = 3.0\,A \tag{31}$$

The RMS inductor current is 3.0 for both channels.

A DC current with 30% peak to peak ripple has an RMS current approximately 0.4% above the average current.

The peak inductor current is estimated by:

$$I_{L1(peak)} \approx I_{OUT1(max)} + \frac{1}{2} I_{RIPPLE} = 3.0\,A + \frac{1}{2} 0.661\,A = 3.3\,A \tag{32}$$

$$I_{L2(peak)} \approx I_{OUT2(max)} + \frac{1}{2} I_{RIPPLE} = 3.0\,A + \frac{1}{2} 0.547\,A = 3.3\,A \tag{33}$$

An 8.2-µH inductor with a minimum RMS current rating of 3.0 A and minimum saturation current rating of 3.3 A must be selected. A Coilcraft MSS1048-822ML 8.2-µH, 4.38-A inductor is chosen for both outputs.

Rectifier Diode Selection

A low forward voltage drop schottky diode is used as a rectifier diode to minimize power dissipation and maximize efficiency.

$$V_{(BR)R(min)} \geq \frac{V_{IN(max)}}{0.8} = 1.25 \times V_{IN(max)} = 1.25 \times 13.2\,V = 16.5\,V \tag{34}$$

Allowing 20% over VIN for ringing on the switch node, the rectifier diode's minimum reverse break-down voltage is given by:

$$I_{D1(avg)} \approx I_{OUT1(max)} \times \left(1 - D_{MIN1}\right) = 3.0\,A \times (1 - 0.397) = 1.81\,A \tag{35}$$

$$I_{D2(avg)} \approx I_{OUT2(max)} \times \left(1 - D_{MIN2}\right) = 3.0\,A \times (1 - 0.272) = 2.18\,A \tag{36}$$

$$I_{D(peak)} = I_{L(peak)} \tag{37}$$

Reviewing 20-V and 30-V schottky diodes, the MBRS330T3, 30-V, 3-A diodes in an SMC package are selected for both channels. This diode has a forward voltage drop of 0.4 V at 3 A, so the conduction power dissipation is:

$$P_{D1(max)} \approx V_{FM} \times I_{D1(avg)} \approx 0.4\,V \times 1.81 = 0.72\,W \tag{38}$$

$$P_{D2(max)} \approx V_{FM} \times I_{D2(avg)} \approx 0.4\,V \times 2.18 = 0.87\,W \tag{39}$$

For this design, the maximum power dissipation is estimated as 0.72 W and 0.87 W respectively.

Output Capacitor Selection

Output capacitors are selected to support load transients and output ripple current. The minimum output capacitance to meet the transient specification is given by:

$$C_{OUT1(min)} = \frac{\left(I_{TRAN(MAX)}\right)^2 \times L}{\left(V_{OUT1}\right) \times V_{OVER}} = \frac{(1A)^2 \times 8.2\,\mu H}{5.0\,V \times 0.2\,V} = 8.2\,\mu F \tag{40}$$

$$C_{OUT2(min)} = \frac{\left(I_{TRAN(MAX)}\right)^2 \times L}{\left(V_{OUT2}\right) \times V_{OVER}} = \frac{(1A)^2 \times 8.2\,\mu H}{3.3\,V \times 0.2\,V} = 12.4\,\mu F \tag{41}$$

The maximum ESR to meet the ripple specification is given by:

$$\mathrm{ESR1}_{(max)} = \frac{V_{RIPPLE1(total)} - \left(\frac{I_{RIPPLE1}}{8 \times C_{OUT1} \times f_{SW}}\right)}{I_{RIPPLE1}} = \frac{0.050\,\mathrm{V} - \left(\frac{0.661\,\mathrm{A}}{8 \times 8.2\,\mu\mathrm{F} \times 600\,\mathrm{kHz}}\right)}{0.661\,\mathrm{A}} = 0.024\,\Omega\mathrm{F} \tag{42}$$

$$\mathrm{ESR}_{(max)} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT1} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{0.050\,\mathrm{V} - \left(\frac{0.547\,\mathrm{A}}{8 \times 12.4\,\mu\mathrm{F} \times 600\,\mathrm{kHz}}\right)}{0.547\,\mathrm{A}} = 0.033\,\Omega\mathrm{F} \tag{43}$$

A single 22-µF ceramic capacitor with approximately 2.5 mΩ of ESR is selected to provide sufficient margin for capacitance loss due to DC voltage bias.

Input Capacitor Selection

The TPS55386 datasheet recommends a 10µF (minimum) ceramic bypass capacitor on each PVDD pin. While out of phase operation reduces input RMS current, the input capacitors must be sized to support the greater of the two input RMS currents, or 1.5A to allow operation when one channel is at maximum load and the other is un-loaded. The ceramic capacitor must handle the RMS input ripple current of the converter.

The RMS current in the input capacitors is estimated by:

$$I_{RMS\_CIN} = I_{OUT} \times \sqrt{D \times (1 - D)} = 3\,\mathrm{A} \times \sqrt{0.5 \times (1 - 0.5)} = 1.5\,\mathrm{A} \tag{44}$$

One 1210 size 10-µF, 25-V, X5R ceramic capacitor with a 2-mΩ ESR and a 2-A RMS current rating are selected to bypass each PVDD input. Higher voltage capacitors minimize capacitance loss under DC bias voltage, ensuring the capacitors have sufficient capacitance at their working voltage.

Voltage Feedback

The primary feedback divider resistor (R_{FB}) from V_{OUT} to FB should be selected between 10 kΩ and 100 kΩ to maintain a balance between power dissipation and noise sensitivity. For a 3.3-V and 5-V output, 20.5 kΩ is selected, so the lower resistor is given by:

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{V_{OUT} - V_{FB}} \tag{45}$$

For R_{FB} = R2 = R9 = 20.5 kΩ and V_{FB} = 0.80V, R_{BIAS1} = 3.90kΩ and R_{BIAS2} = 6.5kΩ (R4 = 3.83kΩ and
R7 = 6.49 kΩ selected) for 5.0 V and 3.3 V respectively.

Compensation Components

The TPS55386 controller uses an internal transconductance error amplifier, which compares the feedback voltage to the internal 0.80-V reference and sources a current proportional to the resulting error out of the COMP pin. A series resistor and capacitor to ground generate an integrator with zero while a high frequency capacitor provides a second pole to reduce the high frequency gain. The compensation loop components are selected by the following equations with the 5.0-V output used in example calculations:

Calculate the modulator gain at DC:

$$F_{M1} = \frac{600000}{19.7 \times e^{\left(1.5 \times 10^{6} \times t_{ON}\right)} + 50 \times 10^{-6} \times \left(\frac{V_{IN} - V_{OUT1}}{L}\right)} = \frac{600000}{19.7 \times e^{\left(1.5 \times 10^{6} \times 6.68 \times 10^{-7}\right)} + 50 \times 10^{-6} \times \left(\frac{13.2 - 5.0}{8.2\,\mu\mathrm{H}}\right)} = 5.82 \times 10^{3} \tag{46}$$

Then calculate the converter gain at DC:

$$fc_1 = \frac{V_{IN} \times F_m \times 2 \times (10)^{-4}}{1 + \left(\frac{V_{IN} \times Fm \times 50 \times (10)^{-6}}{R_{LOAD1}} \right)} = \frac{13.2 \times 5.82 \times (10)^3 \times 2 \times (10)^{-4}}{1 + \left(\frac{13.2 \times 5.82 \times (10)^3 \times 50 \times (10)^{-6}}{1.67\Omega} \right)} = 4.63 \tag{47}$$

Calculate the required error amplifier gain at the desired crossover frequency of 35 kHz:

$$K_{EA1} = -20 \times \log\left(\frac{fc_1}{1 + 2\pi \times f_{CO} \times R_{LOAD1} \times C_{OUT1}} \right) = -20 \times \log\left(\frac{4.65}{1 + 2\pi \times 35\,kHz \times 1.67\,\Omega \times 22\,\mu F} \right) = 5.80\,dB \tag{48}$$

Then compensation resistor at the output of the error amplifier is:

$$R_{COMP1} = \frac{10^{\frac{K_{EA}}{20}} \times (Z_{LOWER} + Z_{UPPER})}{g_M \times Z_{LOWER}} = \frac{10^{\frac{5.80\,dB}{20}} \times (3.83\,k\Omega + 20.5\,k\Omega)}{315\,\mu S \times 3.83\,k\Omega} = 38.5\,k\Omega \Rightarrow R15 = 38.3\,k\Omega \tag{49}$$

Calculate the required compensation zero frequency:

$$f_{ZERO1} = \frac{1}{2\pi \times C_{OUT1} \times R_{LOAD1}} = \frac{1}{2\pi \times 22\,\mu F \times 1.67\,\Omega} = 4.4\,kHz \tag{50}$$

Then calculate the compensation capacitor:

$$C_{COMP1} = \frac{1}{2\pi \times f_{POLE1} \times R_{COMP1}} = \frac{1}{2\pi \times 4.4\,kHz \times 3.83\,k\Omega} = 967\,pF \Rightarrow C21 = 1nF \tag{51}$$

The high-frequency pole is placed at eight times the crossover frequency:

$$C_{HF1} = \frac{1}{2\pi \times 4 \times f_{CO} \times R_{COMP}} = \frac{1}{2\pi \times 4 \times 35\,kHz \times 38.3\,k\Omega} = 29.6\,pF \Rightarrow C23 = 33\,pF \tag{52}$$

Boot-Strap Capacitor

To ensure proper charging of the high-side FET gate and limit the ripple voltage on the boost capacitor, a 47-nF boot strap capacitor is used.

ILIM2

The current limit must be set above the peak inductor current I_{Lpeak}. Comparing I_{Lpeak} to the available minimum current limits, I_{LIM} is connected to BP for a 3.6-A minimum current limit.

SEQ

The SEQ pin is left floating, leaving the enable pins to function independently. If the enable pins are tied together, the two supplies start-up ratio-metrically. SEQ could also be connected to BP or GND to provide sequential start-up.

Power Dissipation

The power dissipation in the TPS55386 is from FET conduction losses, switching losses and regulator losses.

Conduction losses are estimated by:

$$P_{CON1} = R_{DS(on)} \times \left(I_{QSW(RMS)}\right)^2 \approx R_{DS(on)} \times \left(I_{OUT}\right)^2 \times \sqrt{D} = 0.085\,\Omega \times (3\,A)^2 \times \sqrt{0.540} = 0.562\,W \quad (53)$$

$$P_{CON2} = R_{DS(on)} \times \left(I_{QSW(RMS)}\right)^2 \approx R_{DS(on)} \times \left(I_{OUT}\right)^2 \times \sqrt{D} = 0.085\,\Omega \times (3\,A)^2 \times \sqrt{0.370} = 0.465\,W \quad (54)$$

The switching losses are estimated by:

$$P_{SW1} = P_{SW2} \approx \frac{\left(V_{IN(max)}\right)^2 \times (C_{Dj} + C_{OSS}) \times f_{SW}}{2} = \frac{(13.2)^2 \times (200\,pF + 250\,pF) \times 600\,kHz}{2} = 23.5\,mW \quad (55)$$

The regulator losses are estimated by:

$$P_{REG} \approx I_{DD} \times V_{IN(max)} + I_{BP} \times \left(V_{IN(max)} - V_{BP}\right) = 5\,mA \times 13.2\,V = 66\,mW \quad (56)$$

Total power dissipation in the device is the sum of conduction and switching losses for both channels plus regulator losses, and are estimated to total 1.2 W.

DESIGN EXAMPLE 1 TEST RESULTS

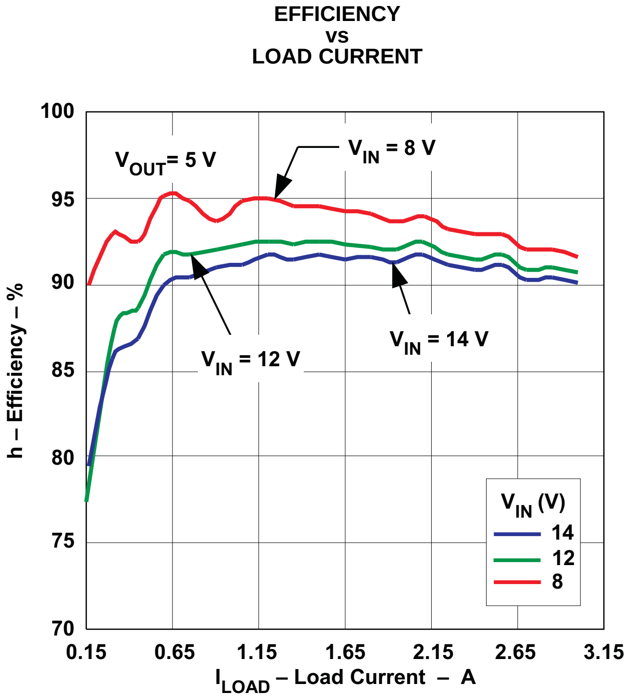


Figure 34.

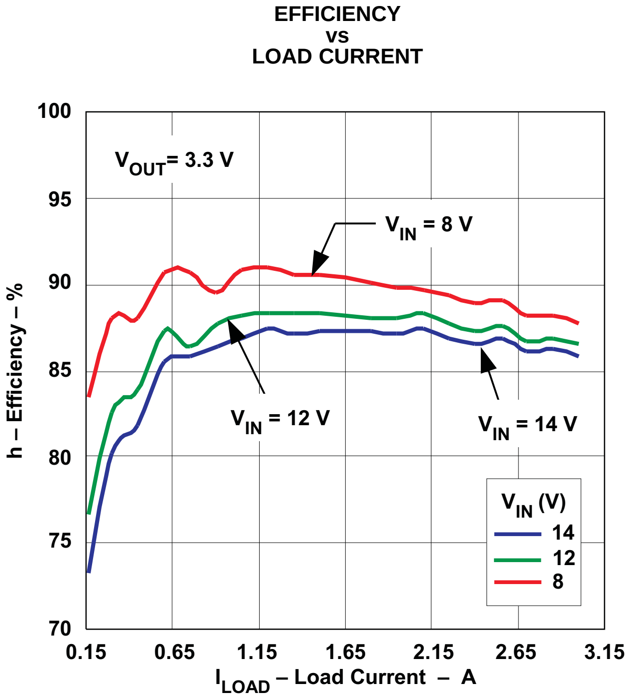


Figure 35.

Table 3. TPS55386 Design Example List of Materials

QTY	REFERENCE DESIGNATOR	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
2	C2, C14	22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	C3216X5R0J226M	TDK
2	C3, C13	470 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C4, C11	0.047 µF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C5, C10	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	C3225X5R1E106M	TDK
1	C12	4.7 µF	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
2	C9, C6	1.0 nF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C8	47 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C7	33 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	D1, D2	MBRS330T3	Diode, Schottky, 3-A, 30-V	SMC	MBRS330T3	OnSemi
2	L1, L2	8.2 µH	Inductor, SMT, 4.38A, 20milliohm	0.402 x 0.394 inch	MSS1048-822L	Coilcraft
1	R7	23.7 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	38.3 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R12	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R11	10 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R4	3.83 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	6.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS55386PWP	IC, Dual 600kHz Non-Sync BUCK with Interal FET	HTSSOP-16	TPS55386PWP	TI

Example 2: Cascading Configuration: 24 V to 12 V at 2 A then 3.3 V at 2 A

This example illustrates a cascaded configuration. To accommodate the low duty cycle of a 24-V to 3.3-V supply, PVDD1 is connected to VOUT2, a 12-V output. VOUT2 is used as the source supply for VOUT1. The sequence pin is connected to BP, ensuring the 12-V supply is in regulation before the 3.3-V is allowed to turn on.

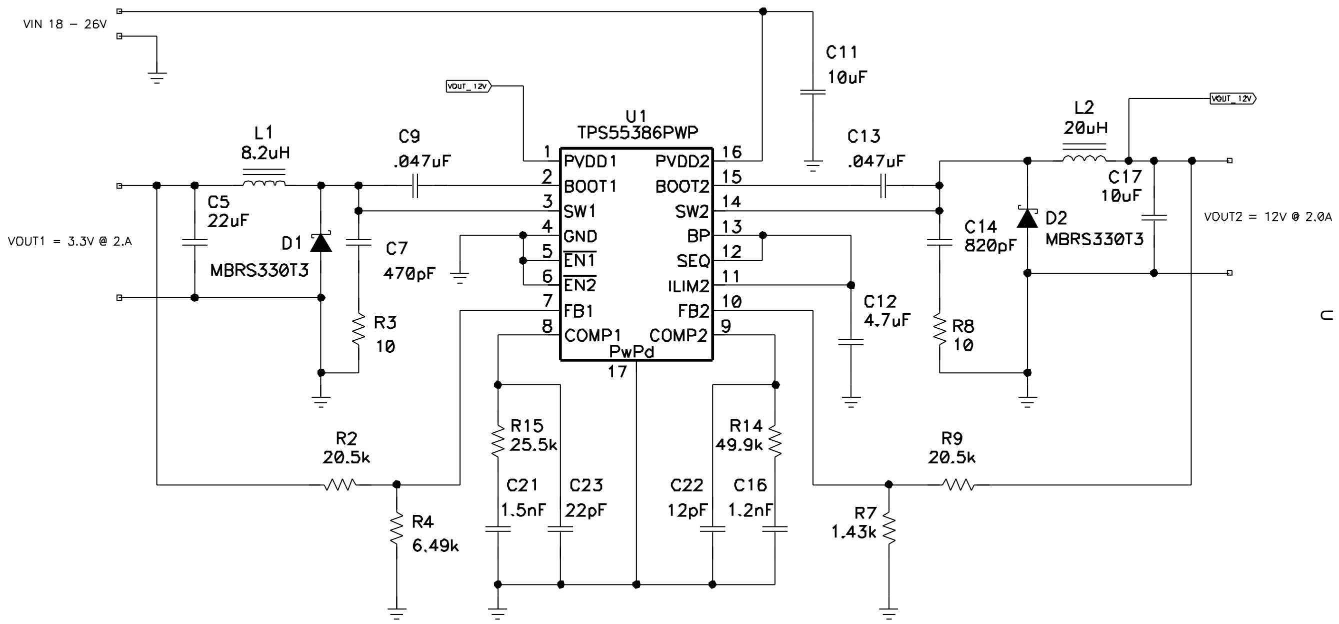


Figure 36. Design Example 2, TPS55386 in a Cascaded Configuration

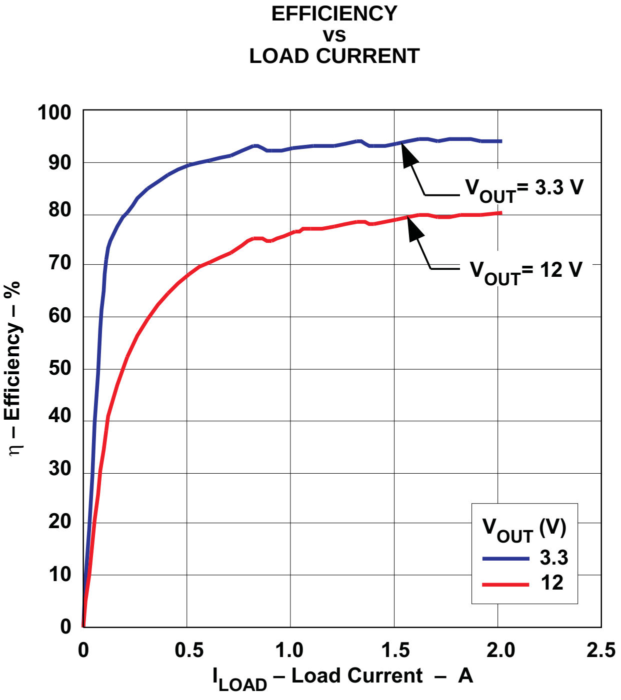


Figure 37.

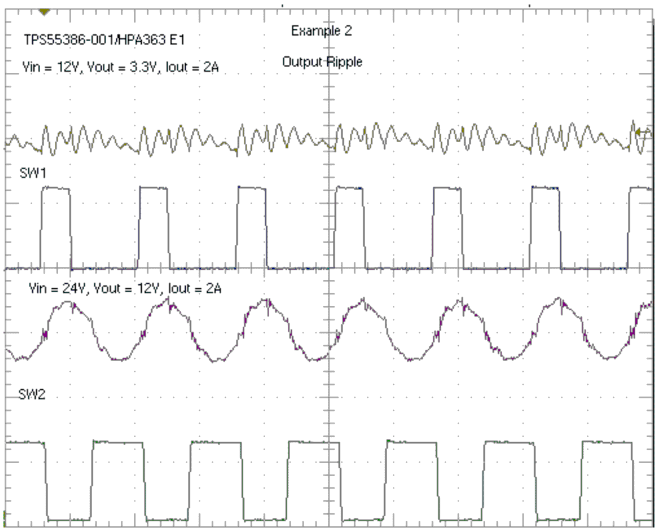


Figure 38. Design Example 2 Outputs and Switch Nodes

Example 3: Multiphase 12 V to 5.0 V at 6 A

The combination of current mode control and a transconductance amplifier allows the TPS55386 to serve as a single-output 2-phase supply. This configuration allows this part to serve as a 6-A non-synchronous converter at an effective 1.2 MHz. COMP2 is connected to COMP1 and FB2 is connected to BP. While not implemented in this example, EN2 could be used to disable Channel 2 at light load, improving efficiency.

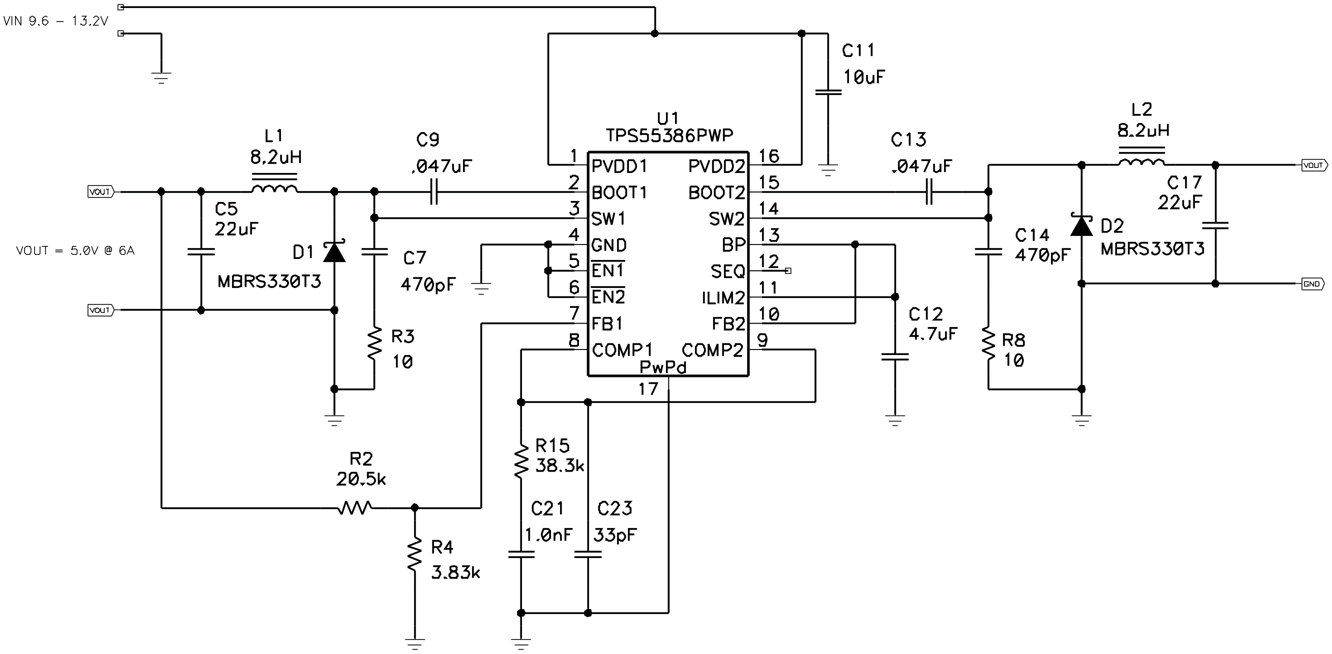


Figure 39. Design Example 3, TPS55386 as a Phase Non-Synchronous Buck Converter

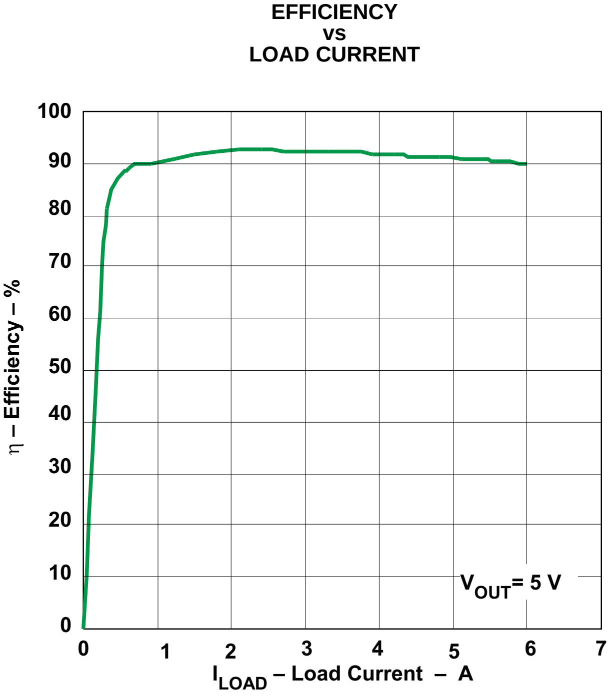


Figure 40.

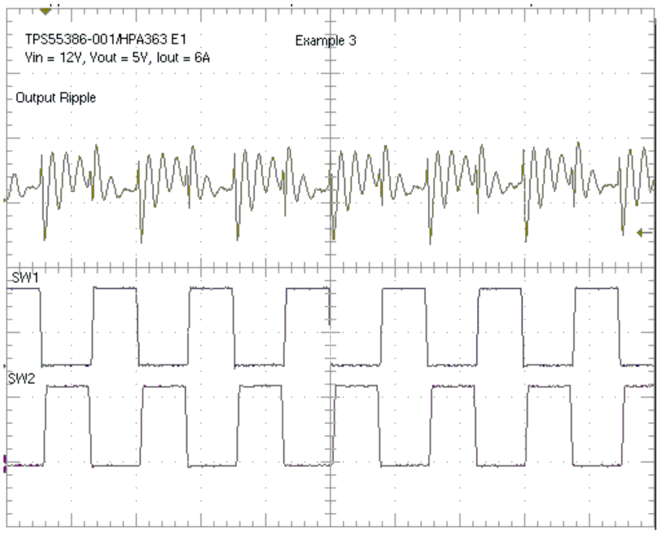


Figure 41. Design Example 3, Output and Switch Nodes

ADDITIONAL REFERENCES

Related Devices

The following devices have characteristics similar to the TPS55383/TPS55386 and may be of interest.

Table 4. Devices Related to the TPS55383 and TPS55386

TI LITERATURE NUMBER	DEVICE	DESCRIPTION
SLUS642	TPS40222	5-V Input, 1.6-A Non-Synchronous Buck Converter
SLUS749	TPS54283 / TPS54286	2-A Dual Non-Synchronous Converter with Integrated High-Side MOSFET
SLUS774	TPS54383 / TPS54386	3-A Dual Non-Synchronous Converter with Integrated High-Side MOSFET
SLVS839	TPS54331	3.5 V to 28 V, Single 3-A Non-Synchronous Buck Converter with Integrated High-Side MOSFET

References

These references, design tools and links to additional references, including design software, may be found at http:www.power.ti.com

Table 5. References

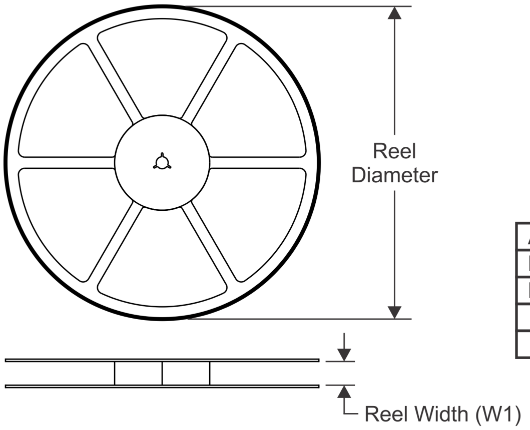
TI LITERATURE NUMBER	DESCRIPTION
SLMA002	PowerPAD Thermally Enhanced Package Application Report
SLMA004	PowerPAD™ Made Easy
SLUP206	Under The Hood Of Low Voltage DC/DC Converters. SEM1500 Topic 5, 2002 Seminar Series
SLVA057	Understanding Buck Power Stages in Switchmode Power Supplies
SLUP173	Designing Stable Control Loops. SEM 1400, 2001 Seminar Series

Package Outline and Recommended PCB Footprint

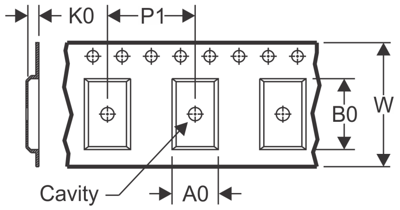
The following pages outline the mechanical dimensions of the 16-Pin PWP package and provide recommendations for PCB layout.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

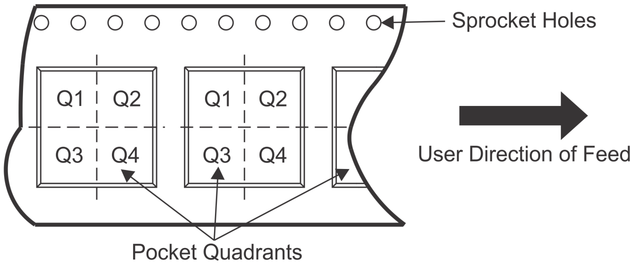


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

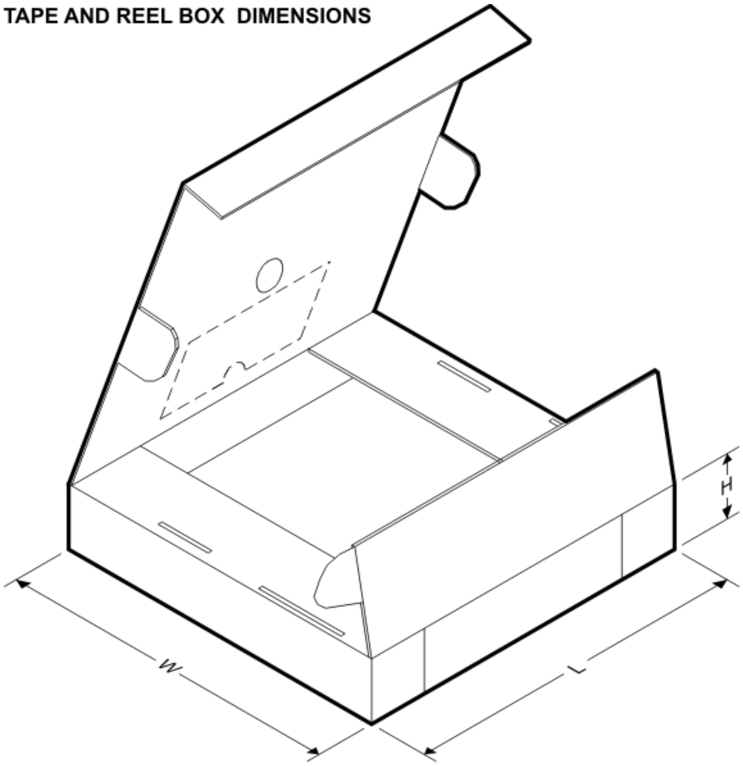
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55383PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS55386PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

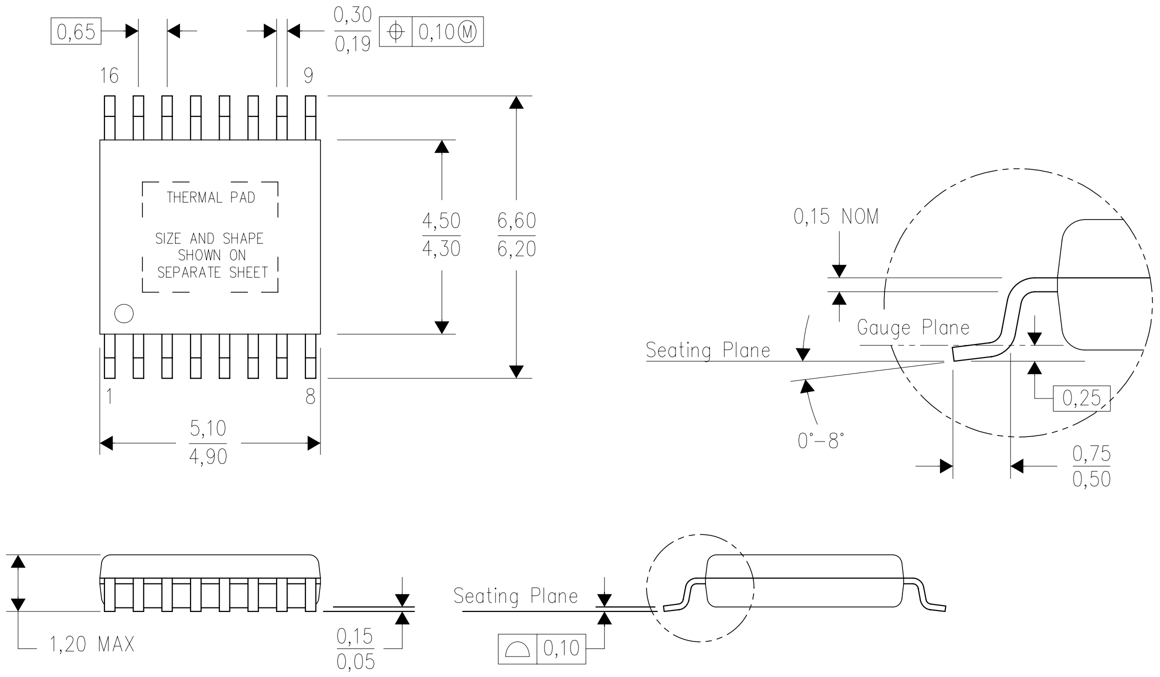
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55383PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
TPS55386PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

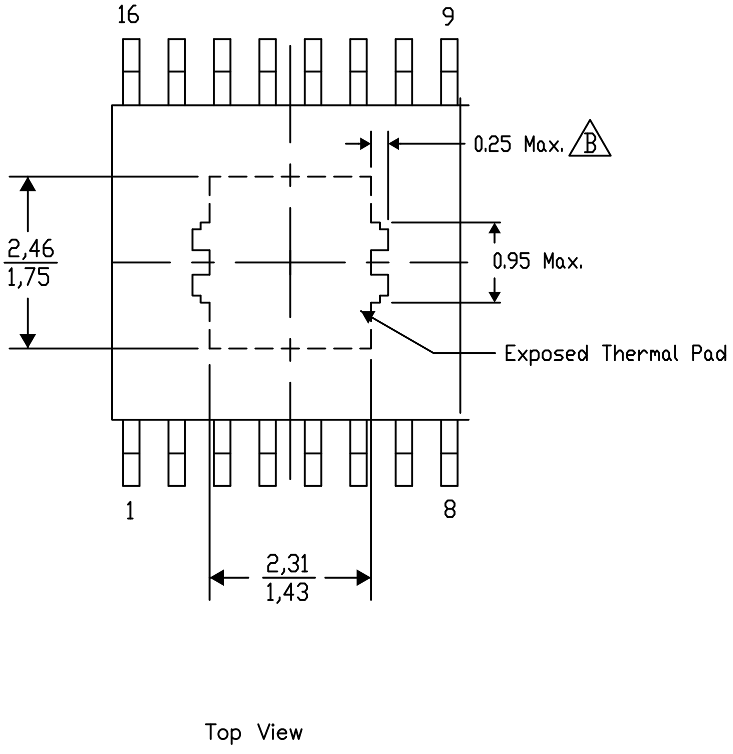
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

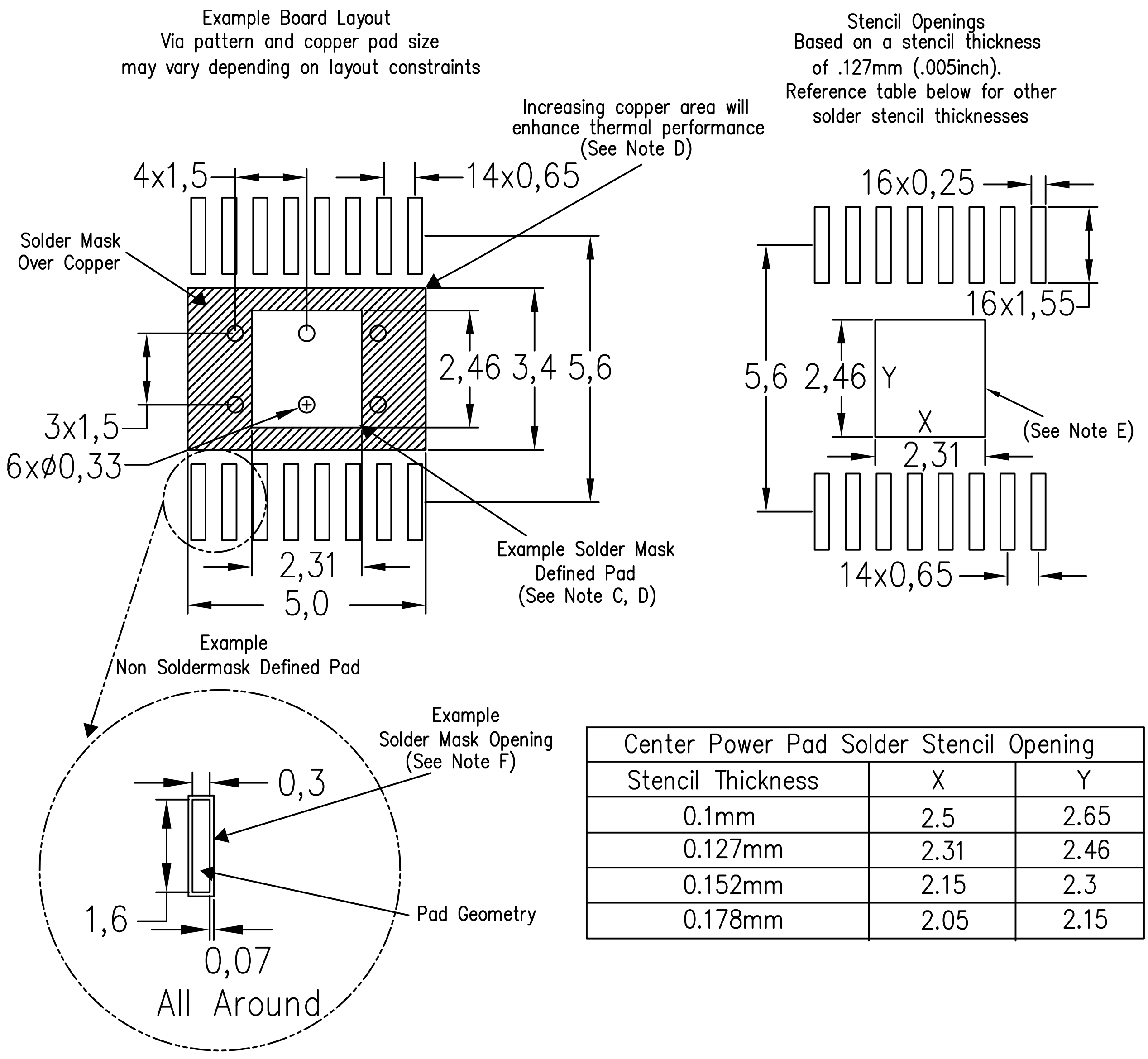
4206332–6/A0 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609-3/W 09/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

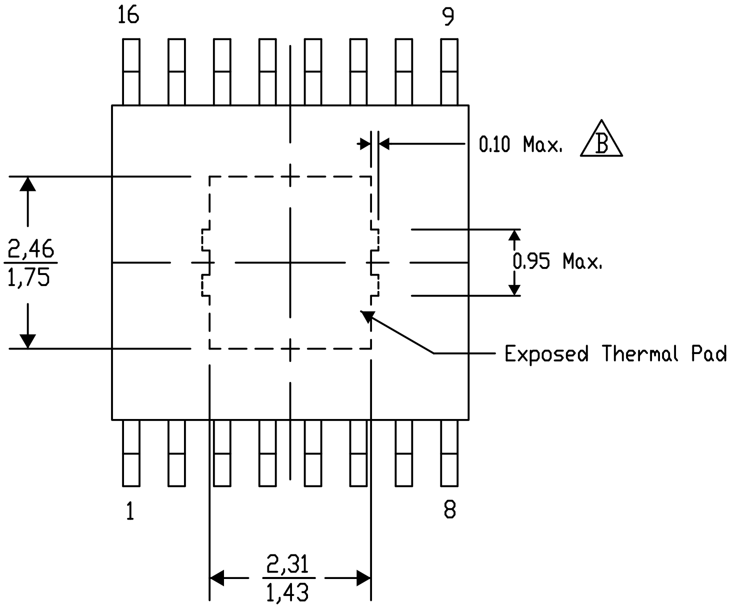
PWP (R–PDSO–G16)   PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–45/A0 01/16

NOTE: A. All linear dimensions are in millimeters
B. Exposed tie strap features may not be present.

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