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RoHS COMPLIANCE

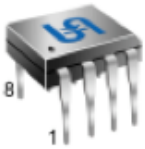
TS34119

Low Power Audio Amplifier

SOP-8



DIP-8



Pin assignment:

1. CD	8. VO2
2. FC2	7. Gnd
3. FC1	6. Vcc
4. Vin	5. VO1

General Description

The TS34119 is a low power audio amplifier, it integrated circuit intended (primarily) for telephone applications， such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0V minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80dB, and the closed loop gain is set with two external resistors. A chip Disable pin permits powering down and/or muting the input signal.

The TS34119 is offered in SOP-8 and DIP-8 package.

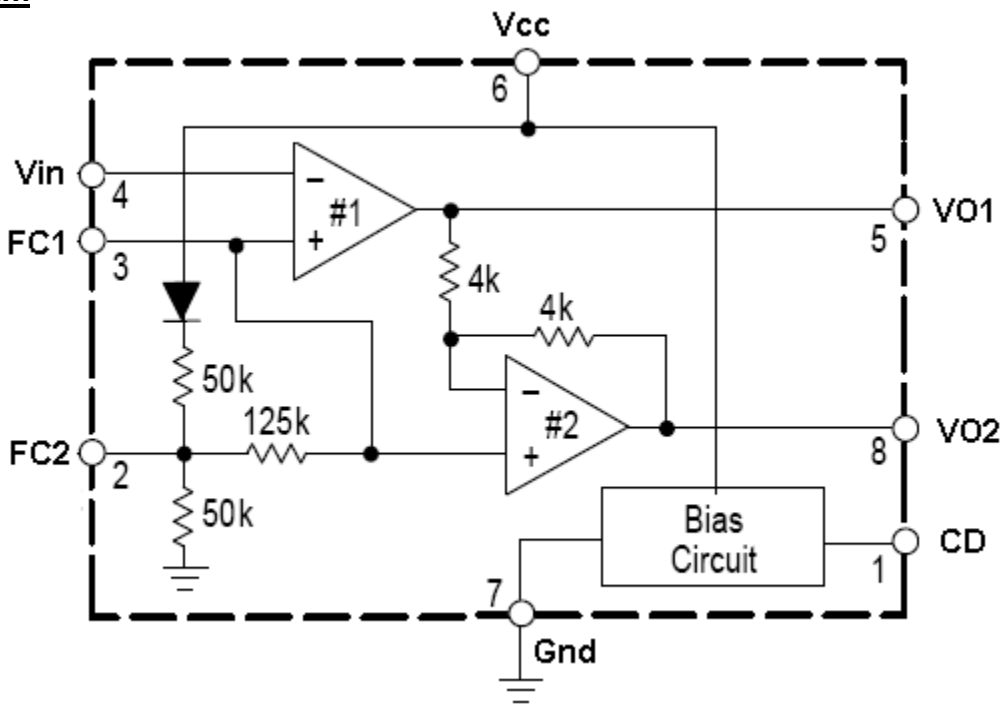
Features

- Wide operating supply voltage (2~16V)
- Chip disable input to power down the IC
- Low quiescent current for battery powered application
- Lower power down quiescent current
- Drives a wide range of speaker load (8~100Ω)
- Output power exceed 250mW with 32Ωspeaker
- Low total harmonic distortion
- Gain adjustable for voice band
- Requires few external components

Ordering Information

Part No.	Package	Packing
TS34119CD C3	DIP-8	50pcs / Tube
TS34119CS RL	SOP-8	2.5Kpcs / 13” Reel

Block Diagram



Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	+1 ~ 18V	V
Maximum Input Voltage (FC1, FC2, CD, Vin)	Vin	-1.0 ~ Vcc+1.0	V
Applied Output Voltage to VO1, VO2 when disabled	Vvo	-1.0 ~ Vcc+1.0	V
Maximum Output Current at VO1, VO2	Io	±250	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Maximum ratings are those values beyond which damage to the device may occur, functional operation should be Restricted to the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	+2 ~ 16V	V
Load Impedance	RL	8 ~ 100	Ω
Peak Load Current	IL	200	mA
Differential Gain (5kHz bandwidth)	AVD	0 ~ 46	dB
Voltage @ CD (pin 1)	VCD	0 ~ Vcc	V

Note: This device contains protection circuitry to guard against damage due to high static voltage or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltage to this high impedance circuit. For proper operation, Vin and Vout should be constrained to the range Gnd ≤ (Vin or Vout) ≤ Vcc. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Gnd or Vcc), unused output must be left open.

Electrical Specifications (VCD=0V, Ta =25°C; unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Amplifiers (AC Characteristics)						
AC Input Resistance	Ri	@ Vin	--	>30	--	MΩ
Open Loop Gain (Amp. #1)	AVOL1	f<100Hz	80	--	--	dB
Closed Loop Gain (Amp. #2)	AV2	Vcc=6V,f=1KHz, R_L=32Ω	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW		--	1.5	--	MHz
Output Power	Pout	Vcc=3V,R_L=16Ω,THD≤10%	55	--	--	mW
		Vcc=6V,R_L=32Ω,THD≤10%	250	--	--	
		Vcc=12V,R_L=100Ω,THD≤10%	400	--	--	
Total Harmonic Distortion (f=1KHz)	THD	Vcc=6V,R_L=32Ω, Po=125mW	--	0.5	1.0	%
		Vcc≥3V,R_L=8Ω, Po=20mW	--	0.5	--	
		Vcc≥12V, R_L=32Ω, Po=200mW	--	0.6	--	
Power Supply Rejection (Vcc=6.0V, ΔVcc=3.0V)	PSRR	C1=∞, C2=0.01uF	50	--	--	dB
		C1=0.1uF, C2=0, f=1KHz	--	12	--	
		C1=1uF, C2=5uF, f=1KHz	--	52	--	
Differential Muting	GMT	Vcc=6V, 1KHz ≤ f ≤ 20KHz, CD=2V	--	>70	--	dB

Electrical Specifications (Continue)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Amplifiers (DC Characteristics)						
Output DC Level @ VO1,VO2	Vo	V_{CC}=3V, RL=16 (R_f=75K)	1.0	1.15	1.25	Vdc
		Vcc=6V, RL=16 (R_f=75K)	--	2.65	--	
		Vcc=12V, RL=16 (R_f=75K)	--	5.56	--	
Output Level	V_{OH}	Iout=-75mA, 2.0 ≤ Vcc ≤ 16V	Vcc-1.0 (typ)			Vdc
	V_{OL}	Iout=75mA, 2.0 ≤ Vcc ≤ 16V	--	0.16	--	
Output DC Offset Voltage (VO1 – VO2)	ΔVo	Vcc=6V, RL=75KΩ, R_L=32Ω	-30	0	+30	mV
Input Bias Current @ Vin	f_{IB}	Vcc=6.0V	--	-100	-200	nA
Equivalent Resistance @ FC1	R_{FC1}	Vcc=6.0V	100	150	220	KΩ
Equivalent Resistance @ FC2	R_{FC2}		18	25	40	
Chip Disable (pin 1)						
Input Voltage Low	V_{IL}		--	--	0.8	Vdc
Input Voltage High	V_{IH}		2.0	--	--	
Power Supply						
Power Supply Current	Icc	Vcc=3V, R_L=∞, CD=0.8V	--	2.7	4.0	mA
		Vcc=16V, R_L=∞, CD=0.8V	--	3.3	5.0	
		Vcc=3V, R_L=∞, CD=2V	--	65	100	uA

Note: a. Currents into a pin are positive, currents out of a pin negative.

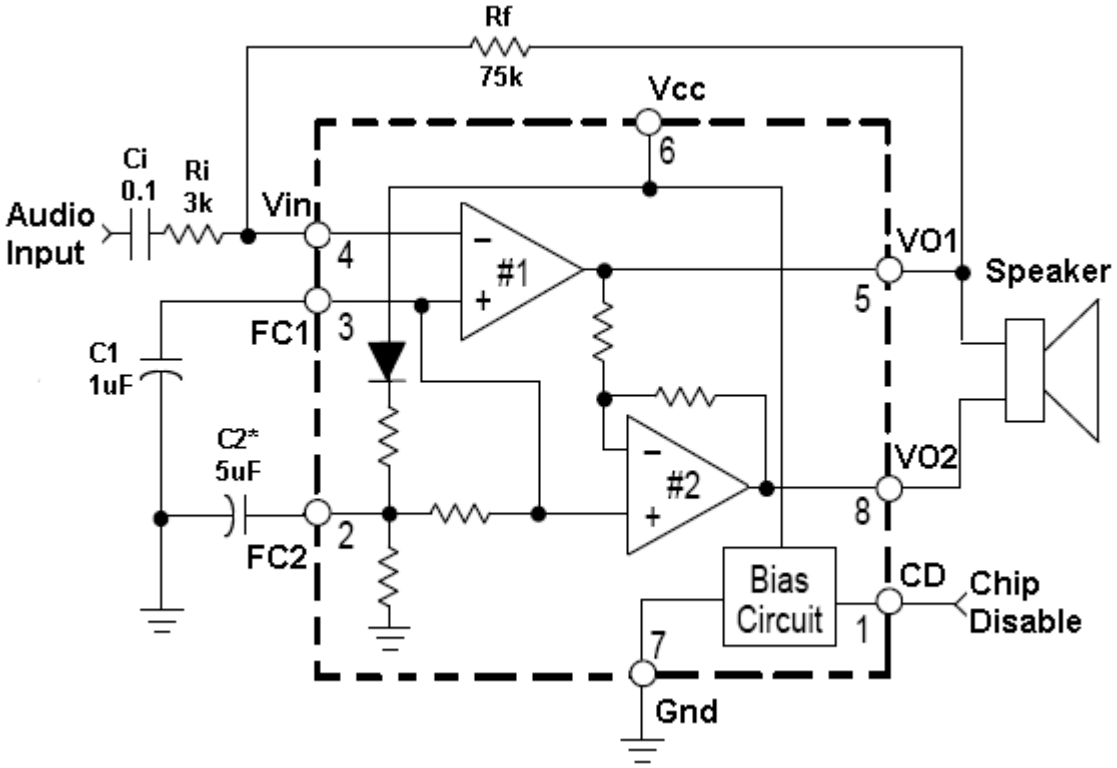
Typical Temperature Performance (-20°C < Ta < +70°C)

Function	Condition	Typical Change	Units
Input Bias Current	@ Vin	±40	Pa/°C
Total Harmonic Distortion	Vcc=6V, R_L=32Ω, Po=120mW, f=1kHz	+0.003	%/°C
Power Supply Current	Vcc=3V, R_L=∞, CD=0V	-2.5	uA/°C
	Vcc=3V, R_L=∞, CD=2V	-0.03	

Pin Function Description

Symbol	Pin	Description
CD	1	Chip Disable-Digital input. A logic "0" (<0.8V) sets normal operation. A logic "I"（≥2.0V）sets the power down mode. Input impedance is nominally 90KΩ
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open it the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1uF capacitor at this pin (with a 5uF capacitor at pin 2) provides 52dB(typically) of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
Vin	4	Amplifier input. The input capacitor and resistor set low frequency roll off and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC} - 0.7) / 2
V_{CC}	6	DC supply voltage (+2.0V ~ +16V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out-of-phase with that at VO1. The dc level is ≈ (V_{CC} - 0.7V) / 2.

Typical Application Circuit



* Optional
Differential Gain = 2 x (Rf / Ri)

Design Guideline

GENERAL

The TS34119 is a low power audio amplifier capable of low voltage operation (Vcc=2.0V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1-VO2) to the speaker to maximize the available voltage swing at low voltages. The different gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80Db (at f≤100Hz), and the closed loop gain is set by external resistor Rf and Rj. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5MHz. In order to adequately cover the telephone voice band (300Hz to 3.4kHz), a maximum closed loop gain of 46dB is recommended. Amplifier #2 is internally set to gain of –1.0 (0dB). The outputs of both amplifiers are capable of souring and sinking a peak current of 200mA.The outputs can typically swing to within ≈ 0.4V above ground, and to within≈1.3V below VCC, at the maximum current. See Figure 18 and 19 for VOH and VOL curves. The output dc offset voltage (VO1-VO2) is primarily a function of the feedback resistor (Rf), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of Vin (pin 4) and through Rf, forcing VO1 to shift negative by an amount equal to (Rf × IIB), Vo2 is shifted posited an equal amount. The output offset voltage, specified in the Electrical Characteristics is measured with the feedback the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as wells internal offset voltages of the amplifiers. The bias current is constant with respect to VCC.

FC1 AND FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figure 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as RFC1 and RFC2). In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50K and 125K resistors. The graph of Figure 1 indicates the turn-on time upon application of VCC of +6V. The turn-on time is ≈ 60% longer for VCC =3V, and ≈ 20% less for VCC =9V. Turn-off time is <10uS upon removal of VCC.

CHIP DISABLE

The chip Disable (pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0V to 0.8V), the TS34119 is enabled for normal operation. When pin 1 is a Logic "1" (2V to VCC), the IC is disabled. If pin 1 is open, that is equivalent to Logic "0" although good design proactive dictates that an input should never be left open. Input impedance at pin 1 is a nominal 90KΩ. The power supply current (when disabled) is shown in Figure 15. Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70dB. The turn-off time the audio output, from the application of the CD signal, is <2uS, and turn on-time is 12 mS-15mS. Both times are independent of C1, C2, and VCC. When the TS34119 is disabled, the voltage at FC1 and FC2 do not change as they are powered from Vcc. The outputs, VO1 and VO2, change to high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of VCC and Ground.

LAYOUT CONSIDERATIONS

Normally a snobbier is not needed at the output of the TS34119, unlike many other audio amplifiers, However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

Design Guideline

POWER DISSIPATION

Figure 8 to 10 indicate the device dissipation (within the IC) for various combinations of VCC, RL, and load power. The maximum power which can safely be dissipated within the TS34119 is found from the following equation:

PD= (140oC - Ta) / Θja

Where Ta is the ambient temperature; and Θja is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.) The power dissipated within the TS34119, in a given application, it is found from the following equation: PD= (VCC × ICC) + (IRMS × VCC) - (RL × IRMS2)

Where ICC is obtained from Figure 15; and IRMS is the RMS current at the load; and RL is load resistance. Figure 8 to 10, along with Figure 11 to 13 (distortion curves), and a peak working load current of ±200mA, define the operating range for the TS34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8Ω, 16Ω and 32Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the TS34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long-term reliability.

Electrical Characteristics Curve

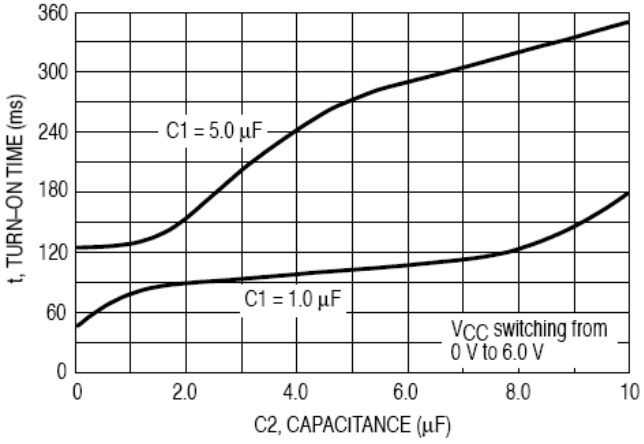


Figure 1. Turn-On Time vs. C2, C2 at Power-On

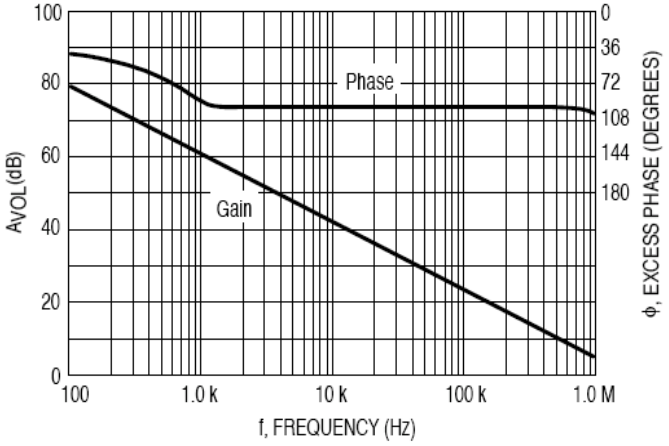


Figure 2. Amplifier #1 Open Loop Gain and Phase

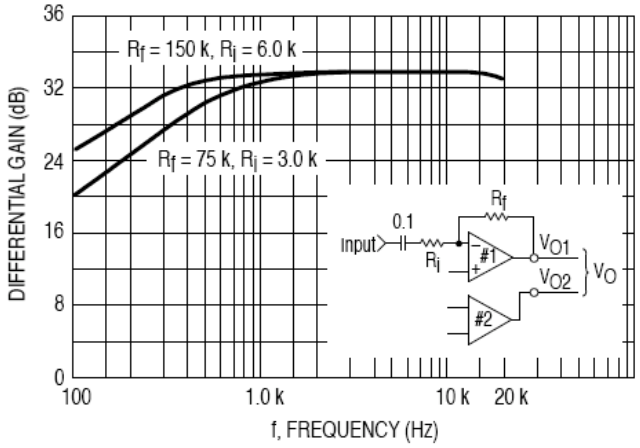


Figure 3. Differential Gain vs. Frequency

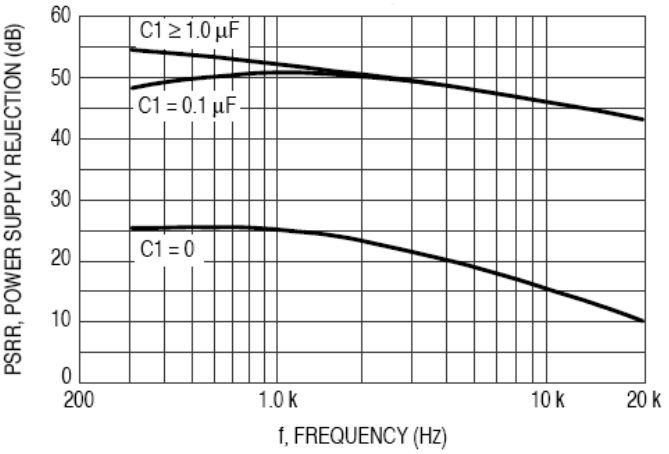


Figure 4. PSRR vs. Frequency (C2=10uF)

Electrical Characteristics Curve (Continue)

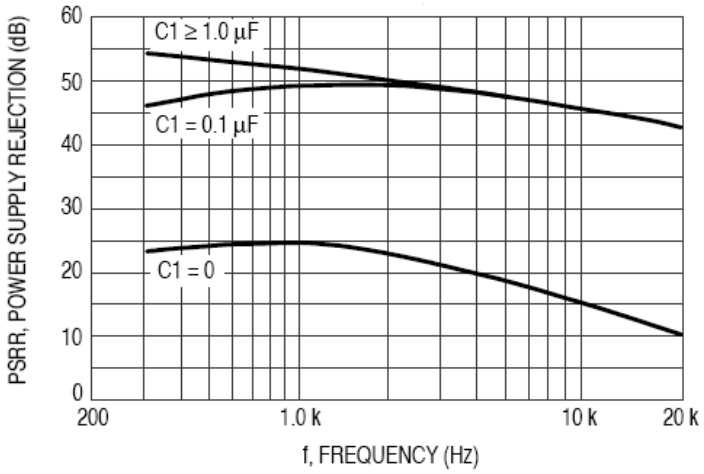


Figure 5. PSRR vs. Frequency (C2=5uF)

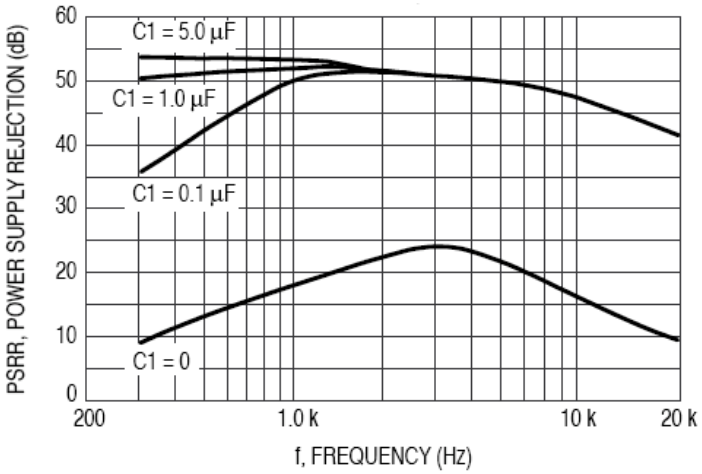


Figure 6. PSRR vs. Frequency (C2=1uF)

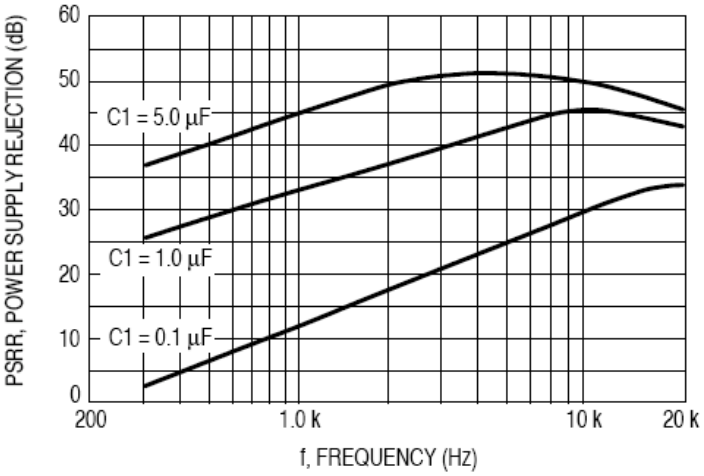


Figure 7. PSRR vs. Frequency (C2=0uF)

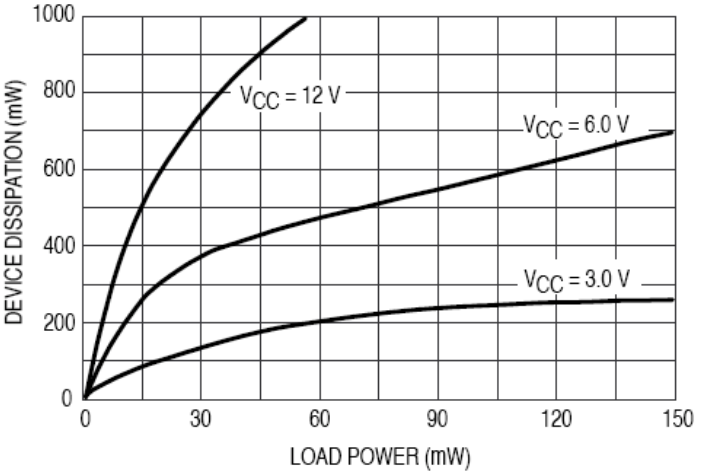


Figure 8. Device Dissipation, 0.8Ω Load

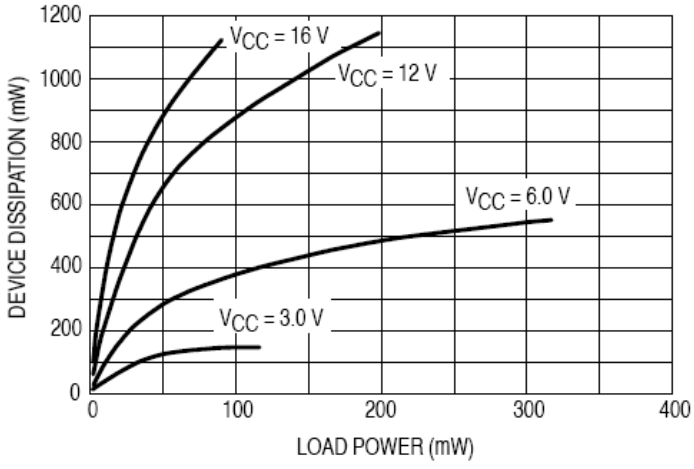


Figure 9. Device Dissipation, 16Ω Load

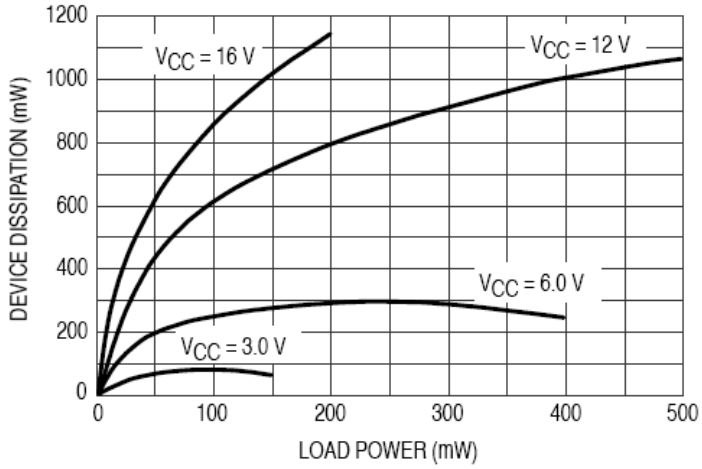


Figure 10. Device Dissipation, 32Ω Load

Electrical Characteristics Curve (Continue)

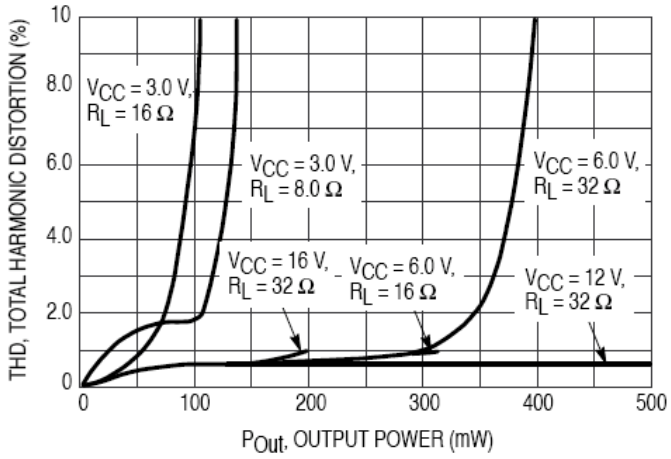


Figure 11. Distortion vs. Power (f=1kHz, AVD=34dB)

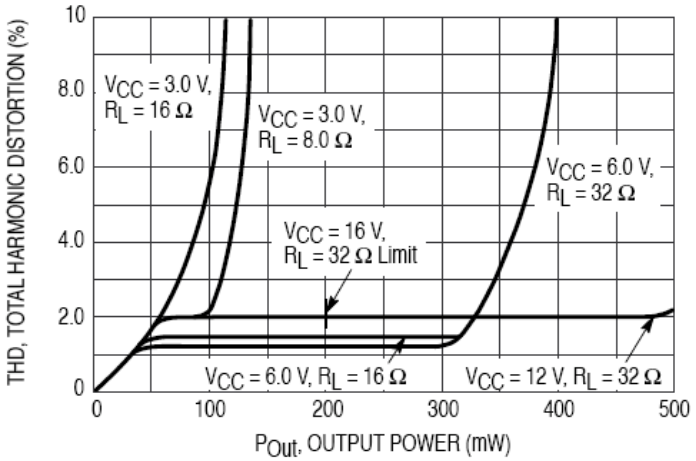


Figure 12. Distortion vs. Power (f=3kHz, AVD=34dB)

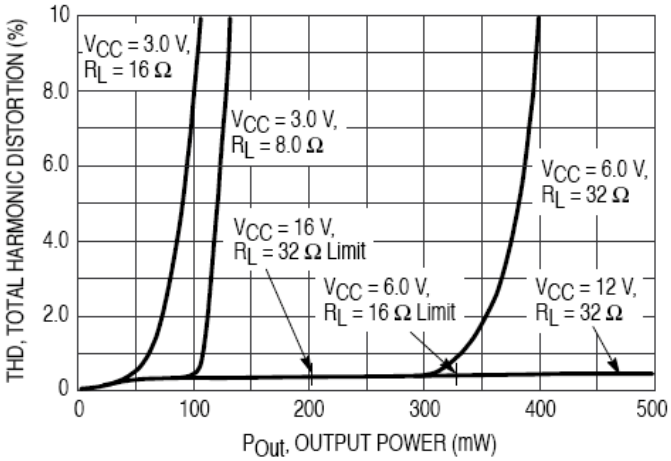


Figure 13. Distortion vs. Power (f=1, 3kHz, AVD=12dB)

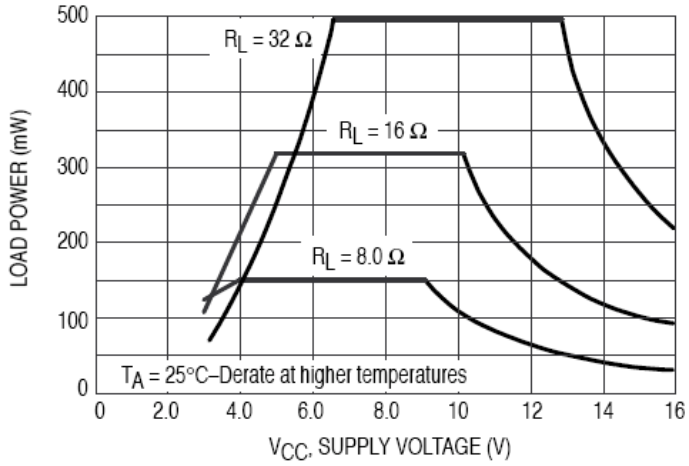


Figure 14. Maximum Allowable Load Power

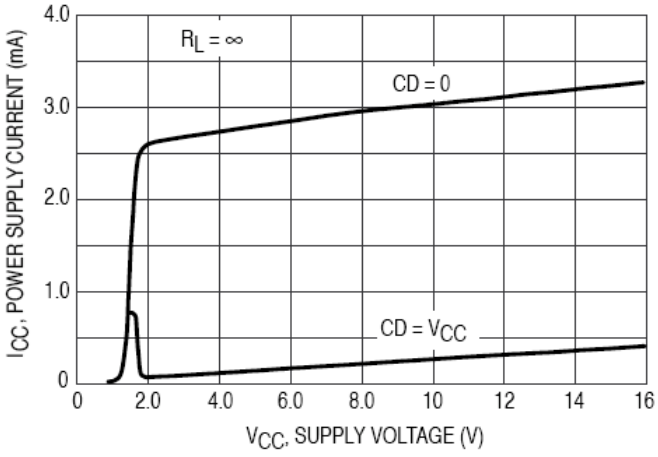


Figure 15. Power Supply Current

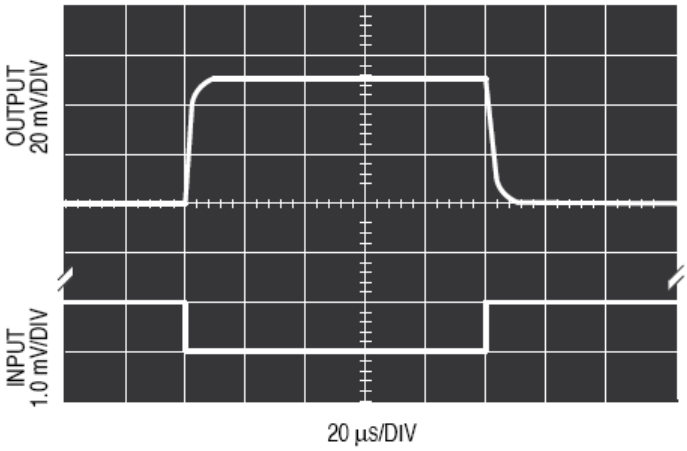


Figure 16. Small Signal Response

Electrical Characteristics Curve (Continue)

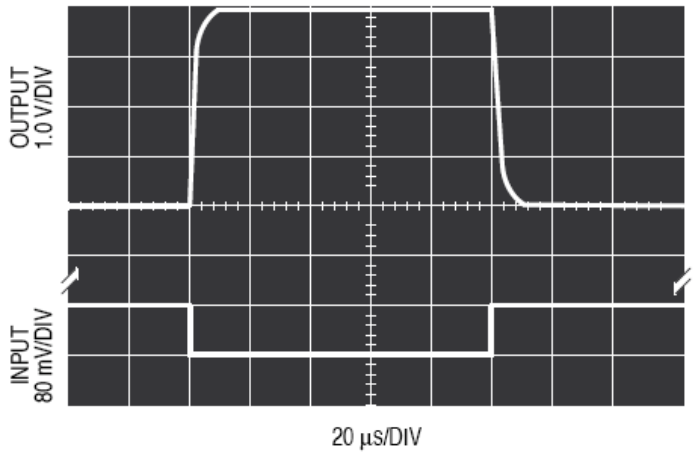


Figure 17. Large Signal Response

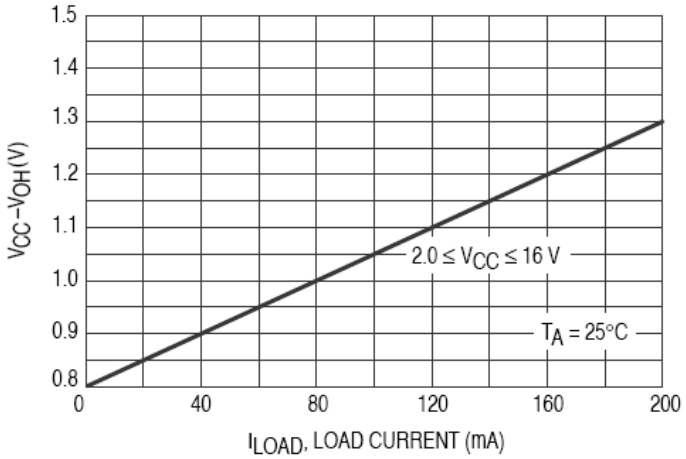


Figure 18. Vcc-Voh @ Vo1, Vo2 vs. Load Current

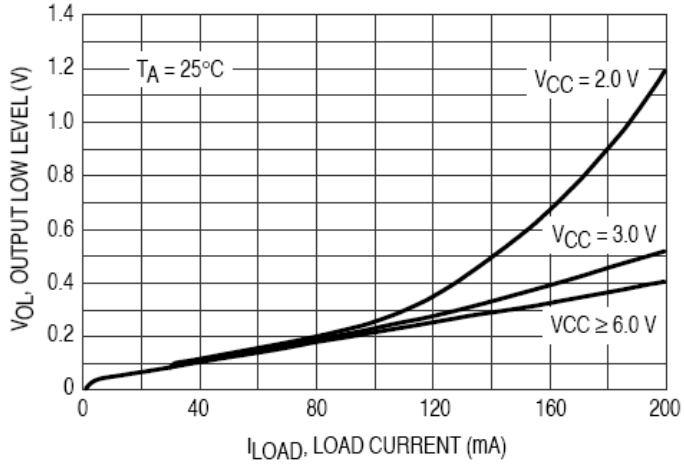


Figure 19. Vol @ Vo1, Vo2 vs. Load Current

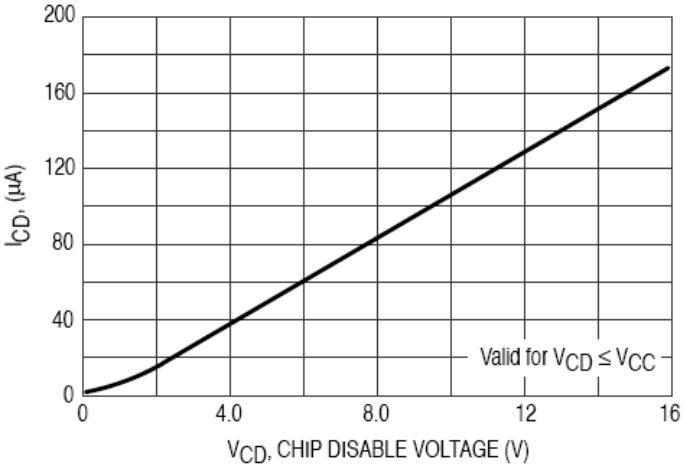


Figure 20. Input Characteristics @ CD (Pin1)

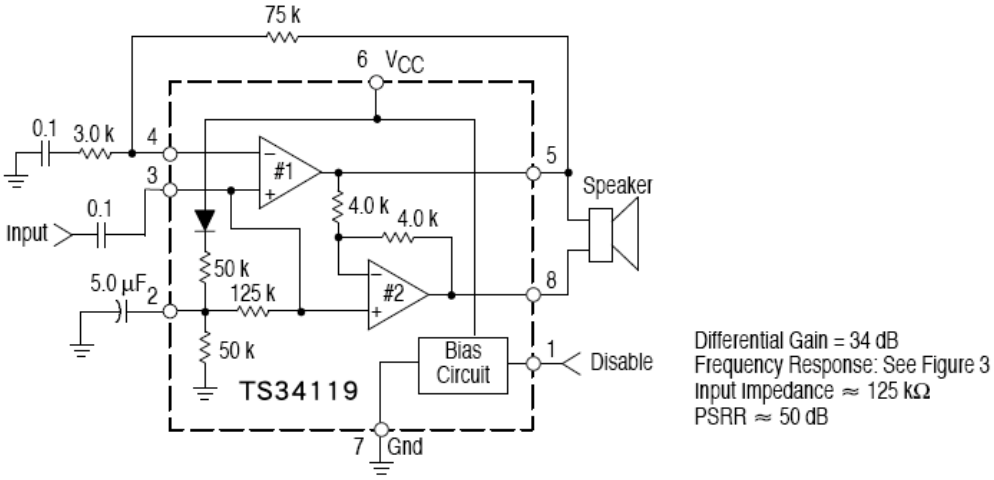


Figure 21. Audio Amplifier with High Input Impedance

Electrical Characteristics Curve (Continue)

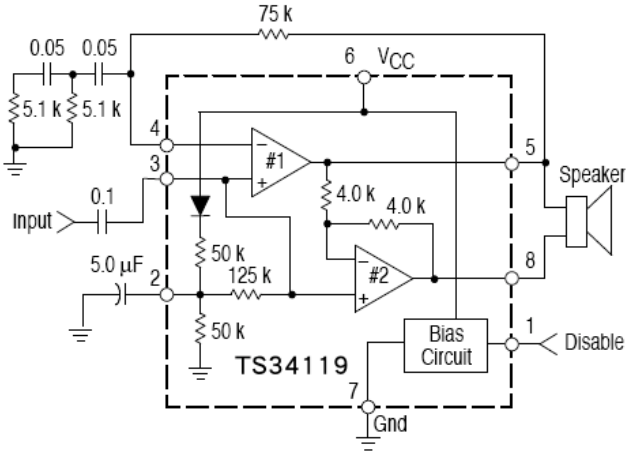


Figure 22. Audio Amplifier with Bass Suppression

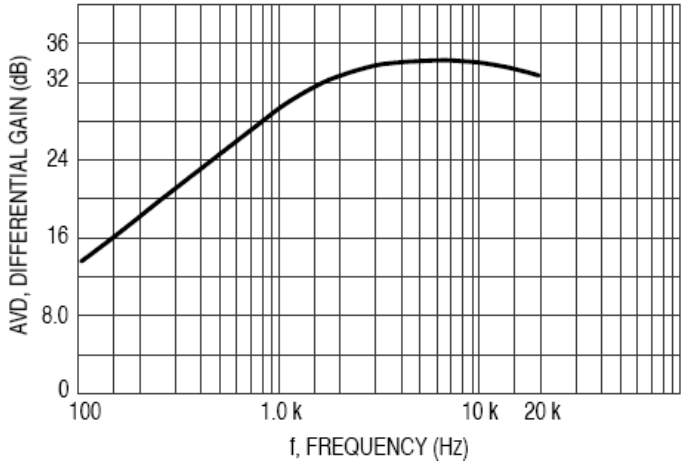


Figure 23. Frequency Response of Figure 22

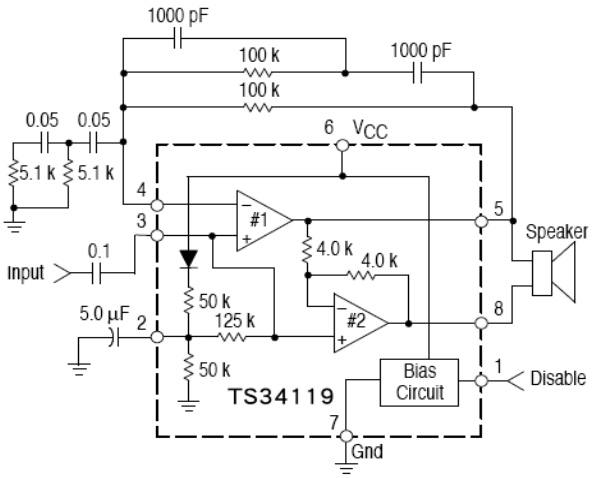


Figure 24. Audio Amplifier with Bandpass

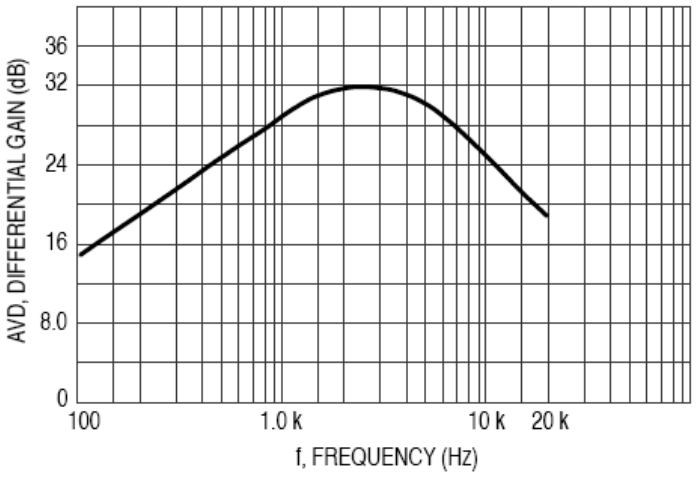
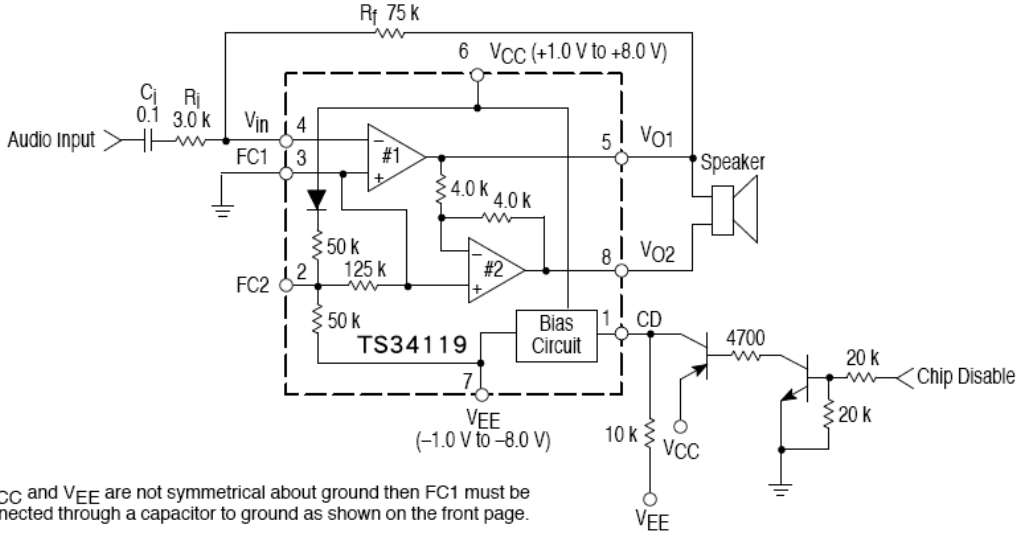


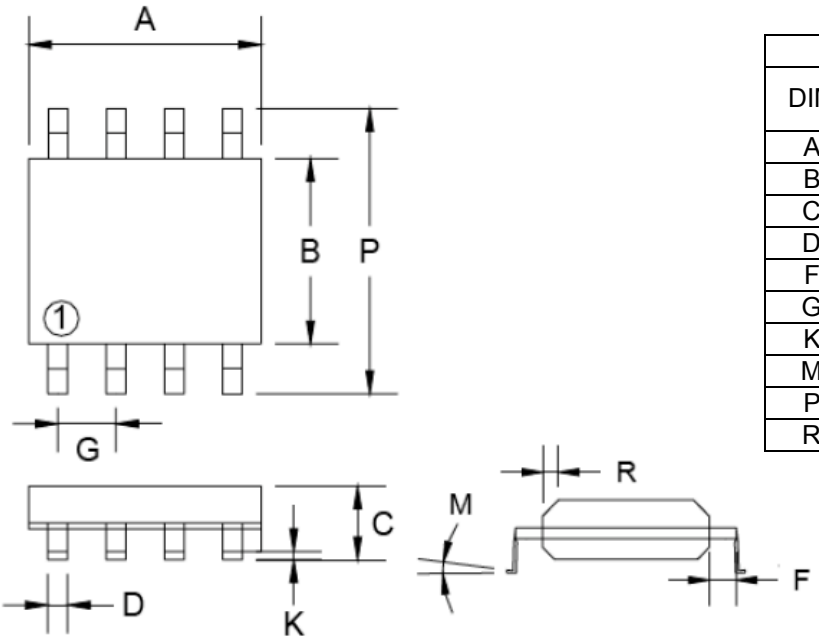
Figure 25. Frequency Response of Figure 24



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

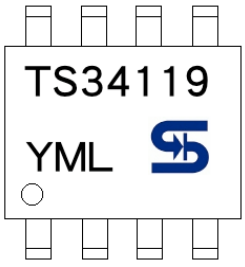
Figure 9. Device Dissipation, 16Ω Load

SOP-8 Mechanical Drawing



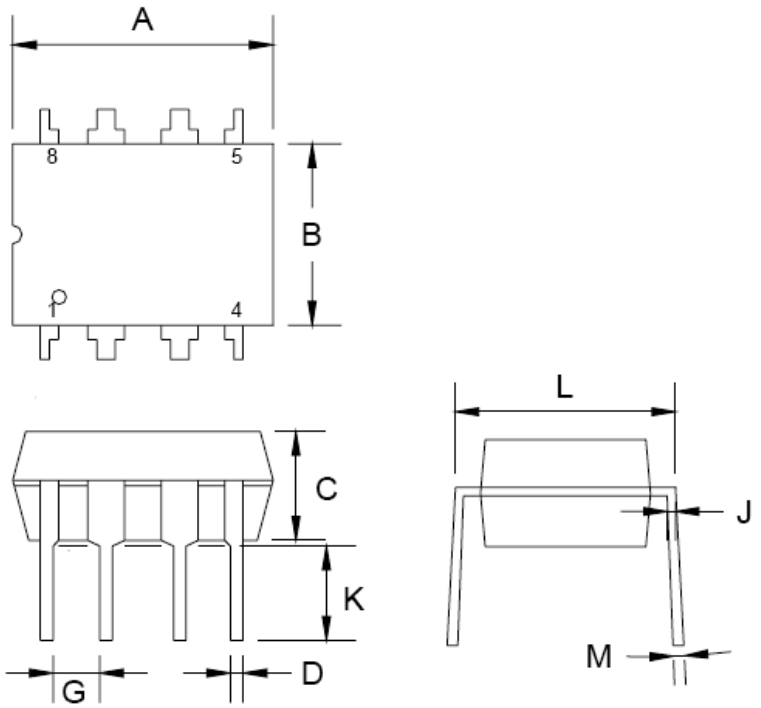
SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Marking Diagram



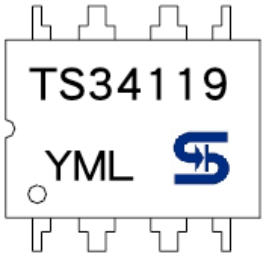
Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

DIP-8 Mechanical Drawing



DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10^{o}	-	10^{o}

Marking Diagram



Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

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