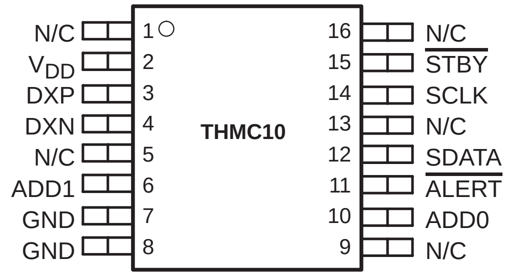
- **Two-Wire SMBus Serial Interface**
- **On-Chip and External Diode-Connected Transistor Temperature Monitoring**
  - **±2.5°C Accuracy for On-Die**
  - **±3°C Accuracy for External**
- **Programmable Under/Overtemperature Limits**
- **Under/Overtemperature Interrupt Signal to Host Controller**
- **Low Operating Current . . . 35 µA (Average)**
- **Low Standby Current . . . 3 µA**
- **3-V to 3.6-V Supply Voltage Range**

SSOP DBQ Package
(TOP VIEW)



description

The THMC10 is a dual digital temperature monitor with under/overtemperature alerts intended for use in personal computer systems or any other system requiring local as well as remote temperature monitoring and management (e.g., servers and workstations). The device may be used in smart battery applications and memory modules. The device is designed to measure the temperature on a microprocessor using a diode-connected transistor on the microprocessor die, such as the one present on the Intel® Pentium® II, III, and the Sun® UltraSPARC™. The device may also be used with a low-cost, diode-connected, discrete transistor, such as a 2N3904 or 2N3906, for remote temperature sensing applications.

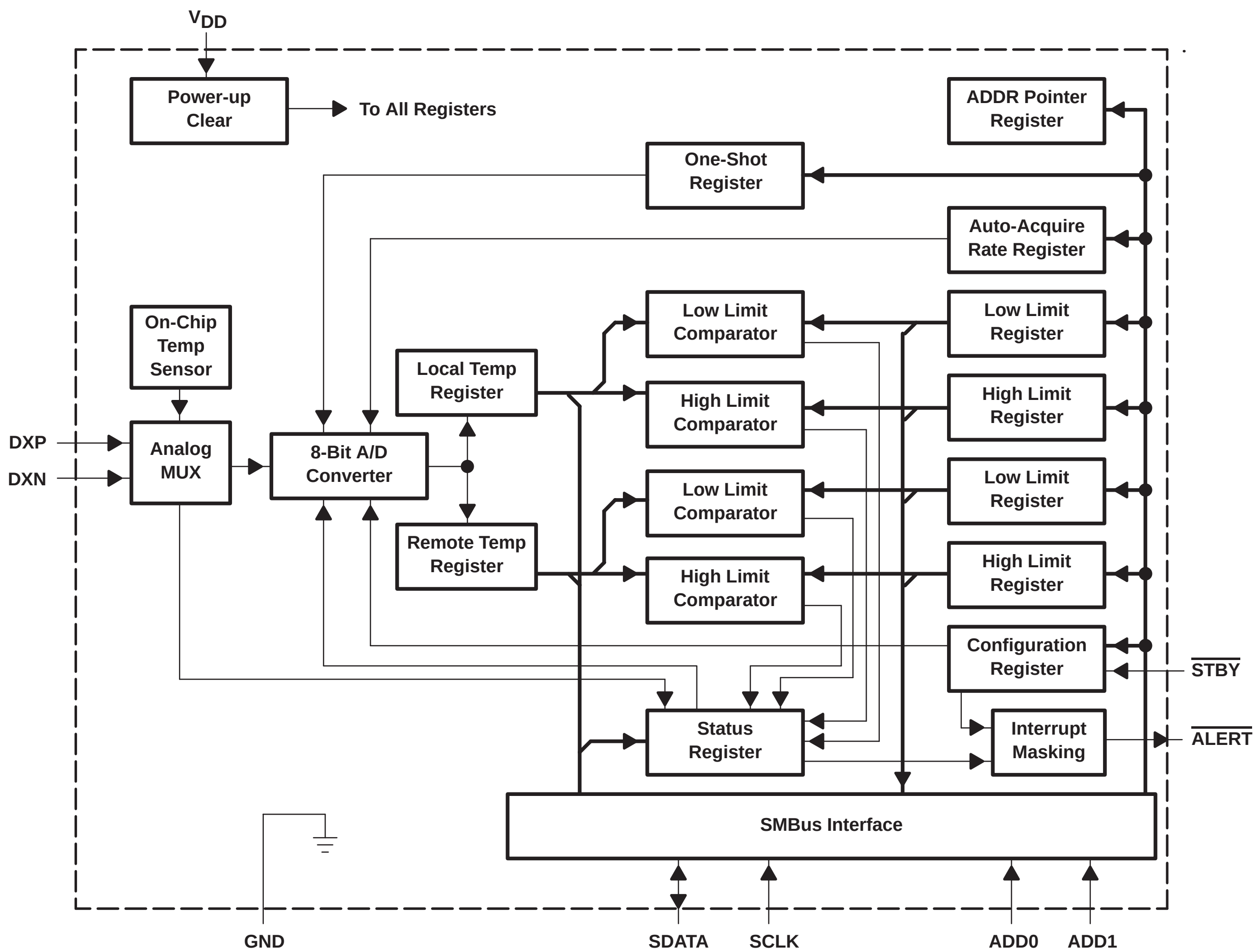
The THMC10 uses a two-current measurement technique on a single diode-connected transistor that cancels the absolute value of the remote transistor’s V_{BE}; therefore, no calibration is needed. The second channel measures an on-chip temperature sensor which can be used to monitor the ambient temperature in the THMC10’s operating environment.

The THMC10 uses a two-wire, SMBus interface to report temperature in an 8-bit, 2s complement format in °C. Under/overtemperature limits for both the on-chip and remote temperature sensors are user programmable via the SMBus interface. The $\overline{\text{ALERT}}$ terminal can be used as an interrupt or SMBus alert function to indicate under/overtemperature. The $\overline{\text{STBY}}$ terminal and the *start/stop* bit in the SMBus interface allow the device to enter a low current standby mode (typically <10 µA).

The THMC10 also provides diagnostics via the $\overline{\text{ALERT}}$ terminal and the SMBus interface for an open remote sensor connection or if the sensor connection is shorted to V_{DD}.

Intel and Pentium are registered trademarks of Intel Corporation.
Sun is a registered trademark and UltraSPARC is a trademark of Sun Microsystems.

schematic/block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADD0	10	I	SMBus address select terminal 0 (Note: Excess capacitance on this terminal may cause SMBus address recognition problems.)
ADD1	6	I	SMBus address select terminal 1 (Note: Excess capacitance on this terminal may cause SMBus address recognition problems.)
$\overline{\text{ALERT}}$	11	O	Active low temperature interrupt signal
DXN	4	I/O	Current sink for external diode connected transistor and A/D negative input (Do not leave floating if no external diode is used − should be tied to GND.)
DXP	3	I/O	Current source for external diode connected transistor and A/D positive input
GND	7, 8	I	IC ground
N/C	1, 5, 9, 13, 16	N/C	No connection
SCLK	14	I	SMBus serial clock input terminal − clock signal for SMBus serial data
SDATA	12	I/O	SMBus serial data I/O terminal − serial data I/O for SMBus
$\overline{\text{STBY}}$	15	I	Active low standby mode input
V_{DD}	2	I	IC supply voltage − should be decoupled with external 0.1 µF capacitor

absolute maximum ratings over operating case temperature (see Note 1) (unless otherwise noted)†

Input voltage on: V_{DD} supply terminal, $V_{(DDIN)}$ . . . −0.3 V to 6 V
I/O terminals, $V_{(IOIN)}$ . . . −0.3 V to V_{DD} + 0.3 V
SMBus terminals, $V_{(SMBIN)}$ . . . −0.3 V to 6 V
DXN terminal, $V_{(DXN)}$ . . . −0.3 V to 0.8 V
SMBus input/output current, $I_{(SMBIN)}$ . . . −1 mA to 50 mA
DXN input current, $I_{(DXN)}$ . . . −1 mA to 1 mA
Continuous power dissipation, P_D . . . 330 mW
Operating case temperature range, T_C . . . −55°C to 125°C
Storage temperature, T_{stg} . . . −65°C to 165°C
Junction temperature, T_J . . . 150°C
Lead temperature (soldering, 10 sec), $T_{(LEAD)}$ . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	MAX	UNITS
Supply voltage, V_{DD}	3	3.6	V
SMBus input high voltage, V_{IH}	2.2		V
SMBus input low voltage, V_{IL}		0.8	V
SMBus operating frequency, $f_{(SCLK)}$	10	100	kHz
Operating ambient temperature, T_A	0	85	°C

dc electrical characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

A/D and supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{(RES)}$	Temperature resolution	No missed codes	1			°C
$T_{(ERR1)}$	Initial temperature error from internal diode	T_A = 60°C to 100°C	−2		2	°C
		T_A = full range	−3		3	
$T_{(ERR2)}$	Initial temperature error from external diode (see Note 2)	T_A = 60°C to 100°C	−2.5		2.5	°C
		T_A = full range	−3.5		3.5	
$V_{(UVLOCK)}$	Under voltage lockout voltage	V_{DD} input, disables acquisition, rising edge	2.65	2.8	2.95	V
$V_{(POR)}$	Power-up reset threshold	On V_{DD} input, falling edge	1	2.25	2.5	V
$I_{(DD,STANDBY)}$	V_{DD} standby supply current	Logic inputs forced to V_{DD} or GND, $\overline{STBY}$ mode, SMBus is static		3	10	µA
		Logic inputs forced to V_{DD} or GND, $\overline{STBY}$ mode, SCLK = 10 kHz		4		µA
I_{DD}	V_{DD} operating supply current (averaged over 4 seconds in auto-acquire mode)	Slow auto-aquire rate (0.25 samples/sec)		40	70	µA
		Fast auto-aquire rate (2 samples/sec)		45	180	
$V_{(D,SOURCE)}$	DXN source voltage			0.7		V
$I_{(DLEAK)}$	DXP and DXN leakage current	$\overline{STBY}$ = 0, DXP = DXN = 0			2	µA
$I_{(ADD,BIAS)}$	Add {0:1} bias current	Momentary on power up		35	100	µA
$I_{(DIODE)}$	Diode source current	DXP = 1.5 V, high level		100		µA
		DXP = 1.5 V, low level		10		
$I_{(RATIO)}$	Diode source current ratio	$DXP = 1.5\text{ V}, \frac{\text{high level}}{\text{low level}}$	9.7	10	10.2	

NOTE 2: Based on $T(°C) = \frac{q\left(\Delta V_{BE}\right)}{n\,k\,[\ln(10)]} - 273$

Where

$q = 1.6 \times 10^{-19}$ (charge)
$n = 1.0085$ (diode ideality factor)
$k = 1.38 \times 10^{-23}$ (Boltzman's constant)

SMBus

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input high voltage		2.2			V
V_{IL}	Input low voltage				0.8	V
I_{OL1}	SMBus output low current	SDATA = 0.6 V	6			mA
I_{OL2}	$\overline{ALERT}$ output low current	$\overline{ALERT}$ = 0.4 V	1			mA
I_I	SMBus input current		−1		1	µA

ac electrical characteristics, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

A/D and supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{(CONV)}$	One-shot conversion time	One-shot mode from SMBus stop bit to temperature conversion completed (both channels)		12		ms
	Acquisition rate accuracy	Auto-aquire mode	−25%		25%	

SMBus

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$f_{(SCLK)}$	SCLK operating frequency	See Figure 1	10		100	kHz
$t_{(BUF)}$	Bus free time between stop and start condition	See Figure 1	4.7			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated	See Figure 1	4			µs
$t_{(SUSTA)}$	Repeated start condition setup time	See Figure 1	4.7			µs
$t_{(SUSTO)}$	Stop condition setup time	See Figure 1	4			µs
$t_{(HDDAT)}$	Data hold time	See Figure 1	300			ns
$t_{(SUDAT)}$	Data setup time	See Figure 1	250			ns
$t_{(LOW)}$	SCLK clock low period	See Figure 1	4.7			µs
$t_{(HIGH)}$	SCLK clock high period	See Figure 1	4		50	µs
$t_{(LOWSEXT)}$	Cumulative clock low extend time (slave device)	See Figure 1			25	ms
$t_{(LOWMEXT)}$	Cumulative clock low extend time (master device)	See Figure 1			10	ms
t_F	Clock/data fall time	See Figure 1			300	ns
t_R	Clock/data rise time	See Figure 1			1000	ns

PARAMETER MEASUREMENT INFORMATION

SMBus timing diagrams

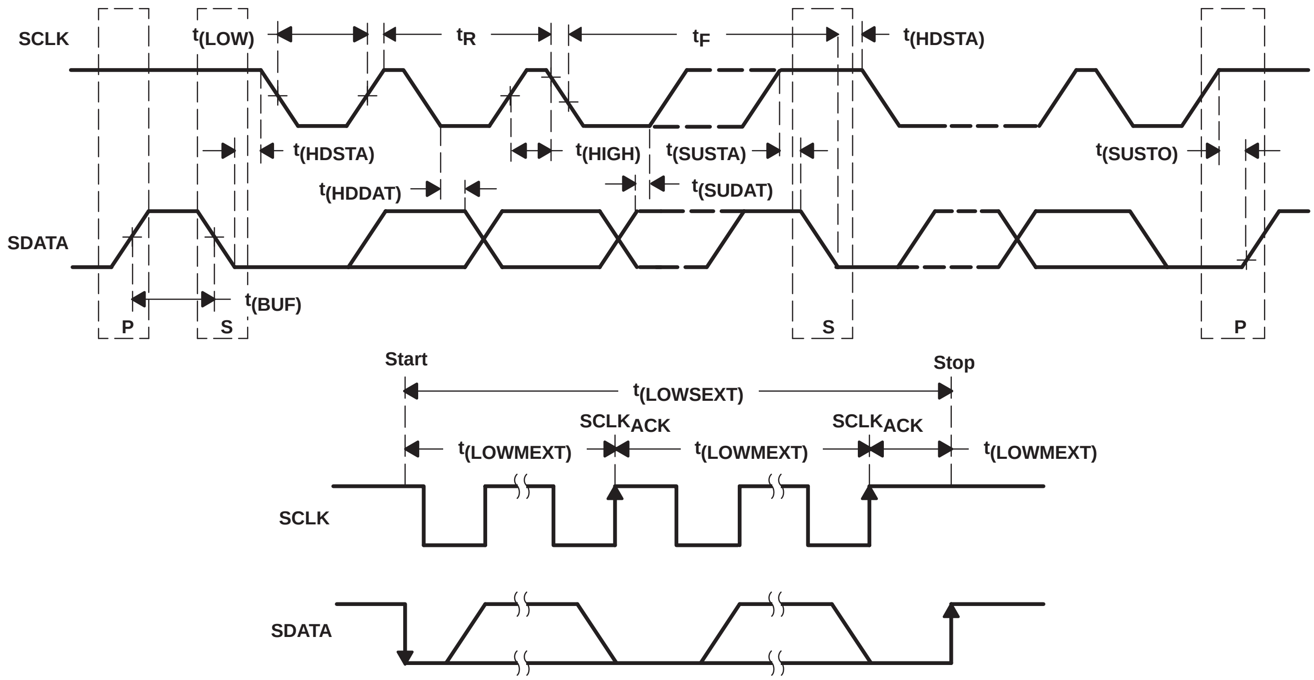


Figure 1. SMBus Timing Diagram

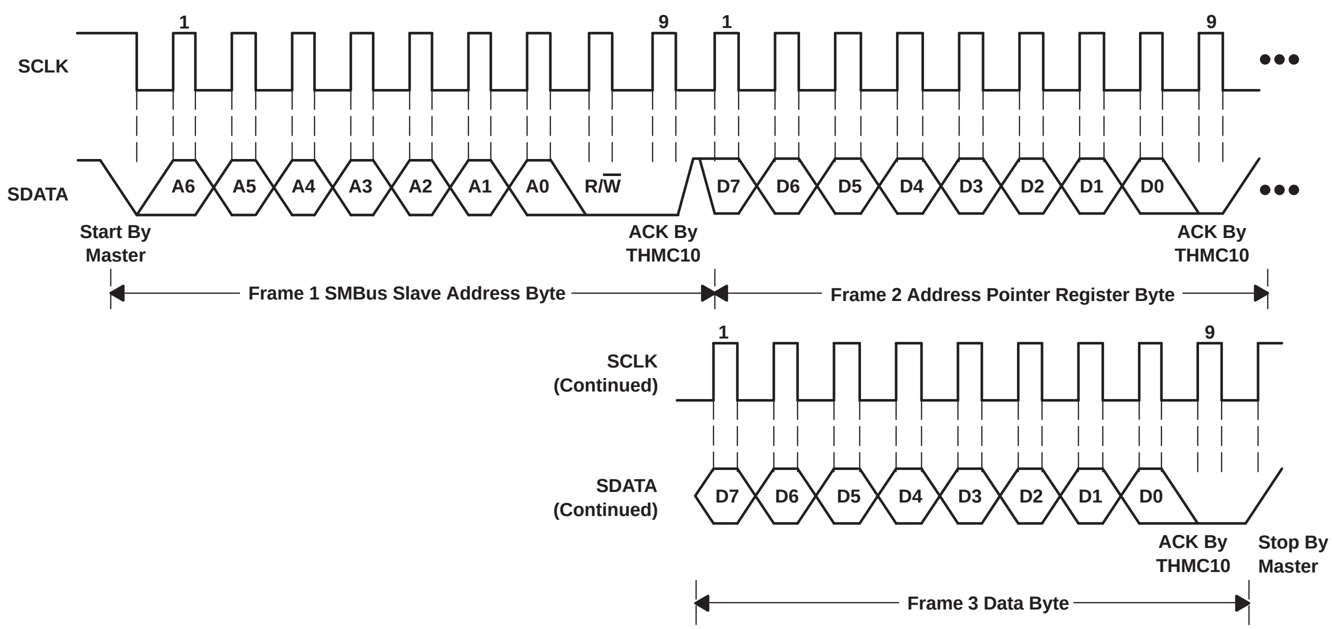


Figure 2. SMBus Timing Diagram for Write Byte Format

PARAMETER MEASUREMENT INFORMATION

SMBus timing diagrams (continued)

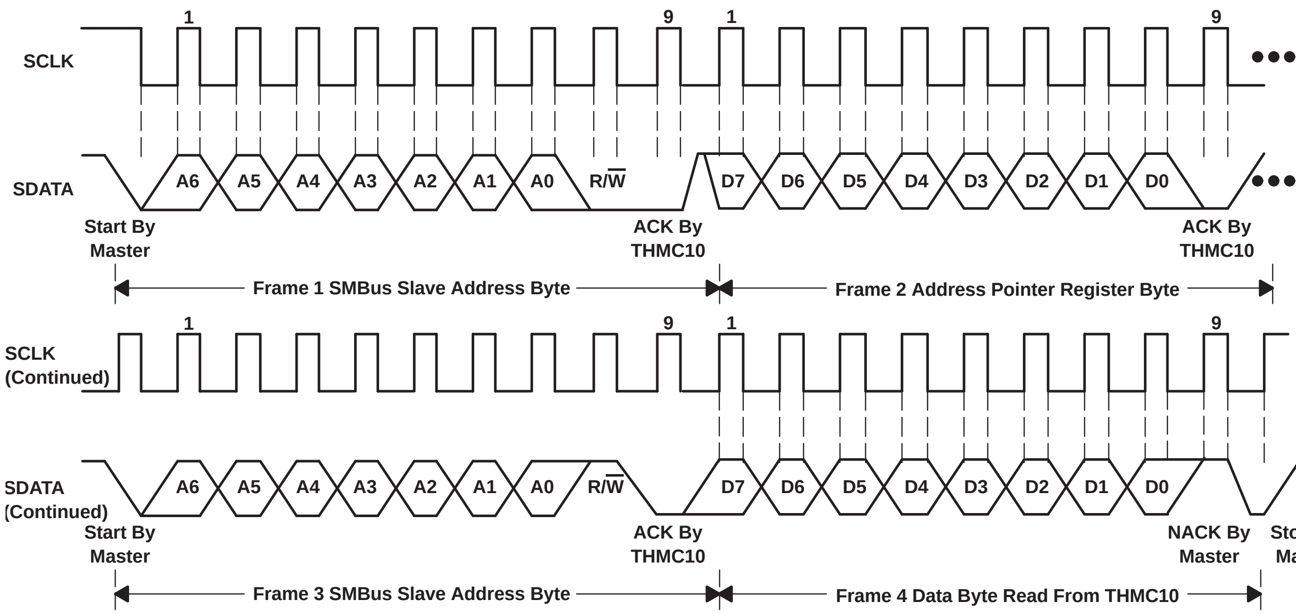


Figure 3. SMBus Timing Diagram for Read Byte Format

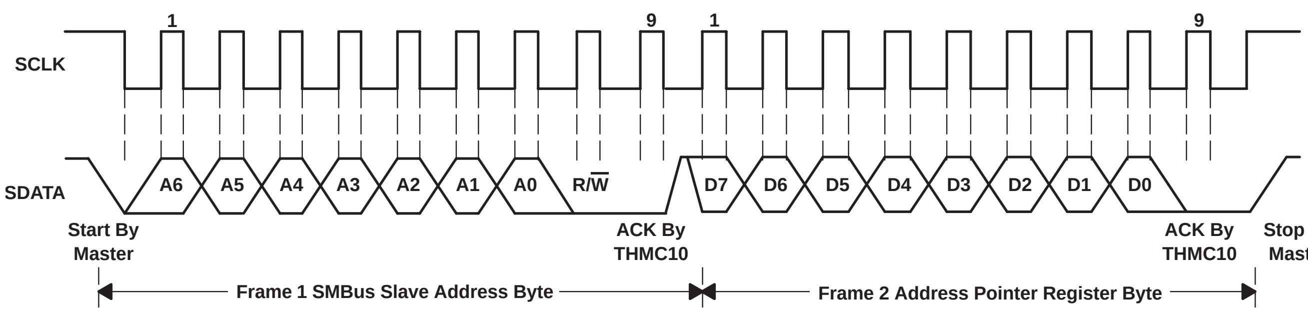


Figure 4. SMBus Timing Diagram for Send Byte Format (Used for One-Shot Command)

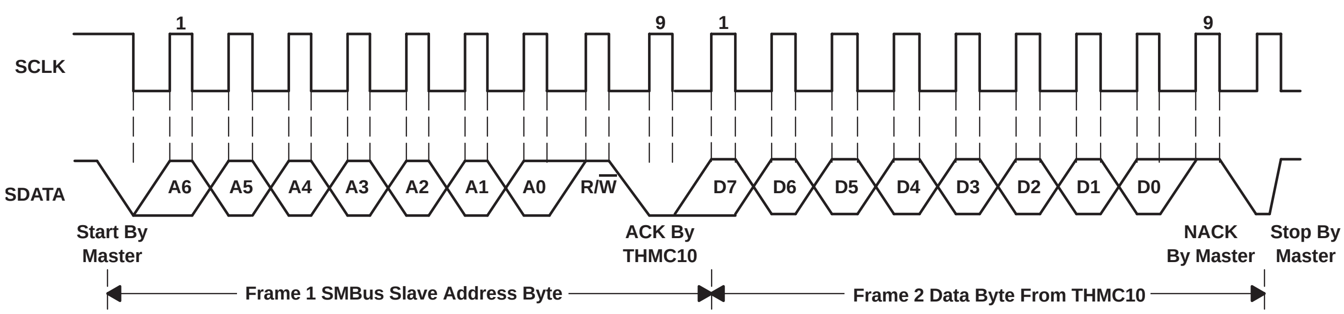


Figure 5. SMBus Timing Diagram for Recieve Byte Format

PRINCIPLES OF OPERATION

SMBus registers and addresses

Table 1. ADD{0:1} SMBus Slave Address Map

ADD0	ADD1	RESULTING THMC10 SMBus SLAVE ADDRESS
0	0	0011 000
0	3-State	0011 001
0	1	0011 010
3-State	0	0101 001
3-State	3-State	0101 010
3-State	1	0101 011
1	0	1001 100
1	3-State	1001 101
1	1	1001 110

Table 2. SDATA Temperature Data Format (In 8-Bit, 2s Complement)

TEMPERATURE (°C)	ROUNDED	DIGITAL OUTPUT
130.00	127	0 111 1111
127.00	127	0 111 1111
126.60	127	0 111 1111
25.25	25	0 001 1001
0.50	1	0 000 0001
0.25	0	0 000 0000
0.00	0	0 000 0000
−0.25	0	0 000 0000
−0.50	0	0 000 0000
−0.75	−1	1 111 1111
−1.00	−1	1 111 1111
−25.00	−25	1 110 0111
−25.25	−26	1 110 0110
−54.75	−55	1 100 1001
−55.00	−55	1 100 1001
−65.00	−65	1 011 1111

PRINCIPLES OF OPERATION

SMBus registers and addresses (continued)

Table 3. Address Pointer Register Map

REGISTER	ADDRESS POINTER	POR STATE	FUNCTION
RIT	00h	0000 0000†	Read internal temperature
RET	01h	0000 0000†	Read external temperature
RS	02h	0000 0000	Read status byte
RC	03h	0000 0000	Read configuration byte
RCR	04h	0000 0010	Read acquisition rate byte
RIHL	05h	0111 1111	Read internal high limit
RILL	06h	1100 1001	Read internal low limit
REHL	07h	0111 1111	Read external high limit
RELL	08h	1100 1001	Read external low limit
WC	09h	N/A	Write configuration byte
WCR	0Ah	N/A	Write acquisition rate byte
WIHL	0Bh	N/A	Write internal high threshold
WILL	0Ch	N/A	Write internal low threshold
WEHL	0Dh	N/A	Write external high threshold
WELL	0Eh	N/A	Write external low threshold
OSHT	0Fh	N/A	One-shot (uses send byte format)
MFG ID	FEh	0100 1001	Read manufacturer ID (0×49 for TI)
REV ID	FFh	N/A	Read silicon revision number

† If the THMC10 is in standby

Table 4. Configuration Register Bit Assignments

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	MASK	0	Masks $\overline{\text{ALERT}}$ interrupts if high.
6	Run/stop	0	Standby mode control bit, if high, standby mode is initiated. (Note: Does not disable SMBus Interface)
5 to 0			Reserved

Table 5. Status Register Bit Assignments

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	BUSY	0	A/D is busy acquiring when high.
6	LHIGH†	0	Internal high-temperature alarm has tripped when high, cleared by power-on reset (POR) or readout of entire status byte.
5	LLOW†	0	Internal low-temperature alarm has tripped when high, cleared by POR or readout of entire status byte.
4	RHIGH†	0	External high-temperature alarm has tripped when high, cleared by POR or readout of entire status byte.
3	RLOW†	0	External low-temperature alarm has tripped when high, cleared by POR or readout of entire status byte.
2	OPEN†	0	A high indicates an external diode open.
1 to 0		0	Reserved

† These flags stay high until cleared by POR or until the status byte register is read.

PRINCIPLES OF OPERATION

SMBus registers and addresses (continued)

Table 6. Acquistion Rate Register Bit Assignments

DATA	ACQUISITION RATE (Hz)	AVERAGE SUPPLY CURRENT (µA TYPICAL AT V_{DD}=3.3V)
00h	0.0625	40
01h	0.125	40
02h	0.25	40
03h	0.5	40
04h	1	42
05h	2	45
06h	4	55
07h	8	65
08h to FFh	Reserved	N/A

Table 7. Alert Response Address Map (Using Receive Byte Format in Figure 5)

THMC10 ALERT RESPONSE SMBUS SLAVE ADDRESS	ADD1	ADD0	DATA IF $\overline{\text{ALERT}}$ LOW
0001 100	0	0	0011 000
0001 100	0	3-State	0011 001
0001 100	0	1	0011 010
0001 100	3-State	0	0101 001
0001 100	3-State	3-State	0101 010
0001 100	3-State	1	0101 011
0001 100	1	0	1001 100
0001 100	1	3-State	1001 101
0001 100	1	1	1001 110

functional description

standby input ($\overline{\text{STBY}}$)

Standby mode disables the A/D and reduces the supply current drain to less than 10 µA.

Standby mode is engaged by forcing the $\overline{\text{STBY}}$ terminal low or by setting the *start/stop* bit in the configuration byte register to a 1.

Hardware and software standby modes behave almost identically. All data is retained in memory and the SMBus interface is active and scanning for reads and writes. The only difference is that in hardware standby mode, the one-shot command does not initiate an acquisition. The standby mode is not a shutdown mode. With activity on the SMBus, extra supply current is drawn (see A/D and supply dc electrical characteristics). In the software standby mode, the THMC10 can be forced to perform temperature acquisitions via the one-shot command, despite the *start/stop* bit being high.

PRINCIPLES OF OPERATION

standby input ($\overline{\text{STBY}}$) (continued)

Forcing the $\overline{\text{STBY}}$ terminal low activates the hardware standby mode. In a notebook computer, this line may be connected to the system suspend-state signal. Pulling the $\overline{\text{STBY}}$ terminal low overrides any software acquisition command. If a hardware or software standby command is received while an acquisition is in progress, the acquisition cycle is truncated, and the data from that acquisition is not latched into either temperature reading register. The previous data is not changed and remains available.

Peak supply current drain during an auto-aquire period is typically 300 µA. Slowing down the auto-acquire rate minimizes the average supply current (see A/D and supply dc electrical characteristics). In between acquisitions, the instantaneous supply current is about 40 µA, due to the current consumed by the auto-aquire rate timer. In standby mode, supply current drops to about 3 µA. At very low supply voltages (under the power-on-reset threshold), the supply current is higher due to the address terminal bias currents. It can be as high as 100 µA, depending on ADD0 and ADD1 settings.

under/overtemperature and remote diode diagnostics interrupt alert terminal ($\overline{\text{ALERT}}$)

The THMC10 allows the user to program upper and lower temperature limits for both the on-chip and the remote temperature sensor. If any of these limits are exceeded, or an open external diode is detected, the THMC10 asserts the $\overline{\text{ALERT}}$ to a logic low state to alert the user that an interrupt has occurred. This feature is useful in applications where minimal SMBus traffic is desired by only interrogating the THMC10 for faults or temperature when a fault has occurred.

It is recommended that the user always double-check the validity of an $\overline{\text{ALERT}}$ condition by reading the current temperature values and comparing them with the programmed high and low temperature limits.

The $\overline{\text{ALERT}}$ function can also be masked by setting bit 6 in the configuration register to a logic 1. If this bit is set, the $\overline{\text{ALERT}}$ terminal is not asserted low, even if a trip point is reached.

The $\overline{\text{ALERT}}$ signal and corresponding status register bits can only be cleared by reading from the alert response address (0001 100) or by a power-on reset of the device (see alert response address section).

NOTE:
The $\overline{\text{ALERT}}$ terminal is an open-drain output and requires an external pullup resistor.

alert response address (0001 100)

The SMBus alert response address allows the user to quickly check the status of the $\overline{\text{ALERT}}$ terminal via the SMBus receive byte protocol (see Figure 5). This is useful in applications where another device on the SMBus needs to know the status of the THMC10 $\overline{\text{ALERT}}$ terminal without requiring the complex logic needed to decode the contents of the status register. If the $\overline{\text{ALERT}}$ has been asserted low, the data read from the alert response address is the THMC10 slave address (determined by ADD0 and ADD1 – see Table 8). If the fault condition which caused the $\overline{\text{ALERT}}$ to go low is no longer present when the alert response address is successfully read, the $\overline{\text{ALERT}}$ terminal returns to a logic high state and the corresponding bits in the THMC10 status register are cleared. If the $\overline{\text{ALERT}}$ terminal has not been asserted low, the THMC10 responds to the alert response address with a NACK signal after the alert response address is sent.

The alert response address can activate several different slave devices simultaneously. It is similar to the general call address outlined in the I^2C Bus specification. If more than one device attempts to respond to the alert response address, SMBus arbitration rules apply, causing the device with the lowest slave address to win control of the SMBus. The device that loses arbitration in this example does not generate an ACK signal and continues to hold the $\overline{\text{ALERT}}$ terminal low until the device with the losing slave address is serviced. This technique requires the SMBus host controller to use level-sensitive interrupt inputs in order to assure that each device is serviced.

PRINCIPLES OF OPERATION

SMBus slave address select terminals (ADD0 and ADD1)

The ADD0 and ADD1 terminals allow the user to select between nine unique SMBus slave addresses to allow up to nine THMC10 devices to be used by the same SMBus host controller. The following truth table shows how the voltage at ADD0 and ADD1 determines the SMBus slave address of the THMC10.

Table 8. SMBus Slave Address Map (ADD0 and ADD1)

ADD0	ADD1	RESULTING SMBus ADDRESS
0	0	0011 000
0	3-State	0011 001
0	1	0011 010
3-State	0	0101 001
3-State	3-State	0101 010
3-State	1	0101 011
1	0	1001 100
1	3-State	1001 101
1	1	1001 110

SMBus serial clock input terminal (SCLK)

The SCLK terminal allows the host controller to send a clock signal that synchronizes the data coming into or out of the SDATA terminal of the THMC10. The frequency of this clock can be anywhere between 10 kHz and 100 kHz. Timing diagrams showing the relationship of SCLK to SDATA are shown in Figure 1 through Figure 4.

SMBus serial data input/output terminal (SDATA)

The SDATA terminal allows the host controller to program the THMC10 with set points and with configuration data. The SDATA terminal also allows the THMC10 to send data back to the host controller (remote and local temperature, interrupt status, etc.). Data sent into or out of the SDATA terminal is synchronous with the rising edge of SCLK. Timing diagrams in Figure 1 through Figure 5 show the relationship between SDATA and SCLK. Table 1 through Table 5 show the THMC10 register maps that are used to configure and read the THMC10.

PRINCIPLES OF OPERATION

external temperature sensor connections (DXP and DXN)

The DXP and DXN terminals are used to sense the remote temperature of either a microprocessor die or a simple diode-connected transistor. Referring to Figure 6, the THMC10 has an internal state machine controlling an analog MUX, an 8-bit A/D converter, plus 10-µA and 90-µA nominal current sources. The analog MUX switches between the THMC10's internal temperature sensor and the external one connected to DXP and DXN. This allows the use of only one 8-bit A/D converter, eliminating errors which would be present when using two separate A/Ds. The THMC10 takes a V_{BE} measurement at 100 µA, then takes a V_{BE} measurement at 10 µA, and subtracts the difference between the two sampled values. It then scales the resulting ΔV_{BE} measurement into a 2s complement, 8-bit binary format that is available over the SMBus interface (see Table 2). By using two different current levels and a single diode-connected transistor to measure the ΔV_{BE}, the absolute V_{BE} is canceled, and therefore no calibration is needed.

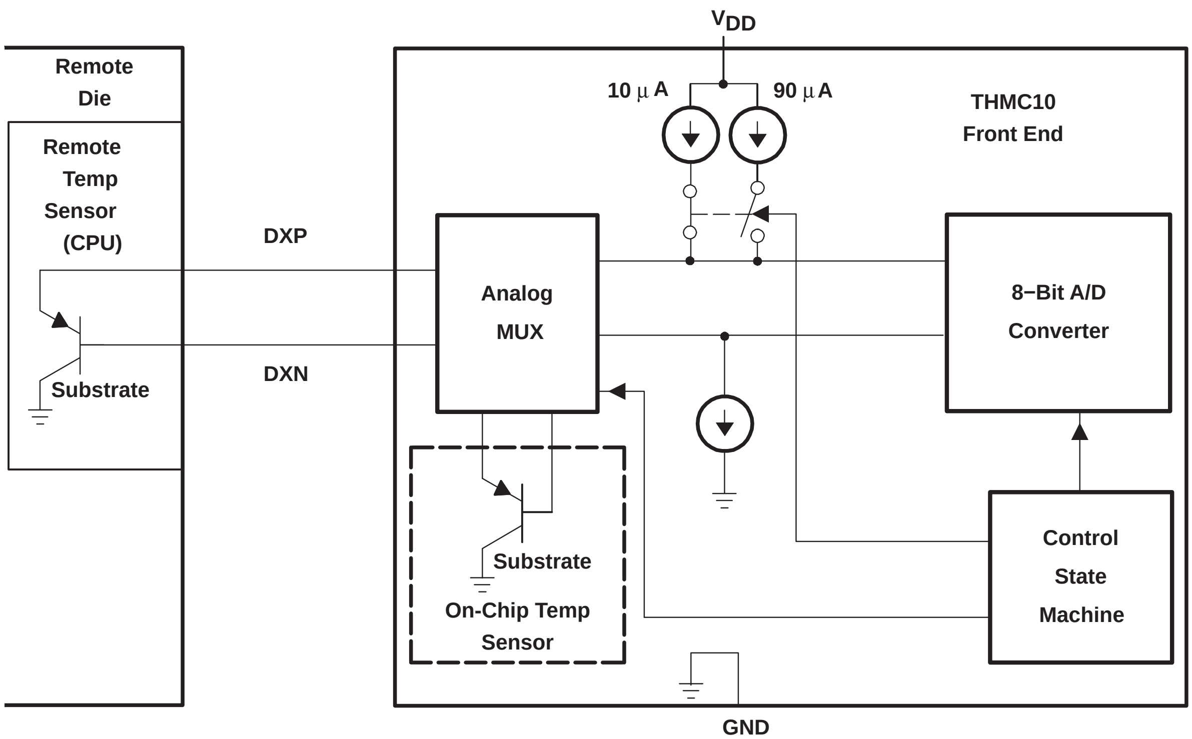


Figure 6. Temperature Measurement Block Diagram

external temperature sensor diagnostics (DXP and DXN)

The THMC10 provides diagnostic capabilities to allow detection of either an open external sensor or a shorted external sensor. When DXP is shorted to GND or V_{DD}, the THMC10 reports 127°C for the external temperature. If the interrupt mask bit is not set in the configuration register, it asserts the $\overline{\text{ALERT}}$ terminal low and sets bit two in the status register. When DXP is shorted to DXN, the THMC10 reports 0°C for the external temperature and no fault is reported. If any of the above conditions exceed a temperature limit, then a temperature limit error is also indicated in the status register if the interrupt mask bit is not set.

PRINCIPLES OF OPERATION

PC board layout considerations

- Place the THMC10 as close as practical to the remote diode. In a noisy environment, such as a computer motherboard, this distance can be 4 inches to 8 inches (typical) or more, as long as the worst noise sources (such as CRTs, clock generators, memory buses, and ISA/PCI buses) are avoided.
- Route the DXP–DXN lines away from the deflection coils of a CRT. Also, avoid routing the traces across a fast memory bus which can easily introduce 30°C error even with good filtering. Otherwise, most noise sources are fairly benign.
- Route the DXP and DXN traces in parallel and in close proximity to each other, away from any high-voltage traces such as 12 Vdc. Leakage currents from PC board contamination must be be taken into consideration, since a 20-MΩ leakage path from DXP to ground causes about 1°C error.
- Connect guard traces to GND on either side of the DXP–DXN traces (Figure 7). With guard traces in place, routing near high-voltage traces is not an issue.
- Route through as few vias and crossunders as possible to minimize copper/solder thermocouple effects.
- When introducing a thermocouple, insure that both the DXP and the DXN paths have matching thermocouples. In general, PC board induced thermocouples are not a serious problem. A copper-solder thermocouple exhibits 3 μV/°C, and it takes about 200 μV of voltage error at DXP–DXN to cause a 1°C measurement error. Hence, most parasitic thermocouple errors are swamped out.
- Use wide traces. Narrow traces are more inductive and tend to pick up radiated noise. The 10-mil widths and spacings recommended in Figure 7 are not absolutely necessary as they offer only a minor improvement in leakage and noise, but usage is recommended where practical.
- Copper can not be used as an EMI shield and only ferrous materials such as steel work well. Placing a copper ground plane between the DXP−DXN traces and traces carrying high-frequency noise signals does not help reduce EMI.

PC board layout checklist

- Place the THMC10 as close as possible to the remote diode.
- Keep traces away from high voltages (12 V bus).
- Keep traces away from fast data/memory buses and CRTs.
- Use recommended trace widths and spacings.
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND.
- Place the noise filter and the 0.1-μF V_{DD} bypass capacitors close to the THMC10.

PRINCIPLES OF OPERATION

PC board layout checklist (continued)

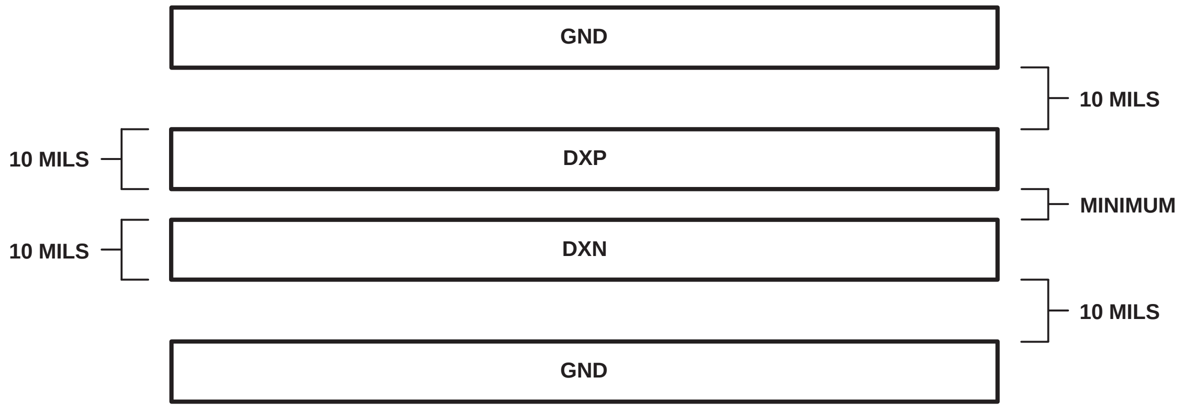


Figure 7. Recommended PC Board Layout for DXP/DXN Traces

uses of twisted pair and shielded cables

For remote-sensor distances longer than 8 inches or in particularly noisy environments, a twisted pair is recommended. Its practical length is 6 feet to 12 feet (typical) before noise becomes a problem, as tested in a noisy electronics laboratory. For longer distances, the best solution is a shielded twisted pair like that used for audio microphones. For example, a Belden® #8451 works well for distances up to 100 feet in a noisy environment. Connect the twisted pair to DXP and DXN and the shield to GND, and leave the shield's remote end unterminated. Excess capacitance at DXN limits practical remote sensor distances (see A/D and supply dc electrical characteristics). For very long cable runs, the cable's parasitic capacitance often provides noise filtering; hence, the 2200-pF capacitor can often be removed or reduced in value. Cable resistance also affects remote-sensor accuracy. A 1-Ω series resistance introduces about 0.5°C error.

Belden is a registered trademark of Belden Corporation.

APPLICATION INFORMATION

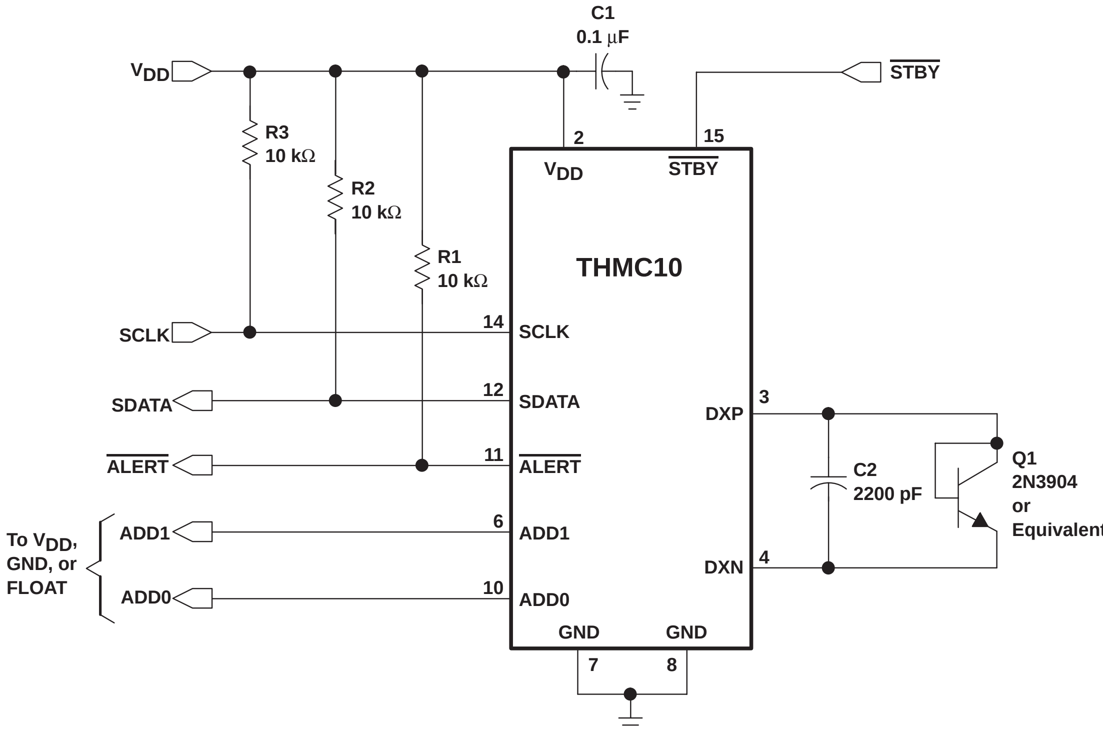


Figure 8. Typical Application Schematic

PERFORMANCE DATA

temperature error vs power supply sinusoidal noise frequency

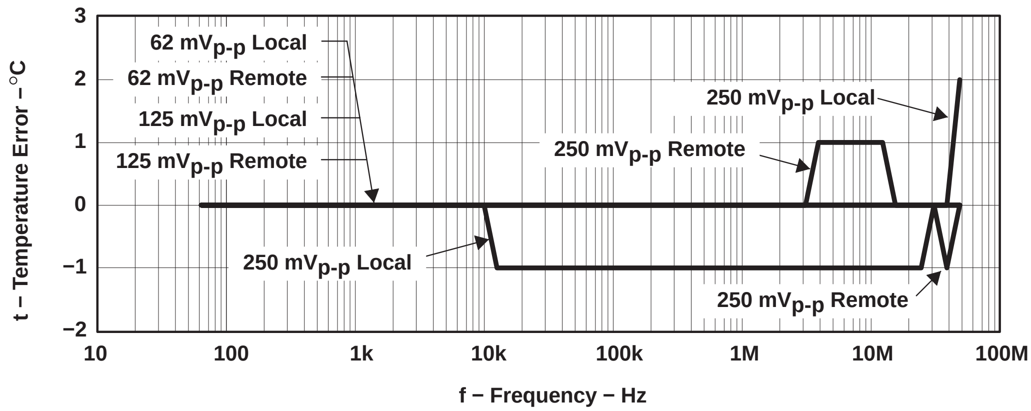
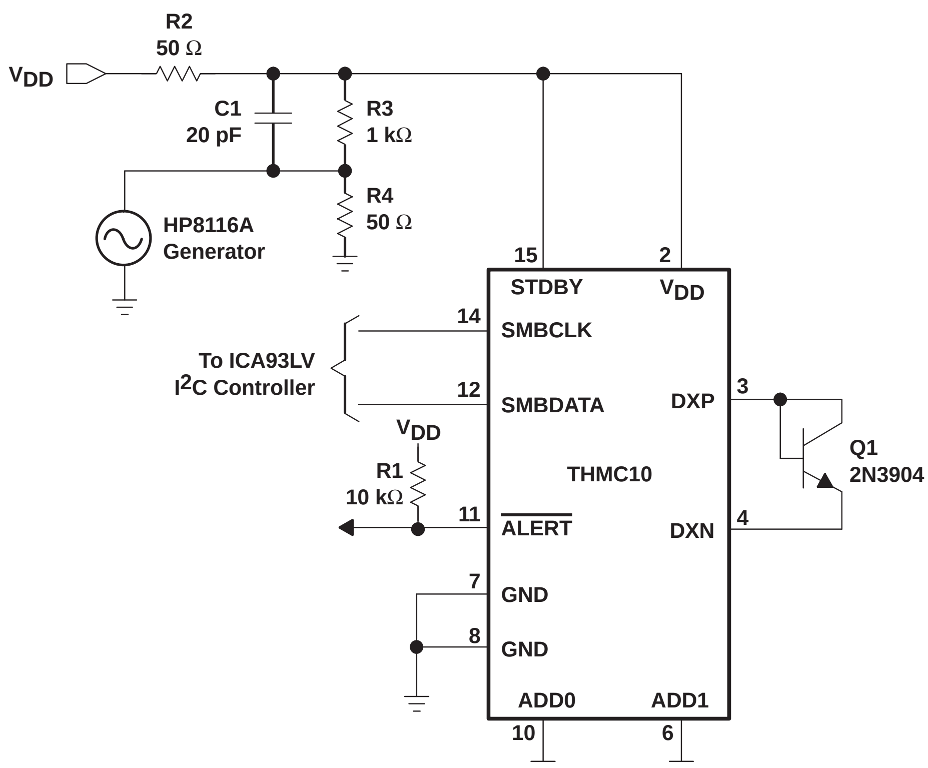


Figure 9. Data Plot



NOTE: No 0.1 µF V_{DD} capacitor.

Figure 10. Test Circuit

PERFORMANCE DATA

temperature error vs PNP collector square wave noise frequency

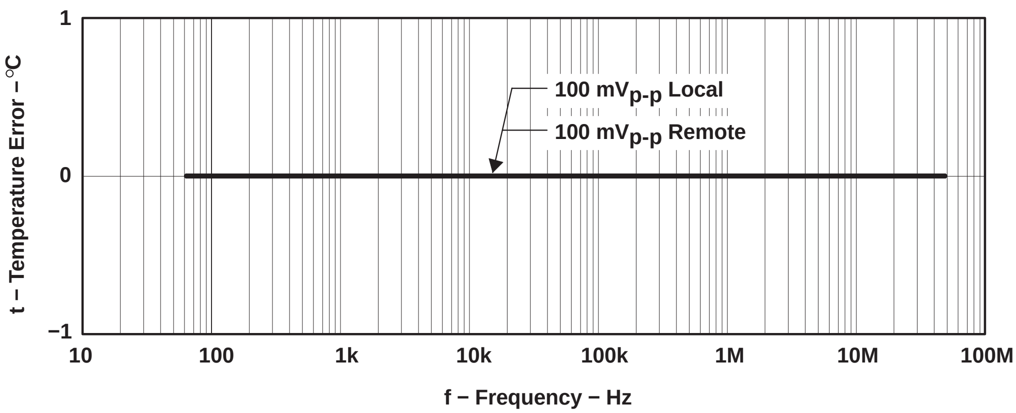
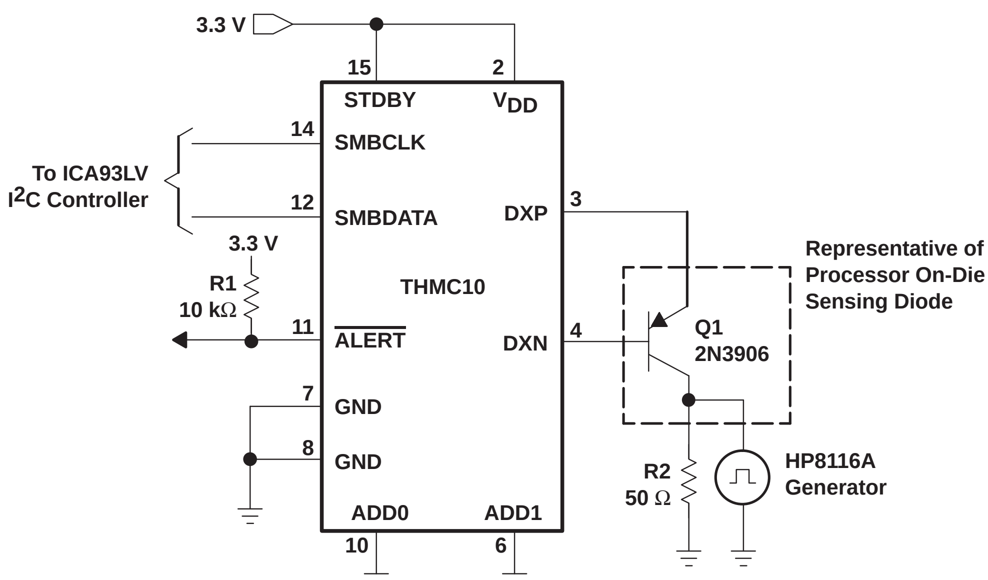


Figure 11. Data Plot



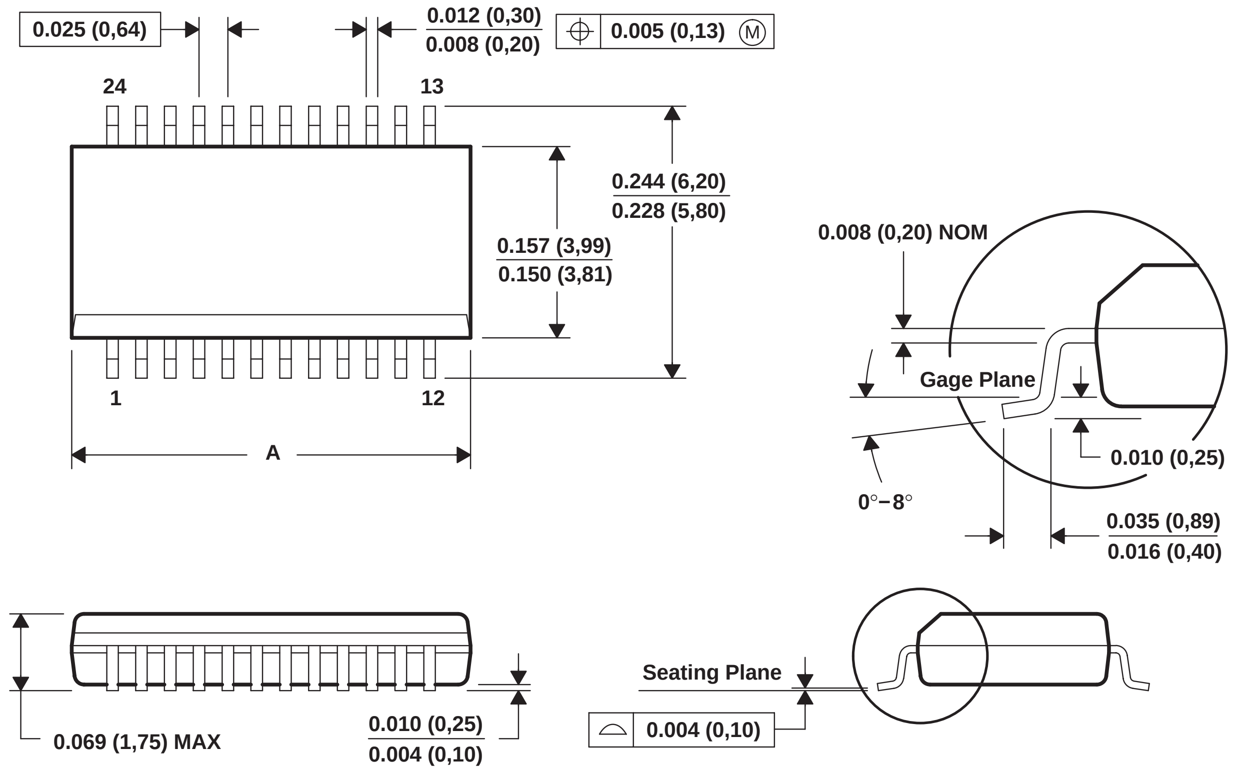
NOTE: No 0.1 µF V_{DD} capacitor.
No 2200 pF DXP-DXN filter capacitor.

Figure 12. Test Circuit

MECHANICAL DATA

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24−PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THMC10DBQR	OBSOLETE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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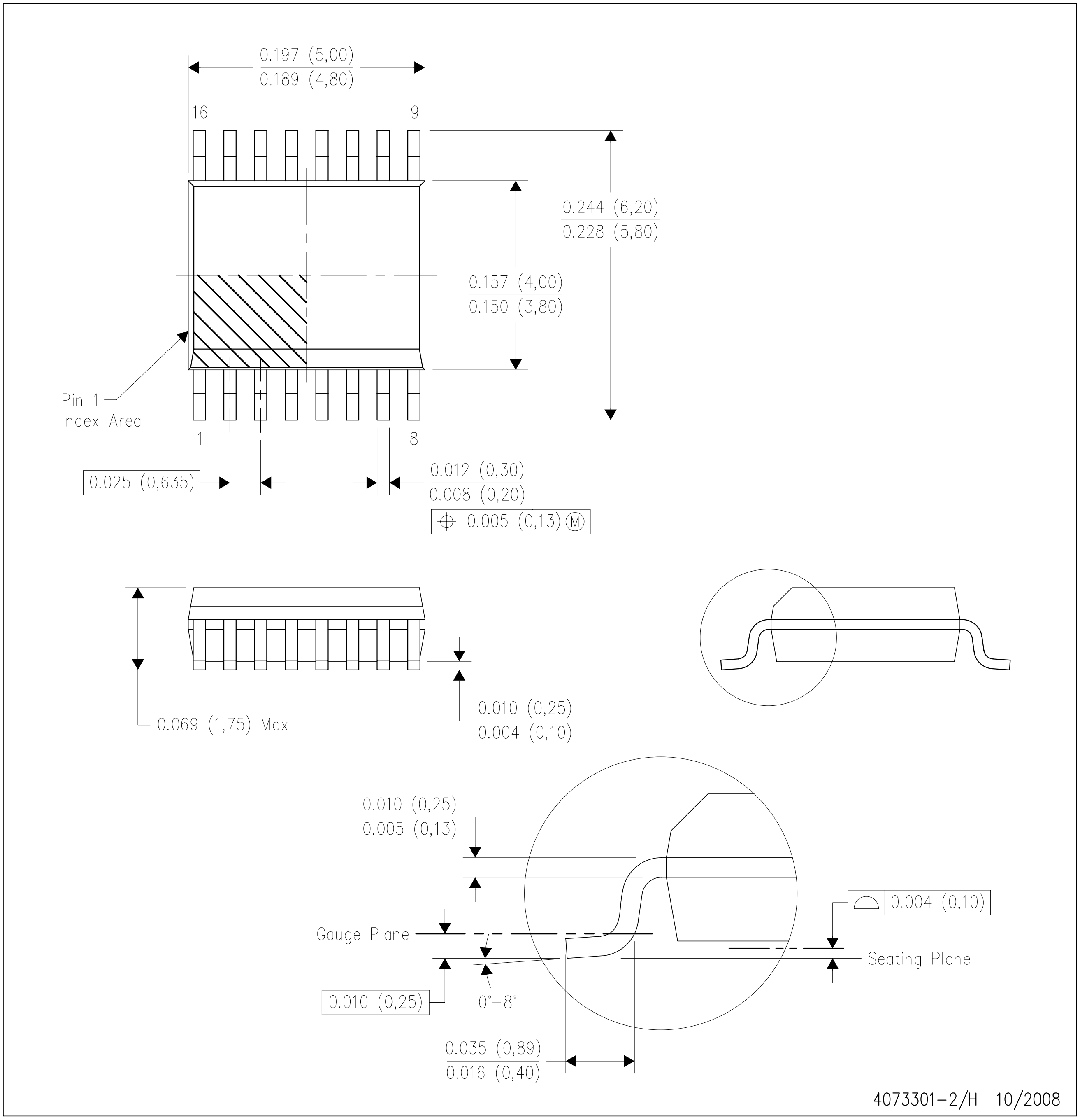
DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.