# BUK95/9606-40B

TrenchMOS™ logic level FET

**Rev. 01 — 14 May 2003** **Product data**

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology.

Product availability:

BUK9506-40B in SOT78 (TO-220AB)

BUK9606-40B in SOT404 (D$^2$-PAK).

### 1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible.

### 1.3 Applications

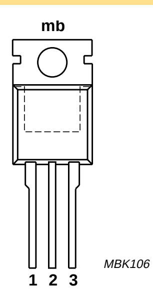
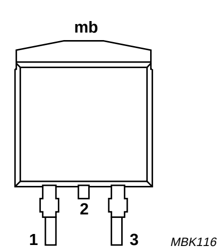
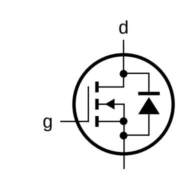
- Automotive systems
- Motors, lamps and solenoids
- 12 V loads
- General purpose power switching.

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 494$ mJ
- $I_D \leq 75$ A
- $R_{DSon} = 5.7$ mΩ (typ)
- $P_{tot} \leq 203$ W.

## 2. Pinning information

**Table 1: Pinning - SOT78 and SOT404, simplified outlines and symbol**

| Pin | Description | Simplified outline | | Symbol |
|---|---|---|---|---|
| 1 | gate (g) |  |  |  |
| 2 | drain (d) [1] | | | |
| 3 | source (s) | | | |
| mb | mounting base, connected to drain (d) | SOT78 (TO-220AB) | SOT404 (D$^2$-PAK) | |

[1] It is not possible to make connection to pin 2 of the SOT404 package.

# 3. Limiting values

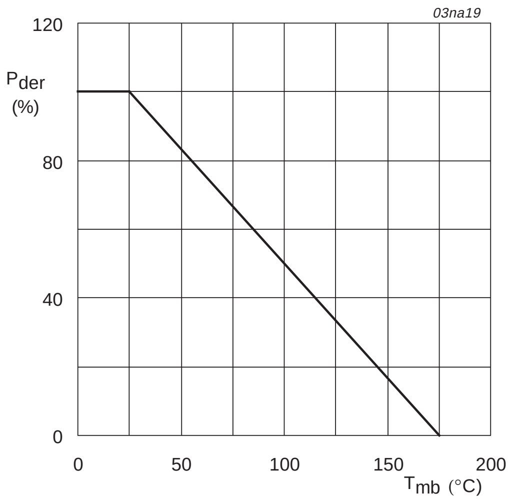
**Table 2: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | | | - | 40 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | $R_{GS}$ = 20 kΩ | | - | 40 | V |
| $V_{GS}$ | gate-source voltage (DC) | | | - | ±15 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; Figure 2 and 3 | [1] | - | 129 | A |
| | | | [2] | - | 75 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 5 V; Figure 2 | [2] | - | 75 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3 | | - | 516 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | | - | 203 | W |
| $T_{stg}$ | storage temperature | | | –55 | +175 | °C |
| $T_j$ | junction temperature | | | –55 | +175 | °C |
| **Source-drain diode** | | | | | | |
| $I_{DR}$ | reverse drain current (DC) | $T_{mb}$ = 25 °C | [1] | - | 129 | A |
| | | | [2] | - | 75 | A |
| $I_{DRM}$ | peak reverse drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs | | - | 516 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 75 A; $V_{DS} \leq 40$ V; $V_{GS}$ = 5 V; $R_{GS}$ = 50 Ω; starting $T_{mb}$ = 25 °C | | - | 494 | mJ |

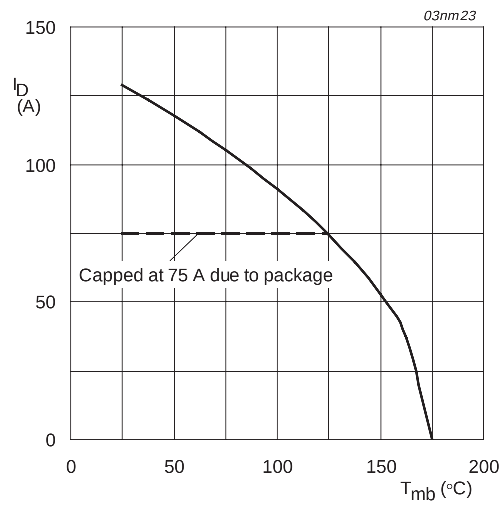
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



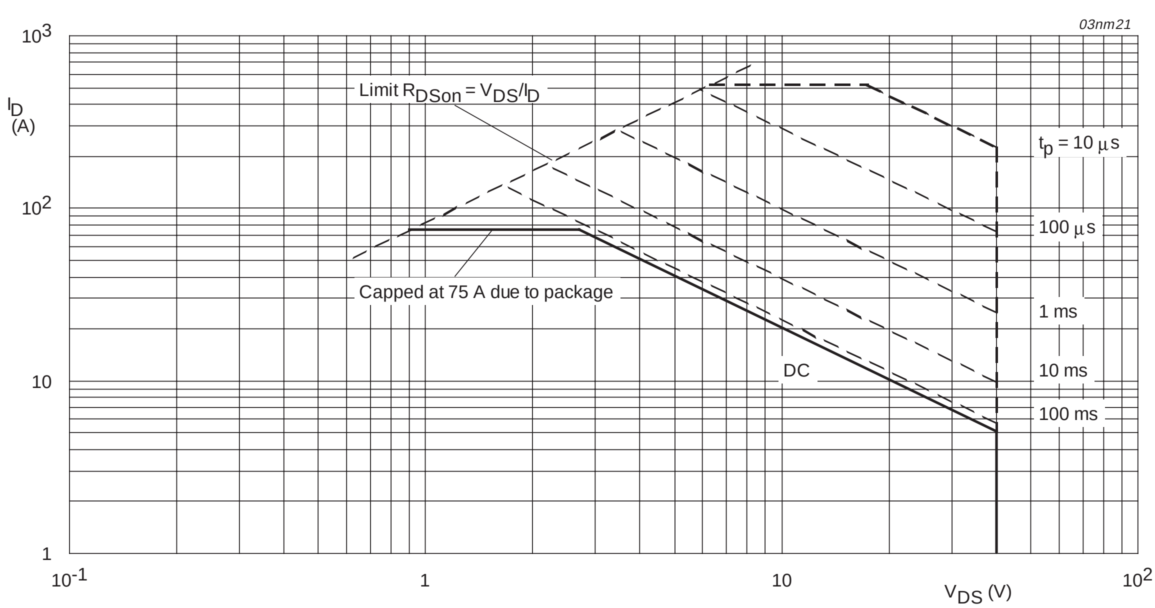

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**




$V_{GS} \geq 5$ V

**Fig 2. Continuous drain current as a function of mounting base temperature.**




$T_{mb} = 25$ °C; $I_{DM}$ single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 4. Thermal characteristics

**Table 3: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 0.74 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | | | | |
| | SOT78 (TO-220AB) | vertical in still air | - | 60 | - | K/W |
| | SOT404 ($D^2$-PAK) | minimum footprint; mounted on a PCB | - | 50 | - | K/W |

### 4.1 Transient thermal impedance

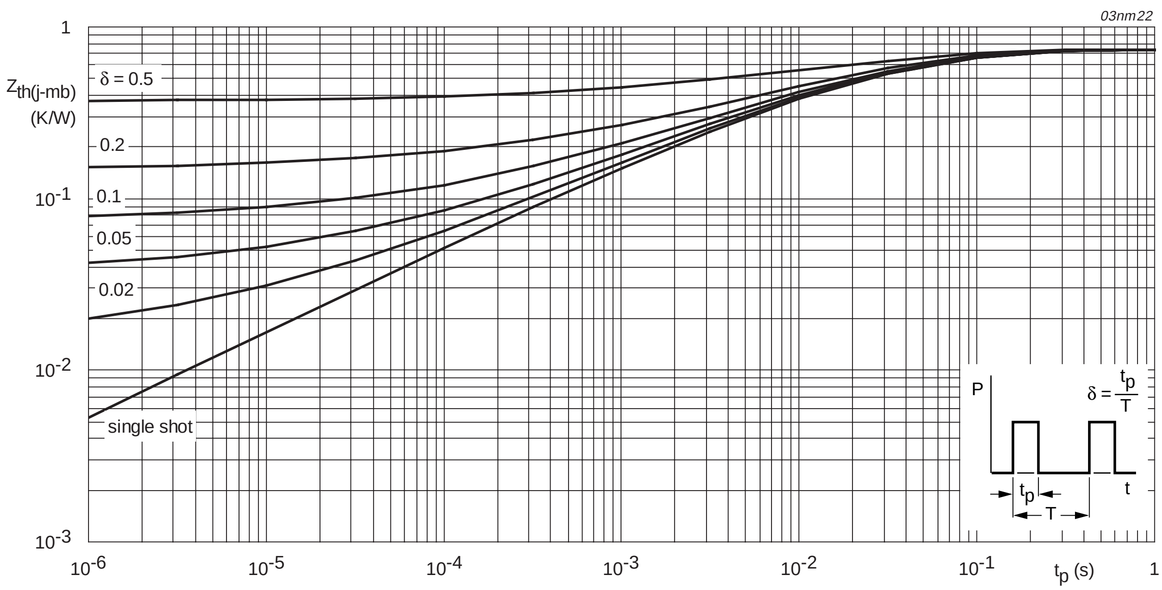



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

# 5. Characteristics

**Table 4: Characteristics**

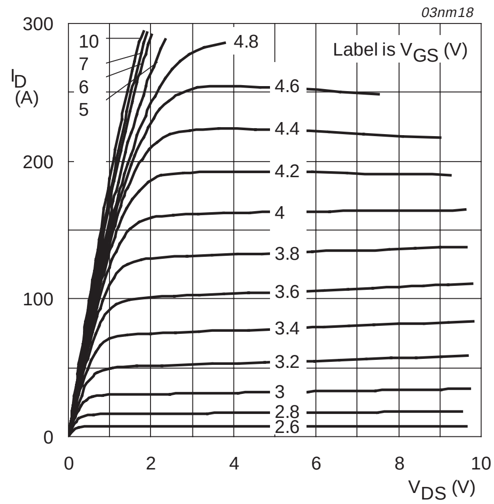
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 0.25 mA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 40 | - | - | V |
| | | $T_j$ = –55 °C | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 1.1 | 1.5 | 2 | V |
| | | $T_j$ = 175 °C | 0.5 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 2.3 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | 0.02 | 1 | µA |
| | | $T_j$ = 175 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±15 V; $V_{DS}$ = 0 V | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 5.7 | 6.4 | mΩ |
| | | $T_j$ = 175 °C | - | - | 12.2 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A | - | - | 7.1 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A | - | 4.1 | 5 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $V_{GS}$ = 5 V; $V_{DD}$ = 32 V; $I_D$ = 25 A; Figure 14 | - | 44 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 11 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 17 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; Figure 12 | - | 3967 | 4901 | pF |
| $C_{oss}$ | output capacitance | | - | 634 | 760 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 278 | 380 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 5 V; $R_G$ = 10 Ω | - | 43 | - | ns |
| $t_r$ | rise time | | - | 145 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 132 | - | ns |
| $t_f$ | fall time | | - | 92 | - | ns |
| $L_d$ | internal drain inductance | from drain lead 6 mm from package to center of die | - | 4.5 | - | nH |
| | | from contact screw on mounting base to center of die SOT78 | - | 3.5 | - | nH |
| | | from upper edge of drain mounting base to center of die SOT404 | - | 2.5 | - | nH |
| $L_s$ | internal source inductance | from source lead to source bond pad | - | 7.5 | - | nH |

**Table 4: Characteristics**...*continued*

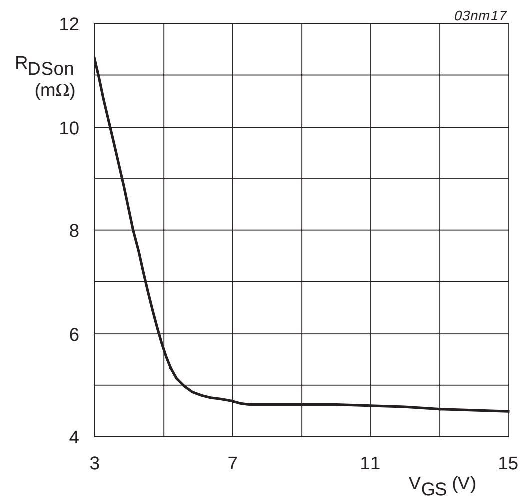
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; Figure 15 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = –100 A/µs $V_{GS}$ = –10 V; $V_{DS}$ = 30 V | - | 61 | - | ns |
| $Q_r$ | recovered charge | | - | 57 | - | nC |



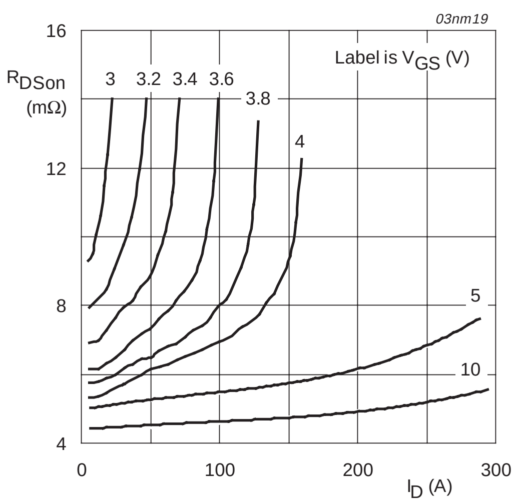

$T_j = 25$ °C; $t_p = 300$ µs

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



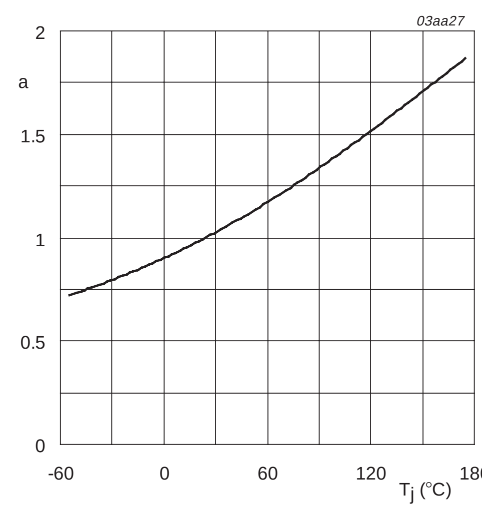

$T_j = 25$ °C; $I_D = 25$ A

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



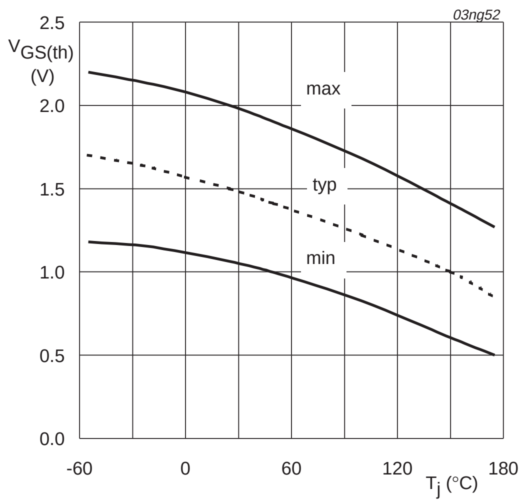

$T_j = 25$ °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



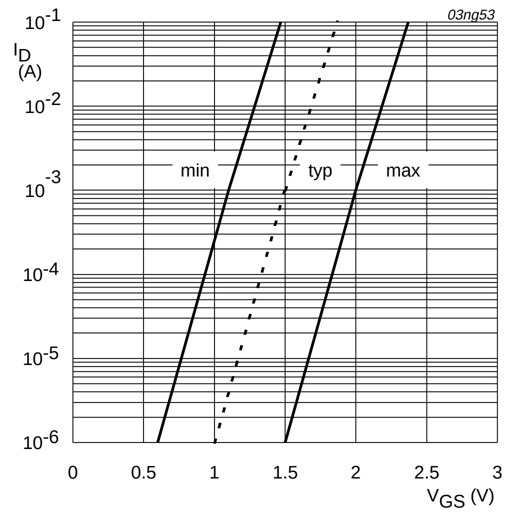

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



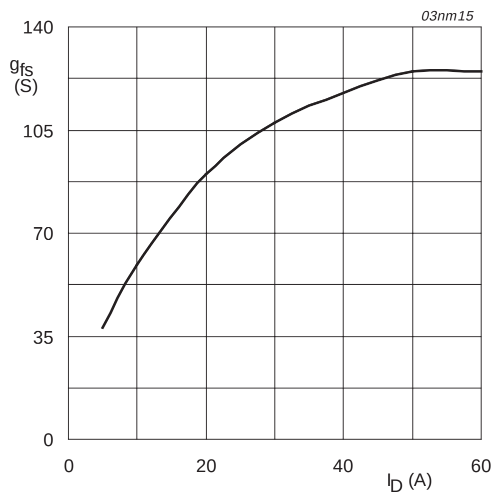

$I_D$ = 1 mA; $V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



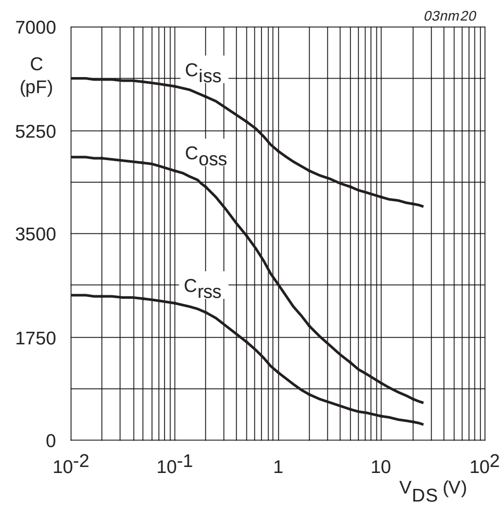

$T_j$ = 25 °C; $V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



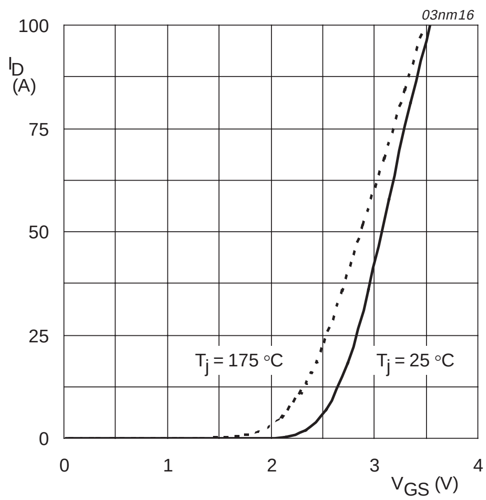

$T_j$ = 25 °C; $V_{DS}$ = 25 V

**Fig 11. Forward transconductance as a function of drain current; typical values.**



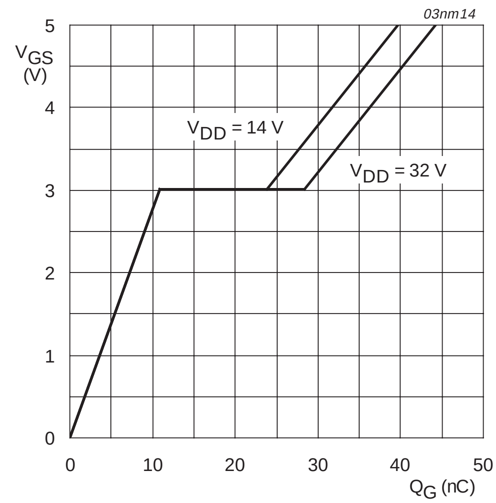

$V_{GS}$ = 0 V; f = 1 MHz

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



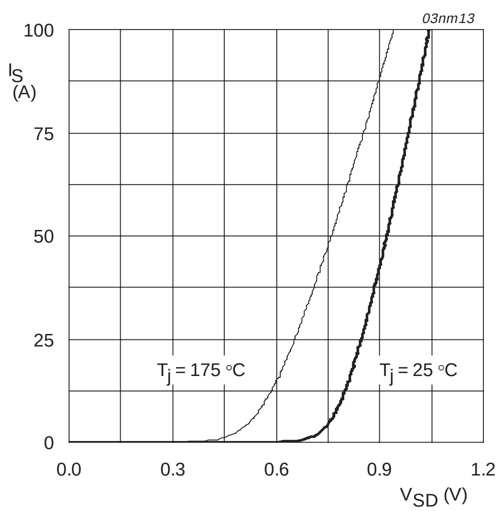

$V_{DS}$ = 25 V

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig 14. Gate-source voltage as a function of gate charge; typical values.**

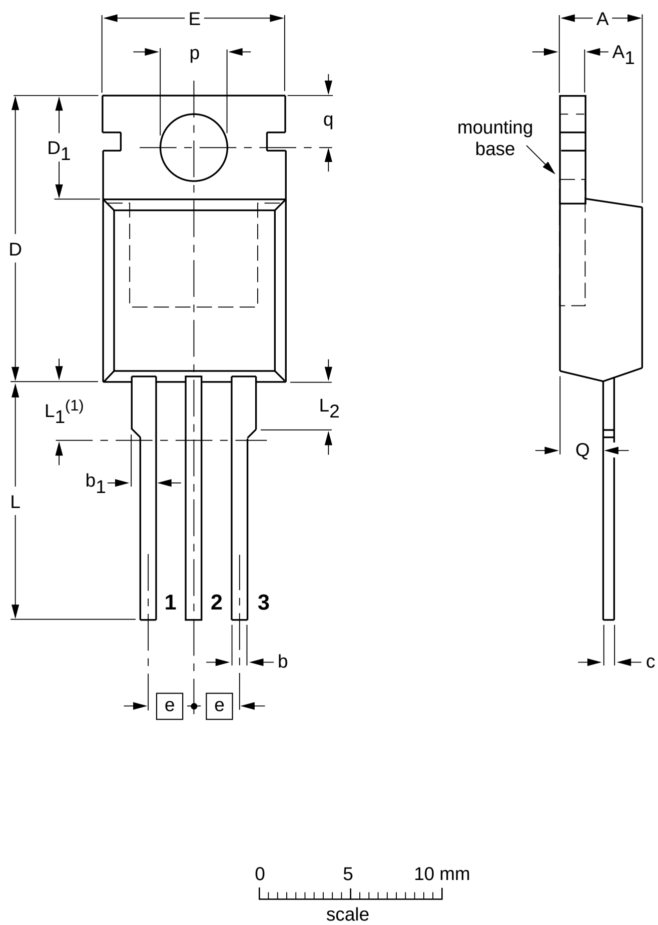



$V_{GS}$ = 0 V

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**

## 6. Package outline

**Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB** **SOT78**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | c | D | $D_1$ | E | e | L | $L_1^{(1)}$ | $L_2$ max. | p | q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.39<br>1.27 | 0.9<br>0.7 | 1.3<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.4<br>5.9 | 10.3<br>9.7 | 2.54 | 15.0<br>13.5 | 3.30<br>2.79 | 3.0 | 3.8<br>3.6 | 3.0<br>2.7 | 2.6<br>2.2 |

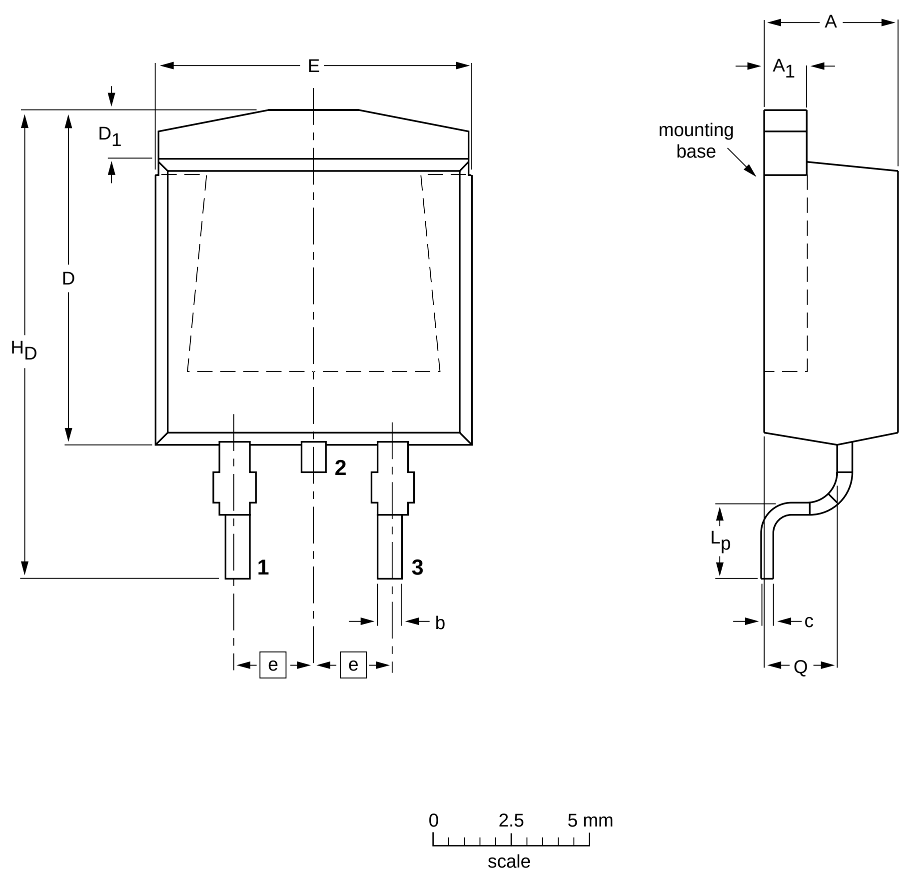
**Note**

1. Terminals in this zone are not tinned.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT78 | | 3-lead TO-220AB | SC-46 | | | ~~00-09-07~~<br>01-02-16 |

**Fig 16. SOT78 (TO-220AB).**

**Plastic single-ended surface mounted package (Philips version of $D^2$-PAK); 3 leads (one lead cropped)** **SOT404**



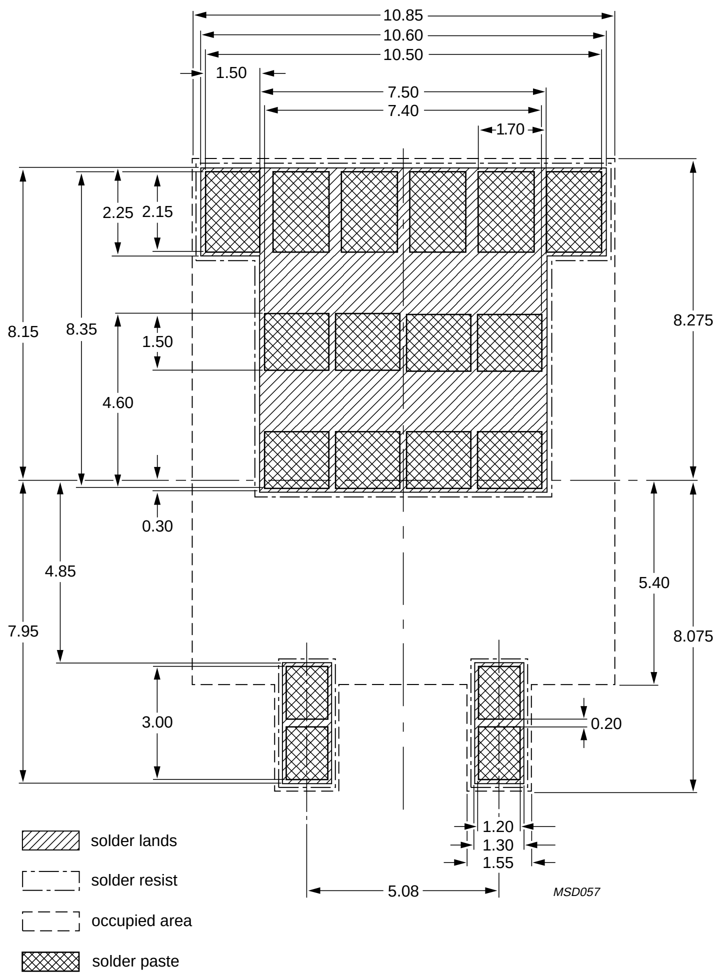

DIMENSIONS (mm are the original dimensions)

| UNIT | A | $A_1$ | b | c | D max. | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.50<br>4.10 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 11 | 1.60<br>1.20 | 10.30<br>9.70 | 2.54 | 2.90<br>2.10 | 15.80<br>14.80 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT404 | | | | | | ~~99-06-25~~<br>01-02-12 |

**Fig 17. SOT404 ($D^2$-PAK).**

# 7. Soldering




Dimensions in mm.

**Fig 18. Reflow soldering footprint for SOT404.**

# 8. Revision history

**Table 5: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20030514 | - | Product data (9397 750 11241) |

## 9. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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# Contents





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