1.0 Product Description

1.1 Functional Overview

The VSC9142 is a dual-mode STS-48c/AU-4-16c SONET/SDH to packet/ATM framing device. In the POS (packet over SONET) mode, the device can be used in equipment interconnecting IP/PPP/HDLC equipment over public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used in equipment interconnecting ATM switches. Features of the VSC9142 include: full insertion/extraction of the transport overhead, bit error rate and extensive SONET/packet/cell performance monitoring, packet/cell filtering and discarding functionalities, JTAG TAP controller, and an 8-bit CPU interface with eight general purpose I/O ports.

When used in conjunction with a high-speed mux/demux transceiver, this device provides a complete physical layer solution for packet/ATM over SONET/SDH, LAPS (ITU COM 7-224), and certain Ethernet over SONET/SDH applications at the STS-48/STM-16 line rate. In addition, this device provides a 4-bit interface for higher bandwidth applications at STS-192/STM-64 line rates. The VSC9142 integrates the following major functional blocks, illustrated in Figure 1.1.

- Serial or 4-bit Line-Side Interface
- 32-bit Packet/UTOPIA Drop-Side Interface
- Packet/ATM Mapping/Demapping
- SONET/SDH Section, Line, and Path SPE/VC Overhead Processing
- Transport Overhead Insertion/Extraction
- SONET/SDH Section and Path Trace Buffers
- Generic 8-Bit Microprocessor Interface
- Bit Error Rate Monitor
- JTAG Test Access Port

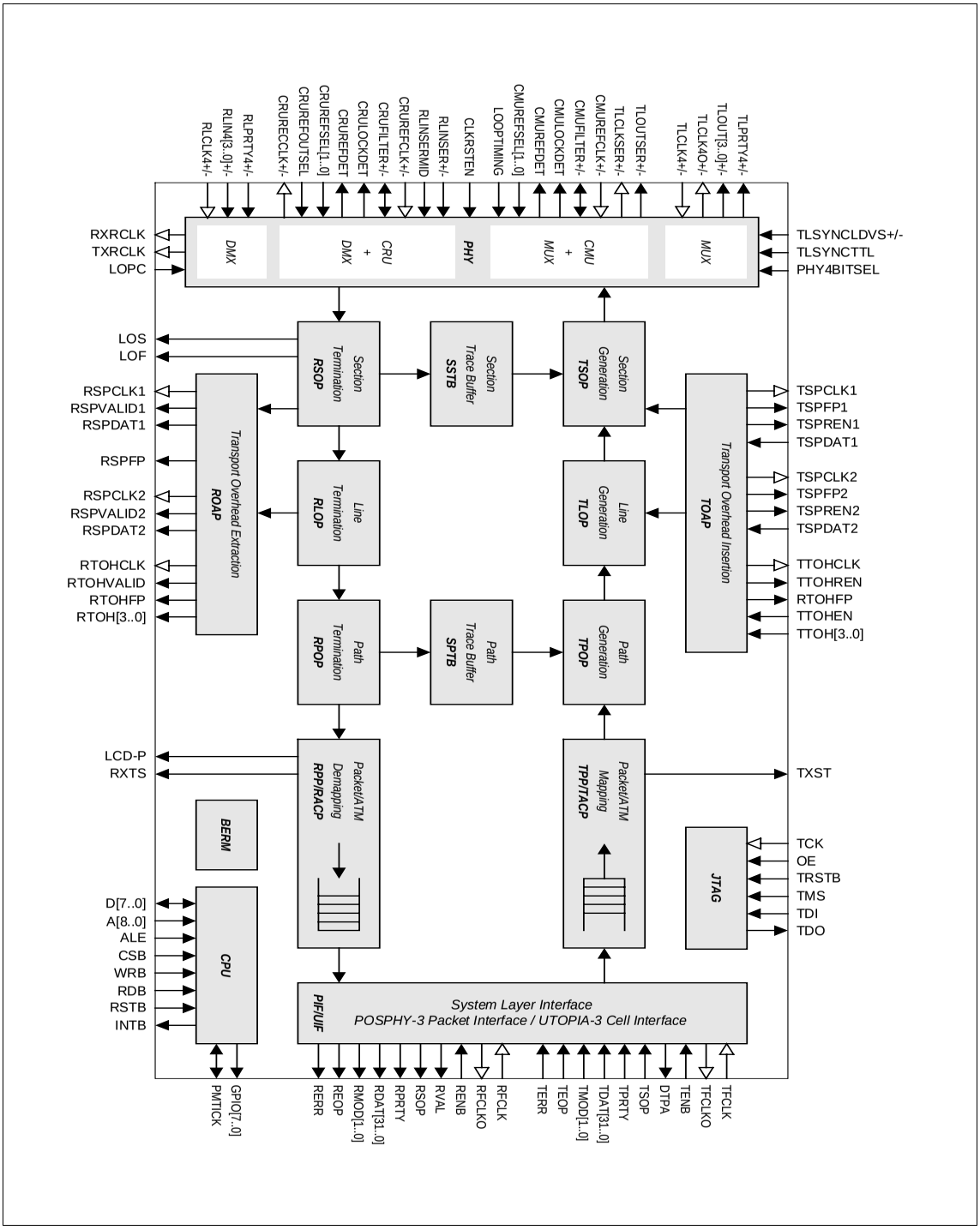


Figure 1.1. VSC9142 Functional Block Diagram

1.2 VSC9142 Functional Blocks

The VSC9142 is partitioned into the functional blocks shown in Figure 1.1. The bullets below define the essential function of the data transmit and receive blocks. The sections following the bullets summarize the key features of each functional block in Figure 1.1.

- Physical Line Side Interface (PHY) is the interface between the line side and the VSC9142's SONET/SDH overhead and payload processing. The PHY performs clock and data recovery on received data in addition to deserialization. Serialization and clock multiplication is performed on the transmit data. An optional 4-bit interface for STS-192 use is provided in both the transmit and receive direction.

- Section overhead processing (RSOP) responsibilities in the receive (Rx) flow are frame synchronization and descrambling, plus Section alarms and error monitoring. Transmit (Tx) Section overhead processing (TSOP) operations include frame pattern generation with scrambling, and alarm and Section error insertion.

- The Rx flow portion of the Line overhead processing blocks (RLOP/TLOP) handles Line alarm and error monitoring, automatic protection switching, and synchronization status extraction on the Rx flow. Line overhead processing in the Tx flow include Line alarm insertion, error code insertion, automatic protection switching insertion, and synchronization status insertion.

- Rx flow functions in the Path overhead processing blocks (RPOP/TPOP) include pointer interpretation, Path overhead extraction, and monitoring Path alarms. Tx functions for Path overhead processing are pointer generation, error code (B3) insertion, and status backreporting.

- Packet processing is handled by the RPP/TPP blocks (which also contain the RACP/TACP ATM Cell processing blocks, described next). Packet processing includes PPP/HDLC framing and deframing when the VSC9142 is used in Packet-over-SONET/SDH applications. In the Rx path, this includes HDLC frame boundary alignment, decompression of the PPP Octet-Stuffing procedure, detection of short/long packets, FCS checking, and abort sequence detection. Tx functions are PPP packet encapsulation, PPP octet stuffing, generation of HDLC frames, FCS generation, and scrambling. Various diagnostic and performance monitoring features are also provided in these blocks.

- The ATM cell processing blocks (RACP/TACP) perform ATM cell mapping and demapping for ATM-over-SONET/SDH applications. Rx flow functions include ATM cell boundary alignment (cell delineation), idle/unassigned cell filtering, single bit error correction in cell headers, cell payload descrambling, and performance monitoring. Tx flow functions include HEC field generation for ATM cell headers, cell rate adaptation using idle/unassigned cells, and cell payload scrambling.

- The receive/transmit FIFOs (Rx FIFO/Tx FIFO) provide clock domain synchronization and buffering between the SONET/SDH transmission path and the drop-side ATM/packet FIFO interface. FIFO overrun/underrun conditions are detected, and programmable full/empty flags are provided.

- The overhead access port (ROAP/TOAP) blocks enable extraction and insertion of transport overhead octets for SONET/SDH frames.

- The SONET/SDH Section/Path trace buffers (SSTB/SPTB) handle extraction and insertion of trace messages. The Rx side extracts and compares received messages with expected messages and performs persistency checks. The Tx side inserts trace messages.

- The POS-PHY Level 3 Packet Interface/UTOPIA-3 like ATM Cell Interface (PIF/UIF) block provides a physical drop-side user-interface between a packet/ATM network and the SONET/SDH flows in the VSC9142 device. The primary external interfaces for the PIF/UIF block are two 32-bit busses, one to transmit and one to receive data.

- The bit error rate monitor (BERM) block provides overall performance monitoring for the link, measuring BERs down to 10^{-10}.

- The JTAG test access port (JTAG TAP) enables external boundary scan compliant with the IEEE 1149.1 Standard Test Port and Boundary Scan Architecture standard.

- This generic microprocessor interface (CPU) facilitates all device configuration, status and performance information extraction, and test-mode operations.

1.2.1 Transmit Path Processing

Physical Line Side Interface (PHY)

- Selectable reference frequency for the clock multiplication unit

- Reference and lock detect signals for the clock multiplication unit

- Looptiming ability to lock the transmit clock to the recovered line clock
- Facility loopback capability for special application or test purposes
- 4-bit interface with programmable parity bit (even or odd) for outgoing data, and synchronization pin (TLSYNC) for STS-192/STM-64 applications
- Programmable reference clock output (8kHz, 19MHz, 38MHz, or 78MHz) derived from the transmit line side clock, either the clock multiplier clock the 4-bit transmit line clock

SONET/SDH Section Overhead Generation (TSOP)

- Supports insertion of Line Alarm Indication Signal (AIS-L; i.e., all "1s" in the line-side transmit data stream except for Section overhead). AIS-L insertion can be automatically triggered by activity on the special purpose serial interfaces.
- Computes and inserts the Section BIP-8 code in B1 octets of transmitted frames (insertion of B1 errors can be forced for diagnostics purposes)
- Generates and inserts A1 A2 framing octets in transmitted frames (insertion of framing bit errors can be forced for diagnostics purposes)
- J0 octet supports both SONET and SDH formats, or can be programmed to a fixed value compatible with older equipment using C1 identification octets
- Z0 growth octets supports both SONET and SDH formats, or can be programmed to carry C1 identification octets for compatibility with older equipment
- Optionally scrambles the outgoing data stream with a frame-synchronous scrambler of a sequence length of 127 and a generating polynomial of $1 + x^6 + x^7$
- Supports forced insertion of all "0s" (LOS) in the outgoing data stream after scrambling for diagnostic purposes
- Enables octets present at the special purpose input ports in the TOAP block to be inserted into the D1-D3, E1, F1 and J0 octets of the outgoing Section overhead
- Enables all reserved Section overhead octets (i.e., for future national or international standards) to be written as 0x00

SONET/SDH Section/Path Trace Buffers (SSTB/SPTB) Transmit Functions

- Store, frame, and insert programmable trace messages into transmit stream
- Supports three different Section/Path trace message formats (transported in the J0 octet) in both the transmit and receive directions (i.e., single octet SONET messages, 16-octet SDH messages, or 64-octet SONET CLLI messages)
- Checks received Section/Path trace messages for persistency and issues a "mismatch" alarm if required

SONET/SDH Line Overhead Generation (TLOP)

- Generates and inserts programmable K1 K2 Automatic Protection Switching (APS) octets in the outgoing data stream
- Generates and inserts Line Remote Defect Indication (RDI-L) in the outgoing data stream on detection of LOS, LOF, or AIS-L alarms in the receive stream
- Calculates and inserts Line BIP-384 code in outgoing B2 octets of the current frame (insertion of B2 errors can be forced for diagnostics purposes)
- Enables the number of Line BIP-384 errors detected in the Receive Line Overhead Processor (RLOP) to be backreported via Line REI in the M1 octet (up to 255 errors can be backreported per frame in individual mode)
- Supports individual- and block-mode backreporting via the M1 octet (insertion of M1 errors can be forced for diagnostics purposes)
- Provides for insertion of a programmable Synchronization Status (SS) value in the S1 octet
- Inserts octets present at the special purpose ports of the Transmit Overhead Access Port (TOAP) into the D4-D12, E2, S1, K1 and K2 octets of the outgoing Line overhead
- Enables all reserved Line overhead octets (i.e., for future national or international standards) to be overwritten as 0x00
- H1, H2, and H3 octets from the Transmit Overhead Access Port (TOAP) can be inserted into the H1, H2, and H3 overhead octets, or applied as an error mask to the H1, H2, and H3 overhead octets

SONET/SDH Overhead Insertion Port (TOAP)

- Provides two identical, independent special purpose ports to enable insertion of special purpose octets and certain SONET/SDH alarms specific to Automatic Protection Switching (APS) into the transport overhead

- Enables selective insertion of acquired transport overhead octets into corresponding transmitted overhead octets of the SONET/SDH frame via the nibble input port TTOH[3..0]

SONET/SDH Path Overhead Generation (TPOP)

- H1 H2 pointer octets can be programmed to support SONET or SDH

- Pointer diagnostic functions are provided, and the remaining 47 H1 H2 octets are programmable

- Path BIP-8 is computed and inserted in the B3 octet. B3 errors can be inserted for diagnostics.

- The number of Path BIP-8 errors detected in the Receive Path Overhead Processor (RPOP) is backreported as Path Remote Error Indications (REI-P) for insertion in G1 octets (supports both individual- and block-mode accumulation).

- Path Remote Defect Indications (RDI-P) insertion is optionally enabled or disabled for the following alarms: LOS, LOF, AIS-L, AIS-P, LOP-P, TIM-P, UNEQ-P, LCD-P and PLM-P. Current and previous RDI-P formats are supported.

- Programmable Path Signal Label (C2) and Path trace (J1) octets

- Programmable F2, H4, Z3, Z4, and Z5 octets

Packet Processing and Monitoring (TPP)

- Programmable insertion of HDLC Flag Sequence octet

- Programmable value for minimum Flag Sequence octets to separate HDLC frames

- HDLC Address-Control-compression insertion control mechanism

- Programmable Address field insertion after start of Flag Sequence

- Programmable Control field insertion after start of Address field

- The Frame Check Sequence (FCS) can be generated using two methods:
  - Using the 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$
  - Using the 32-bit, CRC-32 generating polynomial
    $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

- Octet Stuffing, or "escaping", can be applied after FCS generation and partial scrambling, if enabled. The Control Escape octet and Octet Stuffing Mask are programmable. The Asyc-Control-Character-Map (ACCM) can accommodate a maximum of five octet values, and each value can be individually enabled or disabled.

- Transmitted data is scrambled using a self-synchronizing scrambler (SSS) polynomial $1 + x^{43}$. Full and/or partial scrambling can be independently enabled or disabled.

- The inserted PPP Protocol field can be extracted from the Tx FIFO or internally-generated with a programmable size and value.

- The Tx FIFO is programmable over a range from 1 to 4095 words, or up to 16380 octets of data. All valid packet octets stored in the Tx FIFO are read out and mapped to PPP Protocol/Information fields of generated PPP/HDLC frames.

- Supports packet- and word-based Tx PIF/UIF transfer modes

- The TXF_ERR signal enables errors to be inserted into the FCS, or the transmitted HDLC frame to be aborted.

- Transmitted Address, Control or Protocol fields can be XORed with a programmable mask value via the CPU interface for diagnostic purposes.

- 32-bit performance monitoring counters can be programmed to observe:
  - Octets read from the Tx FIFO
  - Good HDLC frames transmitted (i.e., non-aborted, non-FCS errored)
  - Aborted HDLC frames transmitted
  - FCS Errored HDLC frames transmitted
  - Long or short packets read from the Tx FIFO
  - Empty HDLC frames transmitted
  - Octets before or after octet-stuffing (excluding Abort sequences)

ATM Cell Mapping (TACP)

- ATM cells are mapped to SONET STS-48c SPEs or SDH STM-16 AU-4-16cs. Programmable idle/unassigned cells are inserted into the cell stream.
- Optional scrambling of the 48-octet information field using the self-synchronizing scrambling polynomial $1 + x^{43}$
- HEC generator carries out CRC-8 calculations over the first four header octets using the generating polynomial $1 + x + x^2 + x^8$, and the coset polynomial $1 + x^2 + x^4 + x^6$ can be added to the result. The HEC can then be optionally inserted into the fifth octet of cell headers as they are read from the Tx FIFO.
- Tx FIFO accommodates up to eight ATM cells

UTOPIA-Level 3/POS-PHY-3 Cell/Packet Transmit Interface (PIF/UIF)

- Standards-compliant POS (packet over SONET/SDH) interface
- Programmable parity bit (even or odd) checking
- Interface supports both word- and packet/cell-level transfer modes
- Single PHY UTOPIA-3 like interface for ATM applications
- Programmable "decode-response time" for flow control flags
- DTPA signal output to indicate "level" of the Tx FIFO word count based on programmable high and low "water marks"
- Tx FIFO reset or flush via the CPU interface

1.2.2 Receive Path Processing

Physical Line Side Interface (PHY)

- Selectable reference frequency for the clock recovery unit
- Reference and lock detect signals for the clock recovery unit
- Equipment loopback capability for special application or test purposes
- 4-bit interface with programmable parity bit (even or odd) checking

- Programmable reference clock output (8kHz, 19MHz, 38MHz, or 78MHz) derived from the receive line side clock, either the recovered serial line clock or the 4-bit receive clock

- Dedicated input for Loss of Optical Carrier (LOPC) alarm monitoring

SONET/SDH Section Overhead Termination (RSOP)

- Frame alignment via A1/A2 frame pattern recognition in incoming data stream

- Supports 12-, 24-, or 48-bit A1/A2 framing patterns

- Out Of Frame (OOF) and Loss Of Frame (LOF) alarm condition detection

- Issues alarms for Loss Of Frame (LOF) condition based on programmable monitoring of OOF condition

- Optionally descrambles the incoming data stream with a generating polynomial of $1 + x^6 + x^7$ and a sequence length of 127

- Detects and accumulates Section BIP-8 errors from the B1 octet of received frames (supports both individual- and block-mode accumulation)

- Monitors for absence of transitions or "all-zero" pattern in the incoming data stream prior to descrambling

- Provides programmable detection and termination criteria for Loss Of Signal (LOS) condition

- Supports insertion of Line Alarm Indication Signal (AIS-L; i.e., all "1s" in the line side receive data stream except for Section overhead). AIS-L insertion can be automatically triggered on detection of LOS, LOF, or Loss of Optical Carrier (LOPC) conditions.

- Enables extraction of the entire Section overhead via the Receive Overhead Access Port (ROAP)

- Extracts J0, E1, F1, and D1-D3 octets from Section overhead, and subsequently inserts them into octets on special purpose output ports in the ROAP block

SONET/SDH Section/Path Trace Buffers (SSTB/SPTB) Receive Functions

- Checks received Section trace messages for persistency and issues a "mismatch" alarm if required

- Supports three different Section trace message formats (transported in the J0 octet) in both the transmit and receive directions (i.e., single octet SONET messages, 16-octet SDH messages, or 64-octet SONET CLLI messages)

SONET/SDH Line Overhead Termination (RLOP)

- Extracts and filters Line Remote Defect Indication (RDI-L) and Line Alarm Indication Signal (AIS-L) alarms from received K2 octets (supports programmable filtering constraints)

- Detects and accumulates Line BIP-384 errors from received B2 octets (supports both individual- and block-mode accumulation)

- Detects and accumulates Line Remote Error Indications (REI-L) from received M1 octets (supports both individual- and block-mode accumulation)

- Extracts and filters Synchronization Status (SS) from received S1 octets (supports "unstable/mismatch" alarms and programmable filtering constraints)

- Extracts and filters K1/K2 Automatic Protection Switching (APS) octets (supports "unstable" alarms and programmable filtering constraints)

- Optionally extracts Line overhead via the ports in the ROAP block

- Extracts D4-D12, S1, E2, and K1-K2 octets from Line overhead, and subsequently inserts them into octets on the special purpose output ports in the ROAP block

SONET/SDH Overhead Extraction Port (ROAP)

- Provides two identical, independent special purpose ports to enable extraction of special purpose octets and certain SONET/SDH alarms specific to Automatic Protection Switching (APS) from the transport overhead

- Outputs the RSPFP frame pulse signal, as well as clocks and control signals associated with each output stream.

- Enables acquisition of the entire Section/Line transport overhead via the nibble output port RTOH[3..0]

SONET/SDH Path Overhead Termination (RPOP)

- Extracts and interprets H1 H2 pointer octets which are used to define the SONET SPE (synchronous payload envelope) or SDH VC (virtual container) according to ANSI T1.105 and ITU-T G.707 recommendations
- Monitors H1 H2 octets for concatenation indication (CI)
- Provides diagnostic pointer functions
- Supports Path Alarm Indication Signal (AIS-P) and Loss of Pointer (LOP-P) alarm declaration
- Detects and accumulates Path BIP-8 errors from received B3 octets (supports both individual- and block-mode accumulation)
- Detects and accumulates Path Remote Error Indications (REI-P) from received G1 octets (supports both individual- and block-mode accumulation). Up to 64000 individual errors can be detected per second.
- Programmable detection of Path Remote Defect Indications (RDI-P) from received G1 octets
- Programmable detection and alarm generation for Path Signal Label from received C2 octets

Packet Processing and Monitoring (RPP)

- Programmable identification of the HDLC Flag Sequence
- Programmable detection and discard of invalid frames
- Programmable expected Control Escape and Octet Destuffing Mask
- Programmable expected Address and Control fields
- Programmable Protocol field declaration and processing
- Detects Abort Sequence in incoming HDLC frames
- Verifies the received Frame Check Sequence (FCS) field
- The Frame Check Sequence (FCS) can be generated using two methods:
  - Using the 16-bit, CRC-CCITT generating polynomial $1 + x^5 + x^{12} + x^{16}$

- Using the 32-bit, CRC-32 generating polynomial
  $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

- Descrambles received data using self-synchronizing scrambler (SSS) polynomial $1 + x^{43}$ (full and/or partial descrambling can be independently enabled or disabled)
- Programmable long- and short-packet checking
- Programmable support for Self Describing Padding
- Optional storage of PPP Protocol field in Rx FIFO
- 4096 word Rx FIFO accommodates up to 16380 PPP Protocol/Information field octets
- Two different programmable definitions for received "errored" HDLC frames
- Programmable packet discard and error marking filter.
- 32-bit performance monitoring counters to observe:
  - Aborted HDLC frames received
  - FCS errored HDLC frames received
  - Empty HDLC frames received
  - Received HDLC frames with Address-Control-compression found
  - Long or short packets received
  - Invalid frames received
  - Octets received before or after octet destuffing
  - Frames received, excluding invalid frames
  - Packets discarded by label filtering
  - Error-marked packets from label filtering
  - Packets stored in the Rx FIFO
  - Error-marked packets stored in the Rx FIFO
  - Packet octets stored in the Rx FIFO
  - PPP padding octets received
- SPE Transparent Mode passes the SONET STS-48c SPE or SDH STM-16 AU-4-16c payload directly to the Rx FIFO without processing

ATM Cell Demapping (RACP)

- Cell Delineation is completed using a shortened cyclic code with the generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^8$ can be added to the calculated HEC check bits before comparison.
- Supports single-bit header error correction, as well as programmable cell dropping during single or multiple error detection
- Optional descrambling of the 48-octet information field using the self-synchronizing descrambler polynomial $1 + x^{43}$
- Cell filtering via programmable GFC, PTI, or CLP fields
- Detection and monitoring of correctable and uncorrectable HEC errors, as well as the number of cells written to the Rx FIFO
- Rx FIFO accommodates up to eight ATM cells

UTOPIA-Level 3/POS-PHY-3 Cell/Packet Receive Interface (PIF/UIF)

- Standards-compliant POS (packet over SONET/SDH) interface
- Programmable parity bit (even or odd)
- Interface supports both word- and cell/packet-level transfer modes
- Single PHY UTOPIA-3 like interface for ATM applications
- Rx FIFO reset or flush via the CPU interface

1.2.3 Microprocessor Interface (CPU)

- Read/write support for all configuration bits, and access regardless of device clock source status (except reset state)
- Configuration bits include selection bits, interrupt masking bits, and programmable counter/control values
- Provides eight programmable General Purpose Input/Output (GPIO) ports for monitoring and controlling external signals
- All GPIOs support bistable interrupts when configured as input ports

- Clock activity monitors are available on all input clocks

1.2.4 JTAG Test Access Port (JTAG TAP)

The JTAG test access port (TAP) enables external boundary scan to be performed in compliance with the IEEE 1149.1 Standard Test Port and Boundary Scan Architecture Standard

1.2.5 Bit Error Rate Monitor (BERM)

- Bit error rate monitoring based on Line BIP (B2 octet) error codes (measurement precision down to 10^{-10})
- Four independent BER monitors with individual programmable accumulation periods, saturation thresholds (i.e., maximum number of errors that can be accumulated per frame), and alarm thresholds
- BER Signal Degrade (BER-SD) alarm is provided for BER monitors 1 and 2
- BER Signal Fail (BER-SF) alarm is provided for BER monitors 3 and 4

1.3 Applications

The VSC9142 facilitates the development of highly-integrated, single-board STS-48/STM-16 with concatenated payload to packet/ATM interface line cards. In the POS (packet over SONET) mode, the device can be used to interconnect IP/PPP/HDLC equipment to public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used to interconnect ATM switches. The VSC9142 is an ideal platform for developing highly-integrated switches, routers, hubs; WAN equipment; and test systems.

1.3.1 Typical System Utilization

Since the VSC9142 contains all necessary physical interface blocks, the device can mate directly to the Optical transceiver. Figure 1.2 shows a top-level view of a typical ATM or packet over SONET application for the VSC9142.

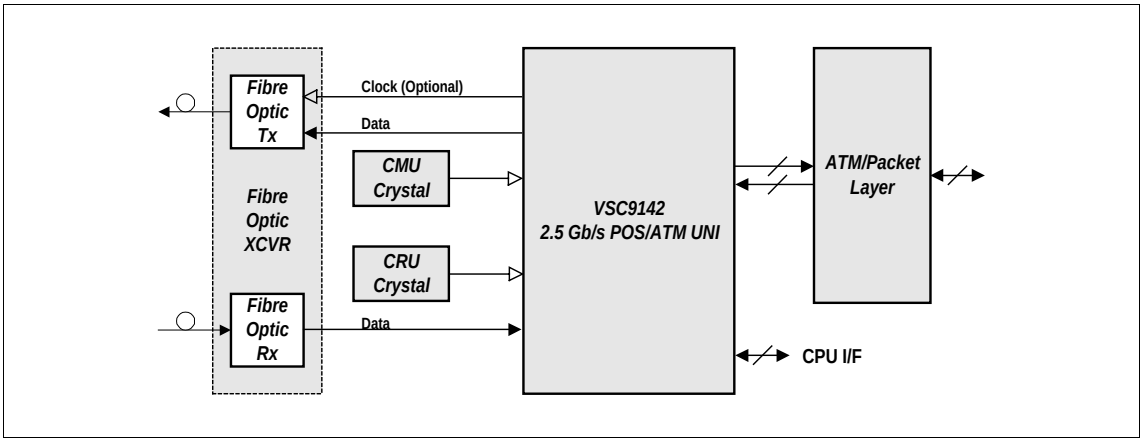


Figure 1.2. Typical ATM- or packet-to-SONET Interface Application

1.3.2 Loopback Configurations

System development and test are simplified via five internal loopback modes. These include equipment, facility, section, line, and packet/UTOPIA loops (see Figure 1.3). The VSC9142's facility loopback mode enables the device to be used for regeneration applications. In this capacity, connections to the device's drop side are not required. In equipment and drop loop modes, external clock sources are muxed internally.

- Facility Loopback connects the PHY block receive input (post demultiplexing) back to the PHY transmit output. The receive and transmit core clocks must be frequency locked via looptiming or register configuration.

- Equipment Loopback connects the data path output from the TSOP block (transmit direction) back to the input of the RSOP block (receive direction). The receive core clock must be set equal to the transmit core clock, via looptiming or register configuration. Likewise RFCLK and TFCLK are required to be frequency locked.

- Section Loopback connects the data path output from the RSOP block to the input of the TSOP block. The receive and transmit core clocks must be frequency locked.

- Line Loopback connects the data path output from the RLOP block to the input of the TLOP block. The receive and transmit core clocks must be frequency locked.

- Packet/Cell Loopback connects the output from the Tx FIFO in the TPP/TAPC block to the input of the Rx FIFO in the RPP/RAPC block. The receive and transmit core clocks are required to be frequency locked.

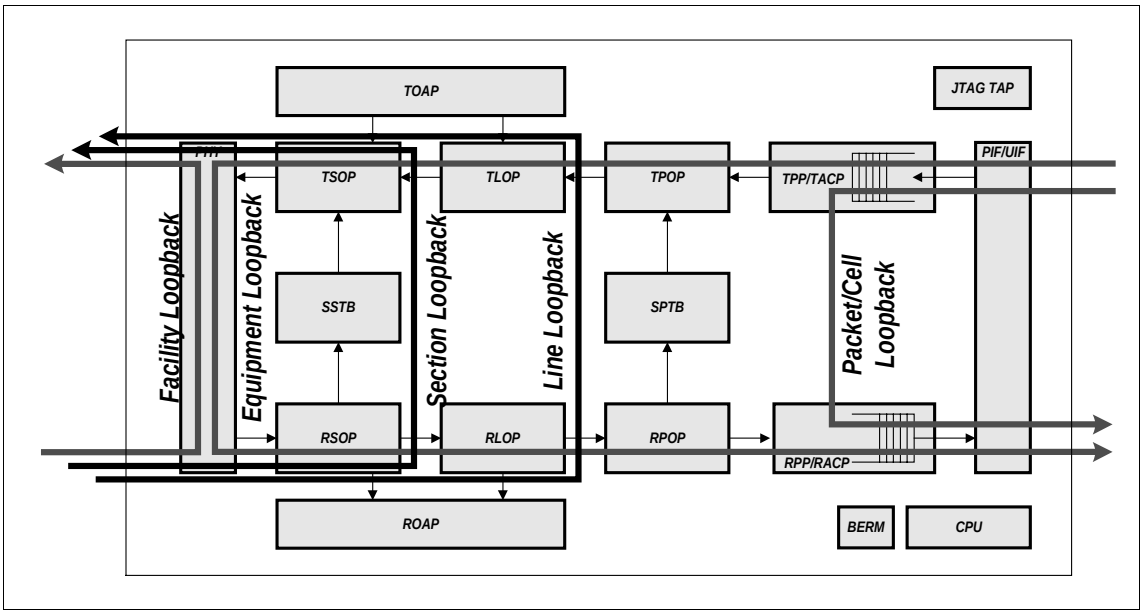


Figure 1.3. VSC9142 Internal Loopback Paths

1.4 Pin Definitions

Figure 1.4 identifies the external ball pads in the 320-pin BGA package. Table 1.1 provides a detailed functional description of all hardware signal pins in the device.

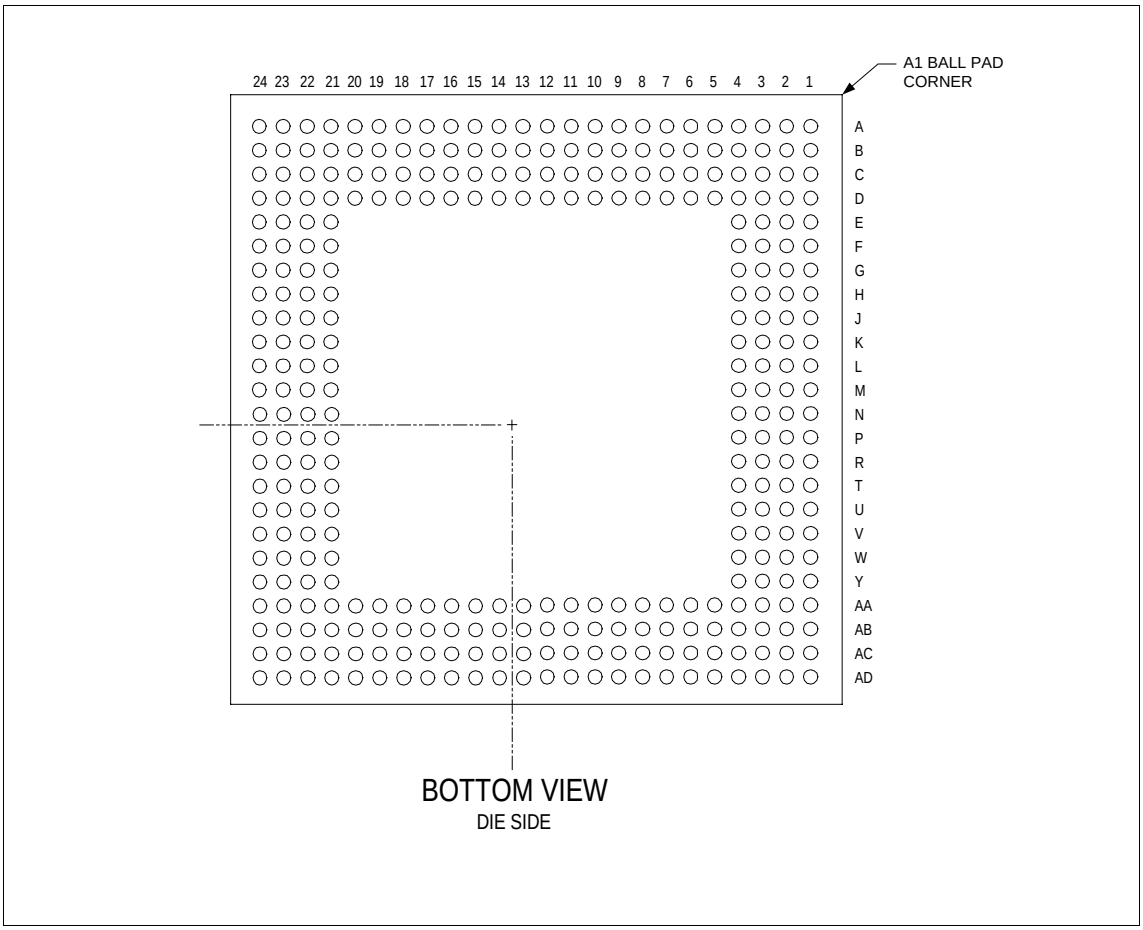


Figure 1.4. VSC9142 320 BGA Ball Pad Identification

Table 1.1. Hardware Signal Definitions (1 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Physical Interface (PHY) Signals	RLINSER- RLINSER+	F24 G24	I	PECL	Serial Line Receive Data	Serial line data input.
	RLIN4[0]- RLIN4[0]+ RLIN4[1]- RLIN4[1]+ RLIN4[2]- RLIN4[2]+ RLIN4[3]- RLIN4[3]+	D22 E21 E22 D23 F21 F22 E23 F23	I	LVDS	Parallel Line Receive Data	This is the parallel line-side receive data bus for the incoming STS-48c/STM-16 AU-4-16c data stream. RLIN4[3] is the most significant and first bit arriving bit on the serial data stream. RLIN4[3..0] is sampled on the rising edge of RLCLK4+. RLIN4[3..0]+ are the true signal values.
	RLPRTY4- RLPRTY4+	C22 C23	I	LVDS	Parallel Line Receive Parity	This is a programmable (even/odd) parity bit for parallel line receive data RLIN4[3..0]. RLPRTY4 is sampled on the rising edge of RLCLK4+. RLPRTY4+ is the true signal value.
	RLCLK4- RLCLK4+	D24 C24	I	LVDS	Parallel Line Receive Clock	This is the reference clock input for the parallel line-receive data carried in RLIN4[3..0]+/-. The nominal frequency is 622.08 MHz for STS-48c/STM-16 AU-4-16c operation. RLCLK4+ is the true signal value.
	RLINSERMID	H23	I	N/A	Serial Line Receive Data Center Tap	RLINSER+/- has a 100 ohms on-chip resistor termination which has a center tap between the two 50 ohm resistors. The center tap can be used to bias the centerpoint for single ended applications or decoupled to GND for differential applications.
	CRUREFCLK- CRUREFCLK+	J21 J22	I	PECL	CRU Reference Clock	This input is the reference clock used within phase locked loop in the clock recovery unit.
	CRUREFDET	AD15	O	TTL	CRU Reference Clock Detect	This output indicates the presense of clock transistions on CRUREFCLK+/-. The signal is active high.
	CRULOCKDET	AC15	O	TTL	CRU Lock Detect	This output indicatest the lock status of the PLL within the CRU with respect to CRUREFCLK+/-. The signal is active high.
	CRUREFSEL1 CRUREFSEL0	AB15 AA15	I	TTL	CRU Reference Clock Select	These inputs select which frequency is to be expected on CRUREFCLK+/-. The binary combination of the two pins are described below (CRUREFSEL0 noted first). 00 78 MHz 01 155 MHz 10 311 MHz
	CRURECCLK- CRURECCLK+	K24 J24	O	PECL	CRU Recovered Clock	This reference clock output is derived from the 2.5 Gb/s reference clock divided down according to CRUREFSEL[1..0].
	CRUFILTER- CRUFILTER+	L23 K22	I	N/A	CRU Loop Filter	These inputs are brought off-chip to connect to a capacitor which completes the CRU loop filter. CRUFILTER+ should be connected to one side of a 0.1uF capacitor while CRUFILTER- should be connected to the other side of the capacitor.
	CRUREFOUTSEL	AD16	I	TTL	CRURECCLK Output Selector	This input selects the clock to be output on pins CRURECCLK+/-. A high level selects a looped version of the reference clock, while a low level selects the divided version of the recovered clock.

Table 1.1 Hardware Signal Definitions (2 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Physical Interface (PHY) Signals (cont.)	TLOUTSER- TLOUTSER+	N24 M24	O	PECL	Serial Line Transmit Data	Serial line data output.
	TLCLKSER- TLCLKSER+	R24 P24	O	PECL	Serial Line Transmit Clock	Serial line clock output
	TLOUT4[0]- TLOUT4[0]+ TLOUT4[1]- TLOUT4[1]+ TLOUT4[2]- TLOUT4[2]+ TLOUT4[3]- TLOUT4[3]+	V23 V22 V24 W23 Y22 W21 AA24 AA23	O	LVDS	Parallel Line Transmit Data	This is the parallel line-side transmit data bus for the outgoing STS-48c/STM-16 AU-4-16c data stream. TLOUT4[3] is the most significant and first transmitted bit in the serial data stream. TLOUT4[3..0] is latched out the rising edge of TLCLK4+, but is centered about TLCLK4O-. TLOUT[3..0]+ are the true signal values.
	TLPRTY4- TLPRTY4+	U23 U22	O	LVDS	Parallel Line Transmit Parity	This is a programmable (even/odd) parity bit for parallel line transmit data TLOUT4[3..0]. TLPRTY4 is latched out on the rising edge of TLCLK4+, but is centered about TLCLK4O-. TLPRTY4+ is the true signal value.
	TLCLK4- TLCLK4+	T24 U24	I	LVDS	Parallel Line Transmit Clock	This is the reference clock input for the parallel line-transmit data carried in TLOUT4[3..0]+/-. The nominal frequency is 622.08 MHz for STS-48c/STM-16 AU-4-16c operation. TLCLK4+ is the true signal value.
	TLCLK4O- TLCLK4O+	Y24 W24	O	LVDS	Parallel Line Transmit Clock Out	This output is the looped version of the reference clock input TLCLK4+/-. The nominal frequency is 622.08 MHz for STS-48c/STM-16 AU-4-16c operation. TLCLK4O+ is the true signal value.
	CMUREFCLK- CMUREFCLK+	N23 M23	I	PECL	CMU Reference Clock	This input is the reference clock used for the clock multiplier unit.
	CMUREFDET	AC17	O	TTL	CMU Reference Clock Detect	This output indicates the presense of clock transistions on CMUREFCLK+/-. The signal is active high.
	CMULOCKDET	AC16	O	TTL	CMU Lock Detect	This output indicatest the lock status of the PLL within the CMU with respect to CMUREFCLK+/-. The signal is active high.
	CMUREFSEL1 CMUREFSEL0	AB16 AA16	I	TTL	CMU Reference Clock Select	These inputs select which frequency is to be expected on CMUREFCLK+/-. The binary combination of the two pins are described below (CMUREFSEL0 noted first). 00 78 MHz 01 155 MHz 10 311 MHz
	CMUFILTER- CMUFILTER+	L22 L21	I	N/A	CMU Loop Filter	These inputs are brought off-chip to connect to a capacitor which completes the CMU loop filter. CMUFILTER+ should be connected to one side of a 0.1uF capacitor while CMUFILTER- should be connected to the other side of the capacitor.

Table 1.1 Hardware Signal Definitions (3 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Physical Interface (PHY) Signals (cont.)	CLKRSTEN	AC12	I	TTL	Clock Reset Enable	Asserting CLKRSTEN halts all primary clock outputs (TXRCLK, RXRCLK, RSPCLK1, RSPCLK2, RTOHCLK, TSPCLK1, TSPCLK2, and TTOHCLK) during master reset. If deasserted, all primary clock outputs run normally during master reset.
	LOOPTIMING	AD18	I	TTL	Looptime Enable	This input enables looptiming which forces the CMU and subsequent Tx clocks to be referenced to the recovered line clock. This signal is active high although the associated register can override the pin.
	LOPC	AC13	I	TTL	Loss of Optical Carrier	This input is used to monitor the optical carrier signal status, and detected changes which can be used to generate interrupts. This enables the optical signal to be monitored via the device CPU interface. When LOPC is asserted, the receive processor is optionally clocked by the transmit clock (derived from TLCLK4+/- or the CMU clock).
	PHY4BITSEL	AB14	I	TTL	4-Bit Physical Interface Select	This input selects the 4 bit interface and disables the CRU and CMU. This input is active high.
	TLSYNCLVDS- TLSYNCLVDS+	T22 T21	I	LVDS	Transmit Synchronization	This is the LVDS input for the synchronous reset signal for the line-side transmit processor. (NOTE: TLSYNCLVDS/ TLSYNCTTL is intended for use in STS-192/STM-64 applications only.)
	TLSYNCTTL	AB23	I	TTL	Transmit Synchronization	This is the TTL input for the synchronous reset signal for the line-side transmit processor. (NOTE: TLSYNCLVDS/ TLSYNCTTL is intended for use in STS-192/STM-64 applications only.)
	RXRCLK	AD12	O	TTL	Receive Reference Clock	This reference clock output is derived from the serial or parallel receive line clock and can be programmed to operate at 78MHz, 38MHz, 19MHz, or 8kHz frequencies.
	TXRCLK	B21	O	TTL	Line Transmit Reference Clock	This reference clock output is derived from the serial or parallel transmit line clock and can be programmed to operate at 78MHz, 38MHz, 19MHz, or 8kHz frequencies.

Table 1.1 Hardware Signal Definitions (4 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Drop Side (PIF/UIF) Transmit Signals	TDAT/TUDATA[0]	J3	I	TTL	Transmit Packet Data Bus (TDAT*x*) *or* UTOPIA Transmit Cell Data Bus (TUDATA*x*)	***POS Mode:*** This 32-bit data bus is used to drive four-octet true data from the Packet to PHY layer. TDAT[31] is the MSB. Packets are aligned to the 32-bit TDAT*x* boundary. ***ATM Mode:*** This 32-bit data bus is used to drive four-octet true data from the ATM to PHY layer. TUDATA[31] is the MSB.
	TDAT/TUDATA[1]	J4				
	TDAT/TUDATA[2]	H3				
	TDAT/TUDATA[3]	G1				
	TDAT/TUDATA[4]	G2				
	TDAT/TUDATA[5]	G3				
	TDAT/TUDATA[6]	F1				
	TDAT/TUDATA[7]	F2				
	TDAT/TUDATA[8]	F3				
	TDAT/TUDATA[9]	E2				
	TDAT/TUDATA[10]	E3				
	TDAT/TUDATA[11]	F4				
	TDAT/TUDATA[12]	D1				
	TDAT/TUDATA[13]	D2				
	TDAT/TUDATA[14]	D3				
	TDAT/TUDATA[15]	E4				
	TDAT/TUDATA[16]	C1				
	TDAT/TUDATA[17]	C2				
	TDAT/TUDATA[18]	D5				
	TDAT/TUDATA[19]	B3				
	TDAT/TUDATA[20]	A3				
	TDAT/TUDATA[21]	C4				
	TDAT/TUDATA[22]	B4				
	TDAT/TUDATA[23]	D6				
	TDAT/TUDATA[24]	C5				
	TDAT/TUDATA[25]	A4				
	TDAT/TUDATA[26]	C6				
	TDAT/TUDATA[27]	B5				
	TDAT/TUDATA[28]	B6				
	TDAT/TUDATA[29]	C7				
	TDAT/TUDATA[30]	A6				
	TDAT/TUDATA[31]	D9				

Table 1.1 Hardware Signal Definitions (5 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Drop Side (PIF/UIF) Transmit Signals (cont.)	***POS Mode:*** TPRTY ***ATM Mode:*** TUPRTY	C8	I	TTL	Transmit Bus Parity	***POS Mode:*** TRPRTY is the odd/even (programmable, default odd) parity bit over TDAT[31..0]. The signal is only valid when asserted simultaneously with TENB. ***ATM Mode:*** TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31..0], driven by the ATM layer. The signal is valid when asserted simultaneously with TUENB*.
	POS Mode: TMOD[1] TMOD[0]	A7 B7	I	TTL	Transmit Word Modulo	***POS Mode only:*** These inputs are used to qualify TDAT*x* data octets. The state of TMOD[1,0] defines which of the four TDAT octets contain valid data when both TEOP and TENB are asserted. Non-EOP words always contain four valid TDAT octets.
	POS Mode: TSOP ***ATM Mode:*** TUSOC	C9	I	TTL	Transmit Start of Packet *or* UTOPIA Transmit Start of Cell	***POS Mode:*** TSOP is asserted (active high) by the Packet layer to indicate that TDAT*x* contains the first valid octet of a new packet. The signal is valid when asserted simultaneously with TENB. The packet interface can be operated without using this signal. ***ATM Mode:*** TUSOC is asserted (active high) by the ATM layer to indicate that TUDATA*x* contains the first valid octet of the cell. The signal is only valid when asserted simultaneously with TUENB*.
	POS Mode: TEOP	D10	I	TTL	Transmit End of Packet	***POS Mode only:*** TEOP is asserted (active high) by the Packet layer to indicate that TDAT*x* contains the last valid octet of the packet. Only valid when asserted simultaneously with TENB.
	POS Mode: DTPA ***ATM Mode:*** TUFULL*/ TUCLAV	A9	O	TTL	Transmit Polled-PHY Packet Available *or* Transmit Full/Cell Available	***POS Mode:*** DTPA transitions high when a programmable minimum number of octets are available in the Tx FIFO. Once high, the DTPA indicates that the Tx FIFO is not full. When DTPA transitions low, it optionally indicates that the Tx FIFO is full or near full. ***ATM Mode:*** TUFULL*/TUCLAV is indicates "Full" or "Cell Available" status of UTOPIA transmit interface for flow control. TUFULL* is for word-level flow control; TUCLAV is for cell-level flow control. Polarity is selectable via an internal register bit (i.e., TUFULL* active low/TUCLAV active high, or vice versa).
	POS Mode: TERR	B9	I	TTL	Transmit Error Indicator	***POS Mode only:*** An active TERR flag can be used to force HDLC frame abortion, or insertion of FCS error in the transmitted HDLC/PPP frames. The TERR value is only valid for TEOP-marked words, and is ignored for all other word writes.
	POS Mode: TENB ***ATM Mode:*** TUENB*	C10	I	TTL	Transmit Write Enable	***POS Mode:*** TENB is used by the Packet layer to indicate cycles when TDAT*x* contains valid packet data (active low). ***ATM Mode:*** TUENB* is used by the ATM layer to indicate cycles when TUDATA*x* contains valid cell data (active low).
	POS Mode: TFCLK ***ATM Mode:*** TUCLK	A10	I	TTL	Transmit Write Clock	***POS Mode:*** TFCLK is a reference clock provided by the Packet layer to the PHY layer to synchronize transfers on TDAT*x*. ***ATM Mode:*** TUCLK is a reference clock provided by the ATM layer to the PHY layer to synchronize transfers on TUDATA*x*.
	POS Mode: TFCLKO ***ATM Mode:*** TUCLKO	B10	O	TTL	Transmit Write Clock Looped	***POS Mode:*** TFCLKO is the TFCLK transfer synchronization reference clock from the Packet layer looped out. ***ATM Mode:*** TUCLKO is the TUCLK transfer synchronization reference clock from the ATM layer looped out.

Table 1.1 Hardware Signal Definitions (6 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Drop Side (PIF/UIF) Receive Signals	RDAT/RUDATA[0] RDAT/RUDATA[1] RDAT/RUDATA[2] RDAT/RUDATA[3] RDAT/RUDATA[4] RDAT/RUDATA[5] RDAT/RUDATA[6] RDAT/RUDATA[7] RDAT/RUDATA[8] RDAT/RUDATA[9] RDAT/RUDATA[10] RDAT/RUDATA[11] RDAT/RUDATA[12] RDAT/RUDATA[13] RDAT/RUDATA[14] RDAT/RUDATA[15] RDAT/RUDATA[16] RDAT/RUDATA[17] RDAT/RUDATA[18] RDAT/RUDATA[19] RDAT/RUDATA[20] RDAT/RUDATA[21] RDAT/RUDATA[22] RDAT/RUDATA[23] RDAT/RUDATA[24] RDAT/RUDATA[25] RDAT/RUDATA[26] RDAT/RUDATA[27] RDAT/RUDATA[28] RDAT/RUDATA[29] RDAT/RUDATA[30] RDAT/RUDATA[31]	W1 V3 V2 V1 U3 U2 T4 T3 T2 T1 R4 R3 R2 R1 P3 P2 N1 N4 N3 N2 M3 M4 M2 M1 L2 L3 K1 K2 K3 K4 J1 J2	O	TTL	Recevie Packet Data Bus (RDAT*x*) *or* Receive Cell Data Bus (RUDATA*x*)	***POS Mode:*** This 32-bit data bus is used to drive four-octet true data from the PHY to Packet layer. RDAT[31] is the MSB. Packets are aligned to the 32-bit RDAT*x* boundary. ***ATM Mode:*** This 32-bit data bus is used to drive four-octet true data from the PHY to ATM layer. RUDATA[31] is the MSB.
	POS Mode: RPRTY ***ATM Mode:*** RUPRTY	Y3	O	TTL	Receive Bus Parity	***POS Mode:*** RPRTY is the odd/even (programmable, default odd) parity bit over RDAT[31..0]. ***ATM Mode:*** RUPRTY is the odd/even (programmable, default odd) parity bit over RUDATA[31..0].
	POS Mode: RMOD[1] RMOD[0]	W2 W3	O	TTL	Receive Word Modulo	***POS Mode only:*** These outputs are used to qualify RDAT*x* data octets. The state of RMOD[1,0] defines which of the four RDAT octets contain valid data when REOP is asserted. Non-EOP words always contain four valid RDAT octets.
	POS Mode: RSOP ***ATM Mode:*** RUSOC	AA1	O	TTL	Receive Start of Packet *or* UTOPIA Receive Start of Cell	***POS Mode:*** RSOP is asserted (active high) by the Packet layer to indicate that RDAT*x* contains the first valid octet of a new packet. The packet interface can be operated without using this signal. ***ATM Mode:*** RUSOC is asserted (active high) by the ATM layer to indicate that RUDATA*x* contains the first valid octet of a cell. This signal is used to support multiple PHY configurations.

Table 1.1 Hardware Signal Definitions (7 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Drop Side (PIF/UIF) Receive Signals (cont.)	***POS Mode:*** REOP	AB2	O	TTL	Receive End of Packet	***POS Mode only:*** REOP is asserted (active high) to indicate that RDAT*x* contains the last valid octet of the packet.
	POS Mode: RVAL ***ATM Mode:*** RUEMPTY*/ RUCLAV	AA2	O	TTL	Receive Data Valid *or* Receive Empty/Cell Available	***POS Mode:*** RVAL asserted (active high) indicates that the recevie data signals (RDAT*x*, RSOP, REOP, RMOD, RPRTY, and RERR) are valid. When RAL is low, all receive signals are invalid and must be disregarded. RVAL transitions low when the Rx FIFO is empty or the end of a packet is reached, and data will not be removed from the Rx FIFO while RVAL is low. Once deasserted, RVAL remains so until the current PHY has been deselected. ***ATM Mode:*** RUEMPTY*/RUCLAV indicates "Empty" or "Cell Available" status of the UTOPIA receive interface for flow control. RUEMPTY* is for word-level flow control; RUCLAV is for cell-level flow control. Polarity is selectable via an internal register bit (i.e., RUCLAV active high/RUEMPTY* active low, or vice versa).
	POS Mode: RERR	W4	O	TTL	Receive Error Indicator	***POS Mode only:*** An asserted RERR flag (active high) indicates that the packet contained an error (i.e., abort/FCS error). The RERR flag is only asserted during EOP-marked words.
	POS Mode: RENB ***ATM Mode:*** RUENB*	AA3	I	TTL	Receive Read Enable	***POS Mode:*** RENB is used by the Packet layer to indicate that the RVAL, RSOP, RPRTY, RDAT*x*, RMOD*x*, REOP, and RERR signals will be sampled at the end of the nest cycle (active low). ***ATM Mode:*** RUENB* is used by the ATM layer to indicate that RUDATA, RUSOC, and RPRTY will be sampled at the end of the nest cycle (active low).
	POS Mode: RFCLK ***ATM Mode:*** RUCLK	Y4	I	TTL	Receive FIFO Write Clock *or* Receive Write Clock	***POS Mode:*** RFCLK is a reference clock provided by the Packet layer to the PHY layer to synchronize transfers on RDAT*x*. ***ATM Mode:*** RUCLK is a reference clock provided by the ATM layer to the PHY layer to synchronize transfers on RUDATA*x*.
	POS Mode: RFCLKO ***ATM Mode:*** RUCLKO	AA4	O	TTL	Receive FIFO Write Clock Looped *or* Receive Write Clock Looped	***POS Mode:*** RFCLKO is the RFCLK transfer synchronization reference clock looped out. ***ATM Mode:*** RUCLKO is the RUCLK transfer synchronization reference clock looped out.
Time Stamp Signals	TXTS	AA6	O	TTL	Transmit Time Stamp	TXTS is an active high pulse generated when a cell/packet exits the TPP block. The difference in time between a TXTS pulse and a TSOP/TUSOC pulse can be used to determine transmit FIFO latency.
	RXTS	AC3	O	TTL	Receive Time Stamp	RXTS is an active high pulse generated when a new cell/packet arrives in the RPP block. The difference in time between an RXTS pulse and an RSOP/RUSOC pulse is used to determine receive FIFO latency.
Rx Alarm Signals	LOS	AB5	O	TTL	Loss of Signal	This is a status signal for loss of signal (LOS) detection (active high). LOS status is also indicated by an internal register bit.
	LOF	AA13	O	TTL	Loss of Frame	This is a status signal for loss of frame (LOF) detection (active high). LOF status is also indicated by an internal register bit.
	LCD-P	AB4	O	TTL	Loss of Cell Delineation	This signal is asserted when the cell delineation state machine is not in SYNC state. This alarm indication is also available via internal register access.

Table 1.1 Hardware Signal Definitions (8 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Rx Overhead Transport Access Processor (ROAP) Signals	RSPFP	C18	O	TTL	Receive Special Purpose Frame Pulse	This is a frame reference for special purpose serial output ports RSPDAT*x*. RSPFP outputs a single clock-cycle-wide pulse coincident with the first bit on the serial data streams. Active high, RSPFP transitions occur on falling edges of RSPCLK*x*. *x* =[1,2]
	RSPCLK1	A19	O	TTL	Receive Special Purpose Clock 1	This is a clock reference for RSPDAT1 on special purpose serial output port 1. The frequency is 2.16MHz with a 50% duty cycle (optionally gapped to match the bandwidth of RSPDAT1).
	RSPDAT1	D20	O	TTL	Receive Special Purpose Data 1	This is the data output for receive special purpose serial port 1. RSPDAT1 transitions occur on the falling edge of RSPCLK1.
	RSPVALID1	C20	O	TTL	Receive Special Purpose Valid 1	This is a status signal for receive transport overhead port 1. RSPVALID1 is asserted when valid data is present on RSPDAT1 (programmable active state). Transitions occur on RSPCLK1 falling edges.
	RSPCLK2	B18	O	TTL	Receive Special Purpose Clock 2	This is a clock reference for RSPDAT2 on special purpose serial output port 2. The frequency is 2.16MHz with a 50% duty cycle (optionally gapped to match the bandwidth of RSPDAT2).
	RSPDAT2	C17	O	TTL	Receive Special Purpose Data 2	This is the data output for receive special purpose serial port 2. RSPDAT2 transitions occur on the falling edge of RSPCLK2.
	RSPVALID2	B17	O	TTL	Receive Special Purpose Valid 2	This is a status signal for receive transport overhead port 2. RSPVALID2 is asserted when valid data is present on RSPDAT2 (programmable active state). Transitions occur on RSPCLK2 falling edges.
	RTOHCLK	B16	O	TTL	Receive Transport Overhead Clock	This is a clock reference for RTOH[3..0] on the receive transport overhead port. The frequency is 38.88MHz (50% duty cycle).
	RTOHVALID	B19	O	TTL	Receive Transport Overhead Valid	This is the valid status signal for the receive transport overhead port. RTOHVALID is asserted when valid data is present on RTOH[3..0] (programmable active state). RTOHVALID changes on the falling edge of RTOHCLK.
	RTOHFP	A18	O	TTL	Receive Transport Overhead Frame Pulse	This is a frame reference for the receive transport overhead port. RTOHFP outputs a single-cycle-wide pulse coincident with the first bit(s) of the first A1 octet output on RTOH[3..0]. RTOHFP transitions occur on the falling edge of RTOHCLK.
	RTOH[0] RTOH[1] RTOH[2] RTOH[3]	A21 D19 B20 C19	O	TTL	Receive Transport Overhead Data	These are the data outputs for the receive transport overhead (Section and Line) octets extracted from the incoming STS-48 data stream. RTOH[3..0] carries the entire transport ovehead in the order the octets are received. The most significant nibble (first received) is output first. RTOH[3] is the most significant bit. RTOH[3..0] transitions occur on the falling edge of RTOHCLK.

Table 1.1 Hardware Signal Definitions (9 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Tx Overhead Transport Access Processor (TOAP) Signals	TSPCLK1	A16	O	TTL	Transmit Special Purpose Clock 1	This is a clock reference for transmit special purpose port 1. The frequency is 2.16MHz with a 50% duty cycle (optionally gapped to match the bandwidth of TSPDAT1).
	TSPFP1	A13	O	TTL	Transmit Special Purpose Frame Pulse 1	This is a frame reference for transmit special purpose port 1. **Mode 1** (TSPCLK1 continuous): TSPFP1 outputs a single-cycle-wide pulse indicating the start of a new data stream on TSPDAT1. After TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge of TSPCLK1. TSPFP1 transitions occur on the falling edge of TSPCLK1. **Mode 2** (TSPCLK1 gapped): TSPFP1 outputs a single-cycle-wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT1. After TSPFP1 is asserted, the first bit of TSPDAT1 is sampled on the second rising edge of TSPCLK1. TSPFP1 transitions occur on the falling edge of TSPCLK1.
	TSPREN1	B15	O	TTL	Transmit Special Purpose Read Enable 1	This is a read enable for transmit special purpose port 1. TSPREN1 assertion to TSPDAT1 sampling is programmable. TSPREN1 transitions occur on TSPCLK1 falling edges.
	TSPDAT1	A15	I	TTL	Transmit Special Purpose Data 1	This is the serial data input for transmit special purpose port 1. TSPDAT1 is sampled on the rising edge of TSPCLK1.
	TSPCLK2	B13	O	TTL	Transmit Special Purpose Clock 2	This is a clock reference for transmit special purpose port 2. The frequency is 2.16MHz with a 50% duty cycle (optionally gapped to match the bandwidth of TSPDAT2).
	TSPFP2	B12	O	TTL	Transmit Special Purpose Frame Pulse 2	This is a frame reference for transmit special purpose port 2. **Mode 1** (TSPCLK2 continuous): TSPFP2 outputs a single-cycle-wide pulse indicating the start of a new data stream on TSPDAT2. After TSPFP2 is asserted, the first bit of TSPDAT2 is sampled on the second rising edge of TSPCLK2. TSPFP2 transitions occur on the falling edge of TSPCLK2. **Mode 2** (TSPCLK2 gapped): TSPFP2 outputs a single-cycle-wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT2. After TSPFP2 is asserted, the first bit of TSPDAT2 is sampled on the second rising edge of TSPCLK2. TSPFP2 transitions occur on the falling edge of TSPCLK2.
	TSPREN2	B11	O	TTL	Transmit Special Purpose Read Enable 2	This is a read enable for transmit special purpose port 2. TSPREN2 assertion to TSPDAT2 sampling is programmable. TSPREN2 transitions occur on TSPCLK2 falling edges.
	TSPDAT2	D13	I	TTL	Transmit Special Purpose Data 2	This is the serial data input for transmit special purpose port 2. TSPDAT2 is sampled on the rising edge of TSPCLK2.
	TTOHCLK	C13	O	TTL	Transmit Transport Overhead Clock	This is a clock reference for the transmit transport overhead port. The frequency is 38.88MHz with a 50% duty cycle.
	TTOHFP	C12	O	TTL	Transmit Transport Overhead Frame Pulse	This is a frame reference for the transmit transport overhead port. TTOHFP outputs a single clock-cycle-wide pulse indicating the start of a new data stream on TTOH[3..0]. The time from TTOHFP assertion to sampling the first bit on TTOH[3..0] is programmable (see TTOHREN). TTOHFP transitions on a falling edge of TTOHCLK.
	TTOHREN	A12	O	TTL	Transmit Transport Overhead Read Enable	This is a read enable for TTOH[3..0]. The time from TTOHREN assertion to TTOH[3..0] sampling is programmable. TTOHREN transitions occur on the falling edge of TTOHCLK.

Table 1.1 Hardware Signal Definitions (10 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Tx Overhead Transport Access Processor (TOAP) Signals	TTOHEN	C14	I	TTL	Transmit Transport Overhead Enable	When asserted, this signal enables insertion of TTOH[3..0] in the corresponding transport overhead octet of the outgoing STS-48 data stream. Transport overhead for the entire STS-48 is input as 4-bit nibbles on TTOH[3..0] (see TTOH[3..0] description). TTOHEN assertion during the first nibble of an overhead octet enables the corresponding overhead octet on TTOH[3..0]. Note: The Section and Line transmit overhead processing blocks (TSOP/TLOP) can selectively overwrite overhead octets inserted through the TTOH interface.
	TTOH[0] TTOH[1] TTOH[2] TTOH[3]	D16 C16 D15 C15	I	TTL	Transmit Transport Overhead Data	These are the data inputs for the transmit transport overhead (Section and Line) octets to be inserted in the outgoing STS-48 data stream. TTOH[3..0] carries the entire transport overhead in the order the octets are to be inserted. The most significant nibble (first received) is input first. TTOH[3] is the most significant bit. TTOH[3..0] is sampled on the rising edge of TTOHCLK.
Microprocessor Interface Signals	D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	AB6 AC4 AD4 AB7 AC5 AC6 AD6 AC7	I/O	TTL	CPU Data	This is a bidirectional data bus that provides microcontroller read/write access for transferring data to and from the device's internal registers.
	A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8]	AB9 AD7 AA10 AC9 AD9 AC10 AB11 AC11 AB13	I	TTL	CPU Address	This is the register address bus used to select specific internal registers during microcontroller read/write accesses.

Table 1.1 Hardware Signal Definitions (11 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
Microprocessor (CPU) Interface Signals	ALE	AA12	I	TTL	CPU Address Latch Enable	This signal is used to latch internal address bus signals, enabling access to the device's multiplexed address/data bus. When low the address bus A[8..0] is latched internally. When high the internal address bus latches are transparent, which enables the bus to interface with multiplexed address/data. The ALE signal has an internal pull-up resistor.
	CSB	AD10	I	TTL	CPU Chip Select (active low)	This signal must be asserted to enable internal register read/write access cycles (active low). The CSB signal is used in conjunction with the RDB/WRB signals. The CSB signal has an internal pull-up resistor.
	RDB	AB8	I	TTL	CPU Read Enable (active low)	This signal is used for internal register read operations. When RDB and CSB are both asserted (active low), data in the register selected by A[8..0] is presented at D[7..0]. The RDB signal has an internal pull-up resistor.
	WRB	AB10	I	TTL	CPU Write Enable (active low)	This signal is used for internal register write operations. When WRB and CSB are both asserted (active low), data present at D[7..0] is written to the register selected by A[8..0]. The WRB signal has an internal pull-up resistor.
	INTB	AA9	O	TTL	CPU Interrupt (active low)	This signal is asserted (active low) when an internal interrupt source is pending and the interrupt is unmasked (enabled). The INTB signal is de-asserted when the interrupt pending bits have been cleared. The INTB is an open-drain signal.
	RSTB	AD3	I	TTL	Chip Reset (active low)	This signal is used to perform an asynchronous reset of the device (active low). The device is held in a reset state while the RSTB signal is low. The signal is Schmitt-trigged with an internal pull-up resistor. All outputs are tristated when RSTB is asserted.
	PMTICK	AB12	I/O	TTL	Performance Monitoring Tick	This bidirectional signal pin provides a means of monitoring PM Ticks (performance monitoring ticks) and latching internal performance monitoring counters. **Output:** When configured as an output, this signal is optionally asserted when the internal PMTICK timer generates a "PM Tick", which latches the performance monitoring counters in the device. **Input:** A low-to-high transition optionally latches the performance monitoring counters in the device. Note: This pin is configured as an input on reset.
	GPIO[0] GPIO[1] GPIO[2] GPIO[3] GPIO[4] GPIO[5] GPIO[6] GPIO[7]	AA20 AB20 AA19 AC20 AB19 AC19 AD19 AB18	I/O	TTL	General Purpose Input/Output	These are general purpose pins that are individually-configurable as inputs or outputs. They are intended for user-customizable control and monitoring functions between the VSC9142 and external devices.

Table 1.1 Hardware Signal Definitions (12 of 12)

	Pin Label	Pad	I/O	Type	Signal Name	Description
JTAG Test Access Port Signals	TDO	AC21	O	TTL	JTAG Test Data Output	This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output that is inactive except when data scan shifting is in progress.
	TDI	AD22	I	TTL	JTAG Test Data Input	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
	TCK	AB21	I	TTL	JTAG Test Clock	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
	TMS	AC22	I	TTL	JTAG Test Mode Select	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
	TRSTB	AB24	I	TTL	JTAG Test Reset	This signal is an asynchronous reset for the IEEE P1149.1 test access port (active low). TRSTB is a Schmitt-triggered input with an internal pull-up resistor.
	OE	AD21	I	TTL	Chip Output Enable	This signal is the test access port enable (active high). When deasserted (low), all TTL device outputs are tristated. OE has an internal pull-up resistor.

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This document is an excerpt of the VSC9142 Data Book. For the complete data book, please contact your local sales representative (NDA required).

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