FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50230-2E

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

32M (×16) FLASH MEMORY & 4M (×16) STATIC RAM

MB84VD22184FM-70/MB84VD22194FM-70

■ FEATURES

- **Power Supply Voltage of 2.7 V to 3.1 V**
- **High Performance**
  70 ns maximum access time (Flash)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –30 °C to +85 °C
- **Package 56-ball FBGA**

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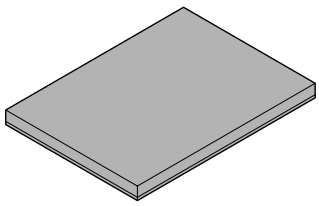
■ PRODUCT LINE UP

Part No.	VD22184FM / VD22194FM	
Supply Voltage(V)	V_{CCf}= 3.0V $^{+0.1\ V}_{-0.3\ V}$	V_{CCS}= 3.0V $^{+0.1\ V}_{-0.3\ V}$
Max Address Access Time (ns)	70	70
Max $\overline{CE}$ Access Time (ns)	70	70
Max $\overline{OE}$ Access Time (ns)	30	35

Note: Both V_{CCf} and V_{CCS} must be in recommended operation range when either part is being accessed.

■ PACKAGE

56-ball plastic FBGA



(BGA-56P-M03)

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— FLASH MEMORY

- **Simultaneous Read/Write Operations (Dual Bank)**
  Bank 1 : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Bank 2 : 24 Mbit (64 KB × 48)
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.
  Read-while-erase
  Read-while-program
- **Minimum 100,000 Write/Erase Cycles**
- **Sector Erase Architecture**
  Eight 4K word and sixty-three 32K word sectors in word mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VD22184: Top sector
  MB84VD22194: Bottom sector
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™* Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready-Busy Output (RY/$\overline{BY}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC}f Write Inhibit ≤ 2.5 V**
- **HiddenROM Region**
  256 byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{WP}$/ACC Input Pin**
  At V_{IL}, allows protection of “outermost” 2 × 8 bytes on boot sectors, regardless of sector protection/unprotection status.
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to “MBM29DL34TF/BF” Datasheet in Detailed Function**

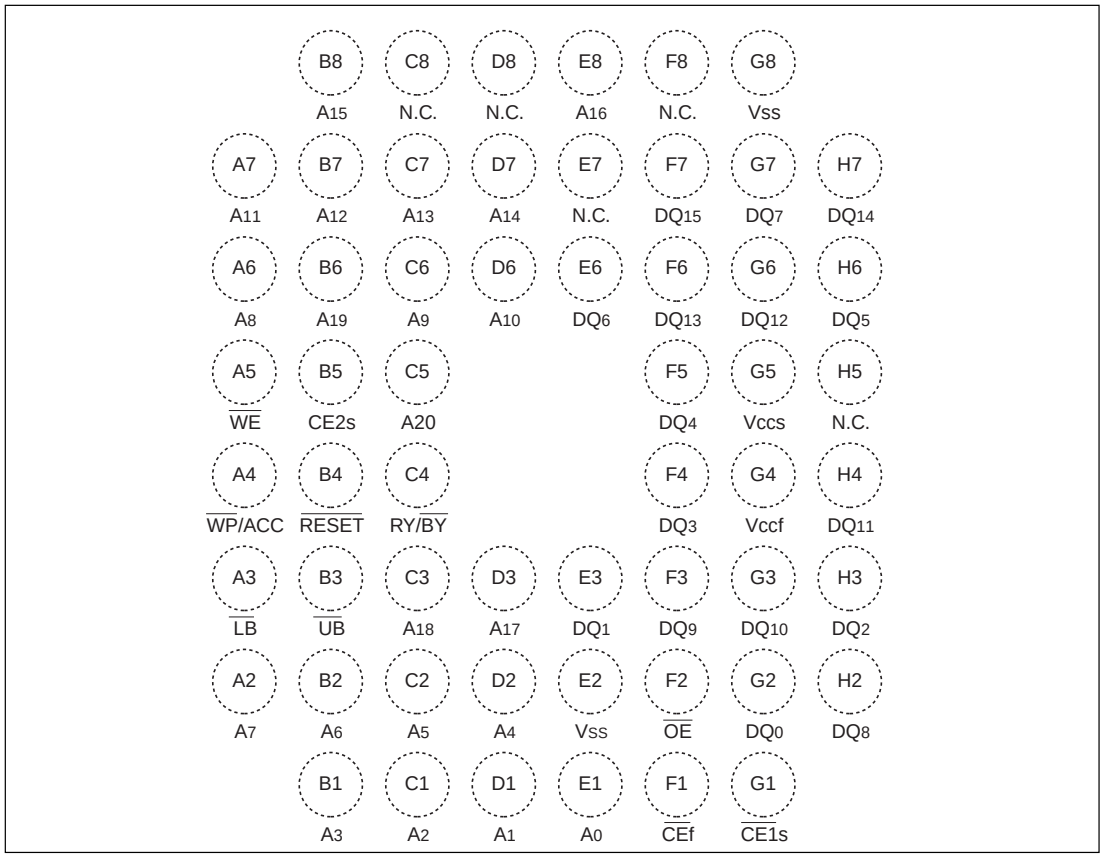
— SRAM

- **Power Dissipation**
  Operating : 40 mA Max
  Standby : 10 µA Max
- **Power Down Features using $\overline{CE1}$s and CE2s**
- **Data Retention Supply Voltage: 1.5 V to 3.1 V**
- **$\overline{CE1}$s and CE2s Chip Select**
- **Byte Data Control: $\overline{LB}$ (DQ_7 to DQ_0), $\overline{UB}$ (DQ_{15} to DQ_8)**

*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENT

(Top View)
Marking side

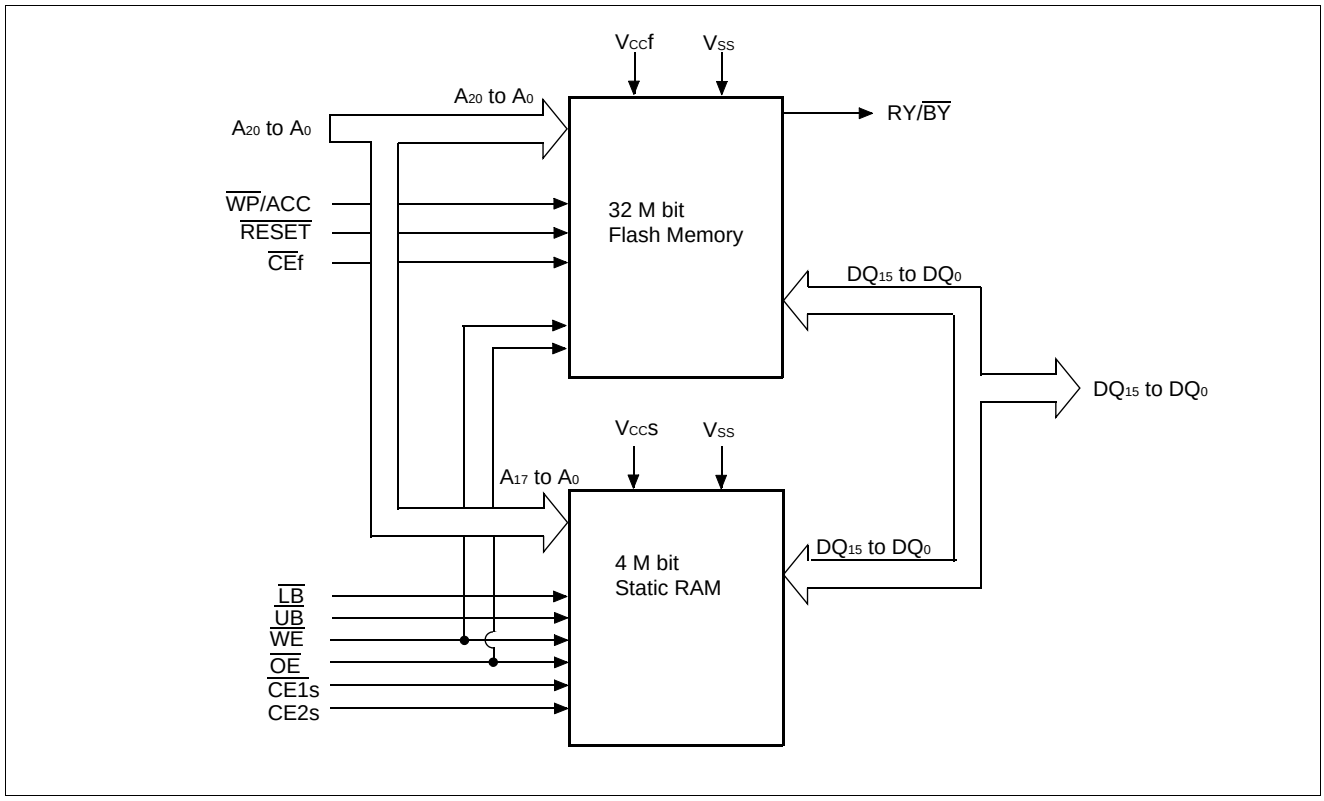


(BGA-56P-M03)

■ PIN DESCRIPTION

Pin Name	Function	Input/Output
A_{17} to A_0	Address Inputs (Common)	I
A_{20} to A_{18}	Address Inputs (Flash)	I
DQ_{15} to DQ_0	Data Inputs / Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE1}$s	Chip Enable (SRAM)	I
CE2s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{UB}$	Upper Byte Control (SRAM)	I
$\overline{LB}$	Lower Byte Control (SRAM)	I
$\overline{RESET}$	Hardware Reset Pin / Sector Protection Unlock (Flash)	I
$\overline{WP}$/ACC	Write Protect / Acceleration (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (SRAM)	Power

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

- **User Bus Operations**

Operation *1, *3	$\overline{CEf}$	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$	$\overline{WP}$/ ACC *5
Full Standby	H	H	X	X	X	X	X	High-Z	High-Z	H	X
		X	L								
Output Disable	H	L	H	H	H	X	X	High-Z	High-Z	H	X
				X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	High-Z	High-Z		
		X	L								
Read from Flash *2	L	H	X	L	H	X	X	D_{OUT}	D_{OUT}	H	X
		X	L								
Write to Flash	L	H	X	H	L	X	X	D_{IN}	D_{IN}	H	X
		X	L								
Read from SRAM	H	L	H	L	H	L	L	D_{OUT}	D_{OUT}	H	X
						H	L	High-Z	D_{OUT}		
						L	H	D_{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	L	L	D_{IN}	D_{IN}	H	X
						H	L	High-Z	D_{IN}		
						L	H	D_{IN}	High-Z		
Temporary Sector Group Unprotection*4	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	High-Z	High-Z	L	X
		X	L								
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

*1 : Other operations except for indicated this column are inhibited.

*2 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*3 : Do not apply $\overline{CEf}$ = V_{IL}, $\overline{CE1s}$ = V_{IL} and CE2s = V_{IH} at a time.

*4 : It is also used for the extended sector group protections.

*5 : $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
$\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
$\overline{WP}$/ACC = V_{ACC} (9V) ; Program time will reduce by 40%.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins except $\overline{RESET}$, $\overline{WP}$/ACC *1	V_{IN}, V_{OUT}	–0.3	$V_{CC}f$ + 0.3	V
			$V_{CC}s$ + 0.4	V
$V_{CC}f$/$V_{CC}s$ Supply *1	$V_{CC}f$, $V_{CC}s$	–0.3	+3.3	V
$\overline{RESET}$ *2	V_{IN}	–0.5	+13.0	V
$\overline{WP}$/ACC *3	V_{IN}	–0.5	+10.5	V

*1 : Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$+0.3 V or $V_{CC}s$+0.4 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$+1.0 V or $V_{CC}s$ + 1.0 V for periods of up to 20 ns.

*2 : Minimum DC input voltage on $\overline{RESET}$ pin is –0.5 V. During voltage transitions, $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-$V_{CC}f$ or $V_{CC}s$) does not exceed +9.0 V. Maximum DC input voltage on $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	–30	+85	°C
$V_{CC}f$/$V_{CC}s$ Supply Voltages	Vccf, Vccs	+2.7	+3.1	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CCf}, V_{CCs}		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CCf}, V_{CCs}		–1.0	—	+1.0	µA
$\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CCf} = V_{CCf} Max, V_{CCs} = V_{CCs} Max, $\overline{RESET}$ = 12.5V		—	—	35	µA
Flash V_{CC} Active Current (Read) *1	I_{CC1f}	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} = 5 MHz	—	—	18	mA
			t_{CYCLE} = 1 MHz	—	—	4	mA
Flash V_{CC} Active Current (Program/Erase) *2	I_{CC2f}	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	30	mA
Flash V_{CC} Active Current (Read-While-Program) *5	I_{CC3f}	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	48	mA
Flash V_{CC} Active Current (Read-While-Erase) *5	I_{CC4f}	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	48	mA
Flash V_{CC} Active Current (Erase-Suspend-Program)	I_{CC5f}	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	35	mA
ACC Input Leakage Current	I_{LIA}	V_{CCf} = V_{CCf} Max, V_{CCs} = V_{CCs} Max, $\overline{WP}$/ACC = V_{ACC} Max		—	—	20	mA
SRAM V_{CC} Active Current	I_{CC1s}	V_{CCs} = V_{CCs} Max, $\overline{CE1}_s$ = V_{IL}, $CE2_s$ = V_{IH}	t_{CYCLE} =10 MHz	—	—	40	mA
SRAM V_{CC} Active Current	I_{CC2s}	$\overline{CE1}_s$ = 0.2 V, $CE2_s$ = V_{CCs} – 0.2 V	t_{CYCLE} = 10 MHz	—	—	40	mA
			t_{CYCLE} = 1 MHz	—	—	8	mA
Flash V_{CC} Standby Current	I_{SB1f}	V_{CCf} = V_{CCf} Max, $\overline{CE}_f$ = V_{CCf} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V		—	—	5	µA
Flash V_{CC} Standby Current (RESET)	I_{SB2f}	V_{CCf} = V_{CCf} Max, $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V		—	—	5	µA
Flash V_{CC} Current (Automatic Sleep Mode) *3	I_{SB3f}	V_{CCf} = V_{CCf} Max, $\overline{CE}_f$ = V_{SS} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V V_{IN} = V_{CCf}± 0.3 V or V_{SS} ± 0.3 V		—	—	5	µA
SRAM V_{CC} Standby Current	I_{SB1s}	$\overline{CE1}_s$ ≥ V_{CCs} – 0.2 V, $CE2_s$ ≥ V_{CCs} – 0.2 V $\overline{LB}$ = $\overline{UB}$ ≥ V_{CCs}–0.2 V or ≤ 0.2V		—	—	10	µA
SRAM V_{CC} Standby Current	I_{SB2s}	$\overline{CE1}_s$ ≥ V_{CCs} – 0.2 V or ≤ 0.2V, $CE2_s$ ≤ 0.2 V $\overline{LB}$ = $\overline{UB}$ ≥ V_{CCs}–0.2 V or ≤ 0.2V		—	—	10	µA

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Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input Low Level	V_{IL}	—	–0.3	—	0.5	V
Input High Level	V_{IH}	—	2.2	—	V_{CC}+0.3*6	V
Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) *4	V_{ID}	—	11.5	—	12.5	V
Voltage for Program Acceleration ($\overline{WP}$/ACC) *4	V_{ACC}	—	8.5	9.0	9.5	V
SRAM Output Low Level	V_{OL}	V_{CCS} = V_{CCS} Min, I_{OL} = 0.1 mA	—	—	0.4	V
SRAM Output High Level	V_{OH}	V_{CCS} = V_{CCS} Min, I_{OH} = –0.1 mA	2.0	—	—	V
Flash Output Low Level	V_{OL}	V_{CCF} = V_{CCF} Min, I_{OL} = 4.0 mA	—	—	0.45	V
Flash Output High Level	V_{OH}	V_{CCF} = V_{CCF} Min, I_{OH} = –0.1 mA	V_{CCS}–0.4	—	—	V
Flash Low V_{CCF} Lock-Out Voltage	V_{LKO}	—	2.3	—	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4 : Applicable for only V_{CCF} applying.

*5 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

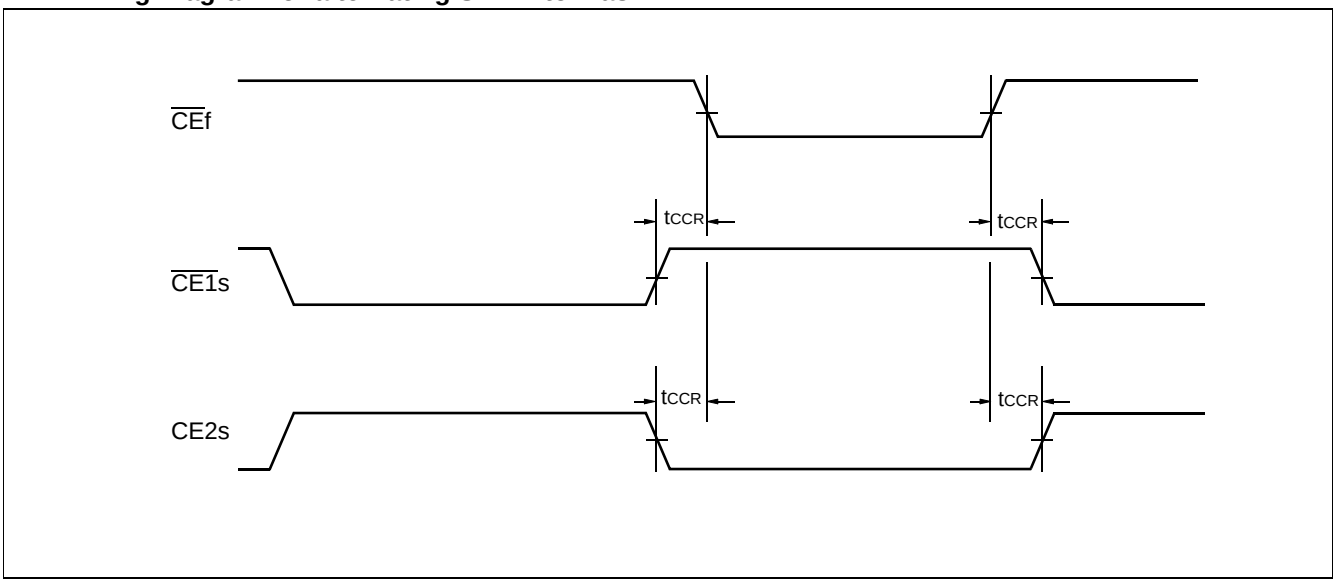
*6 : V_{CC} indicates lower of V_{CCF} or V_{CCS}.

2. AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter	Symbol		Test Setup		Value	Unit
	JEDEC	Standard				
$\overline{CE}$ Recover Time	—	t_{CCR}	—	Min	0	ns

- **Timing Diagram for alternating SRAM to Flash**

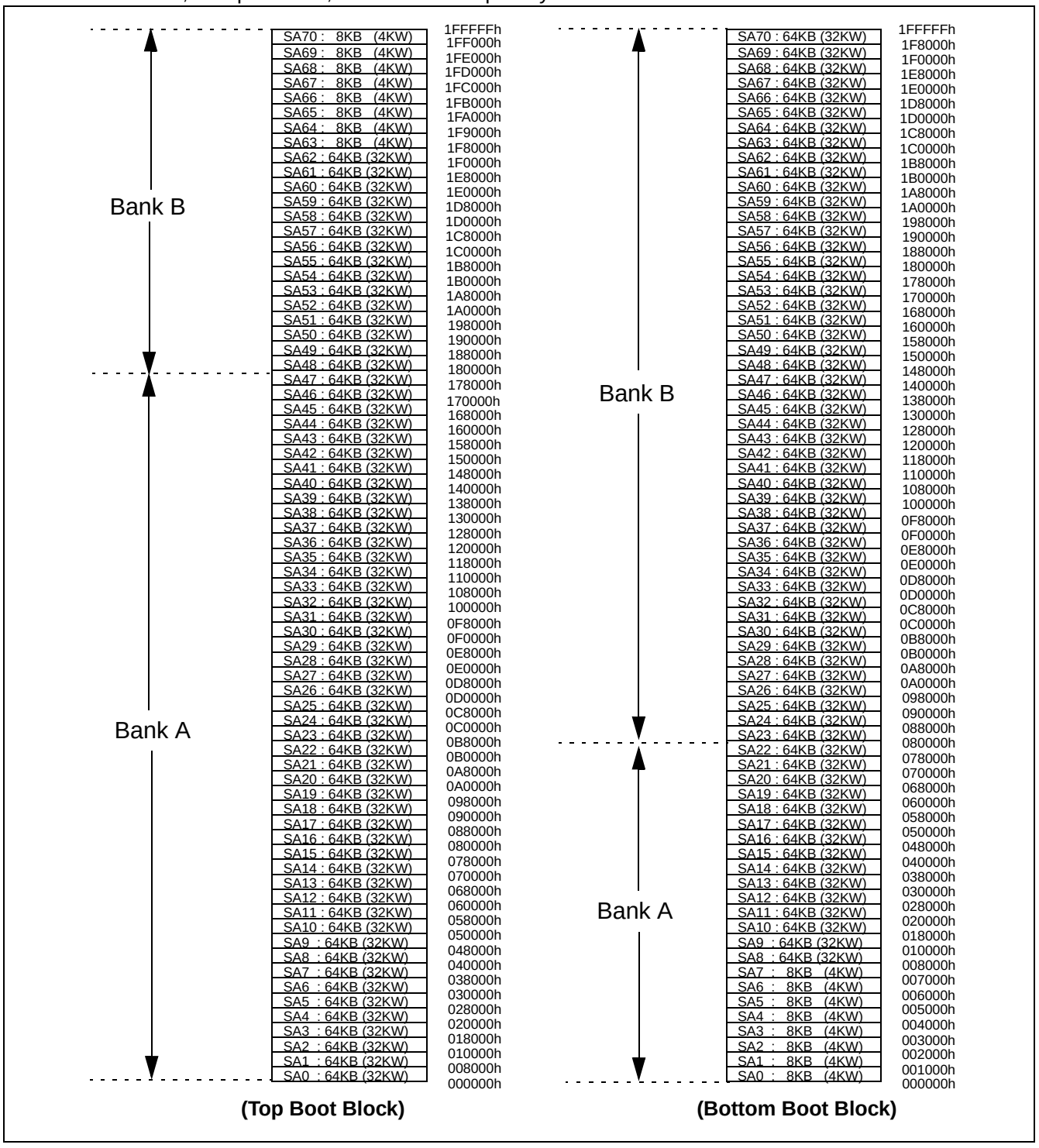


- **Flash Characteristics**
  Please refer to "■32M Flash Memory for MCP".
- **SRAM Characteristics,**
  Please refer to "■4M SRAM for MCP".

■ 32 M FLASH MEMORY for MCP

1. Flexible Sector-erase Architecture on Flash Memory

- Eight 4 K words, and sixty three 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



Sector Address Table (Top Boot Type)

Bank	Sector	Sector address										Sector size (Kwords)	Address range
		Bank address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank B	SA0	0	0	0	0	0	0	X	X	X	X	32	000000h to 007FFFh
	SA1	0	0	0	0	0	1	X	X	X	X	32	008000h to 00FFFFh
	SA2	0	0	0	0	1	0	X	X	X	X	32	010000h to 017FFFh
	SA3	0	0	0	0	1	1	X	X	X	X	32	018000h to 01FFFFh
	SA4	0	0	0	1	0	0	X	X	X	X	32	020000h to 027FFFh
	SA5	0	0	0	1	0	1	X	X	X	X	32	028000h to 02FFFFh
	SA6	0	0	0	1	1	0	X	X	X	X	32	030000h to 037FFFh
	SA7	0	0	0	1	1	1	X	X	X	X	32	038000h to 03FFFFh
	SA8	0	0	1	0	0	0	X	X	X	X	32	040000h to 047FFFh
	SA9	0	0	1	0	0	1	X	X	X	X	32	048000h to 04FFFFh
	SA10	0	0	1	0	1	0	X	X	X	X	32	050000h to 057FFFh
	SA11	0	0	1	0	1	1	X	X	X	X	32	058000h to 05FFFFh
	SA12	0	0	1	1	0	0	X	X	X	X	32	060000h to 067FFFh
	SA13	0	0	1	1	0	1	X	X	X	X	32	068000h to 06FFFFh
	SA14	0	0	1	1	1	0	X	X	X	X	32	070000h to 077FFFh
	SA15	0	0	1	1	1	1	X	X	X	X	32	078000h to 07FFFFh
	SA16	0	1	0	0	0	0	X	X	X	X	32	080000h to 087FFFh
	SA17	0	1	0	0	0	1	X	X	X	X	32	088000h to 08FFFFh
	SA18	0	1	0	0	1	0	X	X	X	X	32	090000h to 097FFFh
	SA19	0	1	0	0	1	1	X	X	X	X	32	098000h to 09FFFFh
	SA20	0	1	0	1	0	0	X	X	X	X	32	0A0000h to 0A7FFFh
	SA21	0	1	0	1	0	1	X	X	X	X	32	0A8000h to 0AFFFFh
	SA22	0	1	0	1	1	0	X	X	X	X	32	0B0000h to 0B7FFFh
	SA23	0	1	0	1	1	1	X	X	X	X	32	0B8000h to 0BFFFFh
	SA24	0	1	1	0	0	0	X	X	X	X	32	0C0000h to 0C7FFFh
	SA25	0	1	1	0	0	1	X	X	X	X	32	0C8000h to 0CFFFFh
	SA26	0	1	1	0	1	0	X	X	X	X	32	0D0000h to 0D7FFFh
	SA27	0	1	1	0	1	1	X	X	X	X	32	0D8000h to 0DFFFFh
	SA28	0	1	1	1	0	0	X	X	X	X	32	0E0000h to 0E7FFFh
	SA29	0	1	1	1	0	1	X	X	X	X	32	0E8000h to 0EFFFFh
	SA30	0	1	1	1	1	0	X	X	X	X	32	0F0000h to 0F7FFFh
	SA31	0	1	1	1	1	1	X	X	X	X	32	0F8000h to 0FFFFFh

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Bank	Sector	Sector address										Sector size (Kwords)	Address range
		Bank address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank B	SA32	1	0	0	0	0	0	X	X	X	X	32	100000h to 107FFFh
	SA33	1	0	0	0	0	1	X	X	X	X	32	108000h to 10FFFFh
	SA34	1	0	0	0	1	0	X	X	X	X	32	110000h to 117FFFh
	SA35	1	0	0	0	1	1	X	X	X	X	32	118000h to 11FFFFh
	SA36	1	0	0	1	0	0	X	X	X	X	32	120000h to 127FFFh
	SA37	1	0	0	1	0	1	X	X	X	X	32	128000h to 12FFFFh
	SA38	1	0	0	1	1	0	X	X	X	X	32	130000h to 137FFFh
	SA39	1	0	0	1	1	1	X	X	X	X	32	138000h to 13FFFFh
	SA40	1	0	1	0	0	0	X	X	X	X	32	140000h to 147FFFh
	SA41	1	0	1	0	0	1	X	X	X	X	32	148000h to 14FFFFh
	SA42	1	0	1	0	1	0	X	X	X	X	32	150000h to 157FFFh
	SA43	1	0	1	0	1	1	X	X	X	X	32	158000h to 15FFFFh
	SA44	1	0	1	1	0	0	X	X	X	X	32	160000h to 167FFFh
	SA45	1	0	1	1	0	1	X	X	X	X	32	168000h to 16FFFFh
	SA46	1	0	1	1	1	0	X	X	X	X	32	170000h to 177FFFh
	SA47	1	0	1	1	1	1	X	X	X	X	32	178000h to 17FFFFh
Bank A	SA48	1	1	0	0	0	0	X	X	X	X	32	180000h to 187FFFh
	SA49	1	1	0	0	0	1	X	X	X	X	32	188000h to 18FFFFh
	SA50	1	1	0	0	1	0	X	X	X	X	32	190000h to 197FFFh
	SA51	1	1	0	0	1	1	X	X	X	X	32	198000h to 19FFFFh
	SA52	1	1	0	1	0	0	X	X	X	X	32	1A0000h to 1A7FFFh
	SA53	1	1	0	1	0	1	X	X	X	X	32	1A8000h to 1AFFFFh
	SA54	1	1	0	1	1	0	X	X	X	X	32	1B0000h to 1B7FFFh
	SA55	1	1	0	1	1	1	X	X	X	X	32	1B8000h to 1BFFFFh
	SA56	1	1	1	0	0	0	X	X	X	X	32	1C0000h to 1C7FFFh
	SA57	1	1	1	0	0	1	X	X	X	X	32	1C8000h to 1CFFFFh
	SA58	1	1	1	0	1	0	X	X	X	X	32	1D0000h to 1D7FFFh
	SA59	1	1	1	0	1	1	X	X	X	X	32	1D8000h to 1DFFFFh
	SA60	1	1	1	1	0	0	X	X	X	X	32	1E0000h to 1E7FFFh
	SA61	1	1	1	1	0	1	X	X	X	X	32	1E8000h to 1EFFFFh
	SA62	1	1	1	1	1	0	X	X	X	X	32	1F0000h to 1F7FFFh
	SA63	1	1	1	1	1	1	0	0	0	X	4	1F8000h to 1F8FFFh
	SA64	1	1	1	1	1	1	0	0	1	X	4	1F9000h to 1F9FFFh
	SA65	1	1	1	1	1	1	0	1	0	X	4	1FA000h to 1FAFFFh
	SA66	1	1	1	1	1	1	0	1	1	X	4	1FB000h to 1FBFFFh
	SA67	1	1	1	1	1	1	1	0	0	X	4	1FC000h to 1FCFFFh
	SA68	1	1	1	1	1	1	1	0	1	X	4	1FD000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	0	X	4	1FE000h to 1FEFFFh
	SA70	1	1	1	1	1	1	1	1	1	X	4	1FF000h to 1FFFFFh

Sector Address Table (Bottom Boot Type)

Bank	Sector	Sector address										Sector size (Kwords)	Address range
		Bank address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank B	SA70	1	1	1	1	1	1	X	X	X	X	32	1F8000h to 1FFFFFh
	SA69	1	1	1	1	1	0	X	X	X	X	32	1F0000h to 1F7FFFh
	SA68	1	1	1	1	0	1	X	X	X	X	32	1E8000h to 1EFFFFh
	SA67	1	1	1	1	0	0	X	X	X	X	32	1E0000h to 1E7FFFh
	SA66	1	1	1	0	1	1	X	X	X	X	32	1D8000h to 1DFFFFh
	SA65	1	1	1	0	1	0	X	X	X	X	32	1D0000h to 1D7FFFh
	SA64	1	1	1	0	0	1	X	X	X	X	32	1C8000h to 1CFFFFh
	SA63	1	1	1	0	0	0	X	X	X	X	32	1C0000h to 1C7FFFh
	SA62	1	1	0	1	1	1	X	X	X	X	32	1B8000h to 1BFFFFh
	SA61	1	1	0	1	1	0	X	X	X	X	32	1B0000h to 1B7FFFh
	SA60	1	1	0	1	0	1	X	X	X	X	32	1A8000h to 1AFFFFh
	SA59	1	1	0	1	0	0	X	X	X	X	32	1A0000h to 1A7FFFh
	SA58	1	1	0	0	1	1	X	X	X	X	32	198000h to 19FFFFh
	SA57	1	1	0	0	1	0	X	X	X	X	32	190000h to 197FFFh
	SA56	1	1	0	0	0	1	X	X	X	X	32	188000h to 18FFFFh
	SA55	1	1	0	0	0	0	X	X	X	X	32	180000h to 187FFFh
	SA54	1	0	1	1	1	1	X	X	X	X	32	178000h to 17FFFFh
	SA53	1	0	1	1	1	0	X	X	X	X	32	170000h to 177FFFh
	SA52	1	0	1	1	0	1	X	X	X	X	32	168000h to 16FFFFh
	SA51	1	0	1	1	0	0	X	X	X	X	32	160000h to 167FFFh
	SA50	1	0	1	0	1	1	X	X	X	X	32	158000h to 15FFFFh
	SA49	1	0	1	0	1	0	X	X	X	X	32	150000h to 157FFFh
	SA48	1	0	1	0	0	1	X	X	X	X	32	148000h to 14FFFFh
	SA47	1	0	1	0	0	0	X	X	X	X	32	140000h to 147FFFh
	SA46	1	0	0	1	1	1	X	X	X	X	32	138000h to 13FFFFh
	SA45	1	0	0	1	1	0	X	X	X	X	32	130000h to 137FFFh
	SA44	1	0	0	1	0	1	X	X	X	X	32	128000h to 12FFFFh
	SA43	1	0	0	1	0	0	X	X	X	X	32	120000h to 127FFFh
	SA42	1	0	0	0	1	1	X	X	X	X	32	118000h to 11FFFFh
	SA41	1	0	0	0	1	0	X	X	X	X	32	110000h to 117FFFh
	SA40	1	0	0	0	0	1	X	X	X	X	32	108000h to 10FFFFh
	SA39	1	0	0	0	0	0	X	X	X	X	32	100000h to 107FFFh

(Continued)

Bank	Sector	Sector address										Sector size (Kwords)	Address range
		Bank address											
		A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		
Bank B	SA38	0	1	1	1	1	1	X	X	X	X	32	0F8000h to 0FFFFFh
	SA37	0	1	1	1	1	0	X	X	X	X	32	0F0000h to 0F7FFFh
	SA36	0	1	1	1	0	1	X	X	X	X	32	0E8000h to 0EFFFFh
	SA35	0	1	1	1	0	0	X	X	X	X	32	0E0000h to 0E7FFFh
	SA34	0	1	1	0	1	1	X	X	X	X	32	0D8000h to 0DFFFFh
	SA33	0	1	1	0	1	0	X	X	X	X	32	0D0000h to 0D7FFFh
	SA32	0	1	1	0	0	1	X	X	X	X	32	0C8000h to 0CFFFFh
	SA31	0	1	1	0	0	0	X	X	X	X	32	0C0000h to 0C7FFFh
	SA30	0	1	0	1	1	1	X	X	X	X	32	0B8000h to 0BFFFFh
	SA29	0	1	0	1	1	0	X	X	X	X	32	0B0000h to 0B7FFFh
	SA28	0	1	0	1	0	1	X	X	X	X	32	0A8000h to 0AFFFFh
	SA27	0	1	0	1	0	0	X	X	X	X	32	0A0000h to 0A7FFFh
	SA26	0	1	0	0	1	1	X	X	X	X	32	098000h to 09FFFFh
	SA25	0	1	0	0	1	0	X	X	X	X	32	090000h to 097FFFh
	SA24	0	1	0	0	0	1	X	X	X	X	32	088000h to 08FFFFh
	SA23	0	1	0	0	0	0	X	X	X	X	32	080000h to 087FFFh
Bank A	SA22	0	0	1	1	1	1	X	X	X	X	32	078000h to 07FFFFh
	SA21	0	0	1	1	1	0	X	X	X	X	32	070000h to 077FFFh
	SA20	0	0	1	1	0	1	X	X	X	X	32	068000h to 06FFFFh
	SA19	0	0	1	1	0	0	X	X	X	X	32	060000h to 067FFFh
	SA18	0	0	1	0	1	1	X	X	X	X	32	058000h to 05FFFFh
	SA17	0	0	1	0	1	0	X	X	X	X	32	050000h to 057FFFh
	SA16	0	0	1	0	0	1	X	X	X	X	32	048000h to 04FFFFh
	SA15	0	0	1	0	0	0	X	X	X	X	32	040000h to 047FFFh
	SA14	0	0	0	1	1	1	X	X	X	X	32	038000h to 03FFFFh
	SA13	0	0	0	1	1	0	X	X	X	X	32	030000h to 037FFFh
	SA12	0	0	0	1	0	1	X	X	X	X	32	028000h to 02FFFFh
	SA11	0	0	0	1	0	0	X	X	X	X	32	020000h to 027FFFh
	SA10	0	0	0	0	1	1	X	X	X	X	32	018000h to 01FFFFh
	SA9	0	0	0	0	1	0	X	X	X	X	32	010000h to 017FFFh
	SA8	0	0	0	0	0	1	X	X	X	X	32	008000h to 00FFFFh
	SA7	0	0	0	0	0	0	1	1	1	X	4	007000h to 007FFFh
	SA6	0	0	0	0	0	0	1	1	0	X	4	006000h to 006FFFh
	SA5	0	0	0	0	0	0	1	0	1	X	4	005000h to 005FFFh
	SA4	0	0	0	0	0	0	1	0	0	X	4	004000h to 004FFFh
	SA3	0	0	0	0	0	0	0	1	1	X	4	003000h to 003FFFh
	SA2	0	0	0	0	0	0	0	1	0	X	4	002000h to 002FFFh
	SA1	0	0	0	0	0	0	0	0	1	X	4	001000h to 001FFFh
	SA0	0	0	0	0	0	0	0	0	0	X	4	000000h to 000FFFh

Sector Group Addresses Table (Top Boot Type)

Sector group	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	0	1	X	X	X	SA1 to SA3
					1	0				
					1	1				
SGA2	0	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	0	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	0	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	0	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	0	1	1	1	X	X	X	X	X	SA28 to SA31
SGA9	1	0	0	0	X	X	X	X	X	SA32 to SA35
SGA10	1	0	0	1	X	X	X	X	X	SA36 to SA39
SGA11	1	0	1	0	X	X	X	X	X	SA40 to SA43
SGA12	1	0	1	1	X	X	X	X	X	SA44 to SA47
SGA13	1	1	0	0	X	X	X	X	X	SA48 to SA51
SGA14	1	1	0	1	X	X	X	X	X	SA52 to SA55
SGA15	1	1	1	0	X	X	X	X	X	SA56 to SA59
SGA16	1	1	1	1	0	0	X	X	X	SA60 to SA62
					0	1				
					1	0				
SGA17	1	1	1	1	1	1	0	0	0	SA63
SGA18	1	1	1	1	1	1	0	0	1	SA64
SGA19	1	1	1	1	1	1	0	1	0	SA65
SGA20	1	1	1	1	1	1	0	1	1	SA66
SGA21	1	1	1	1	1	1	1	0	0	SA67
SGA22	1	1	1	1	1	1	1	0	1	SA68
SGA23	1	1	1	1	1	1	1	1	0	SA69
SGA24	1	1	1	1	1	1	1	1	1	SA70

Sector Group Addresses Table (Bottom Boot Type)

Sector group	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	1	X	X	X	SA8 to SA10
					1	0				
					1	1				
SGA9	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	1	1	1	1	0	0	X	X	X	SA67 to SA69
					0	1				
					1	0				
SGA24	1	1	1	1	1	1	X	X	X	SA70

Sector Group Protection Verify Autoselect Codes Table (Top Boot Type)

Type	A_{20} to A_{12}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	2250h
Sector Group Protection	SA	L	L	L	H	L	01h*

Legend: L = V_{IL}, H = V_{IH}. See DC Characteristics for voltage levels.

* : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

Expanded Autoselect Code Table (Top Boot Type)

Type	Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code	04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	2250h	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0
Sector Group Protection	01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Sector Group Protection Verify Autoselect Codes Table (Bottom Boot Type)

Type	A_{20} to A_{12}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	2253h
Sector Group Protection	SA	L	L	L	H	L	01h*

Legend: L = V_{IL}, H = V_{IH}. See DC Characteristics for voltage levels.

* : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

Expanded Autoselect Code Table (Bottom Boot Type)

Type	Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code	04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	2253h	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	1
Sector Group Protection	01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Command Definitions Table

Command sequence	Bus write cycles req'd	First bus write cycle		Second bus write cycle		Third bus write cycle		Fourth bus read/write cycle		Fifth bus write cycle		Sixth bus write cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset*[1]	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset*[1]	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Program Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program *[2]	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode *[2]	2	BA	90h	XXXh	F0h*[6]	—	—	—	—	—	—	—	—
Extended Sector Group Protection *[3]	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
Query *[4]	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
HiddenROM Program *[5]	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
HiddenROM Exit *[5]	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—

(Continued)

(Continued)

*1 : Both of these reset commands are equivalent.

*2 : This command is valid during Fast Mode.

*3 : This command is valid while $\overline{RESET} = V_{ID}$.

*4 : The valid address are A_6 to A_0.

*5 : This command is valid during HiddenROM mode.

*6 : The date “00h” is also acceptable.

Notes:
- Address bits A_{20} to A_{11} = X = “H” or “L” for all address commands except or Program Address (PA) , Sector Address (SA) , Bank Address (BA) .
- Bus operations are defined in “User Bus Operations Tables” (■DEVICE BUS OPERATION).
- RA = Address of the memory location to be read
  PA = Address of the memory location to be programmed
  Addresses are latched on the falling edge of the write pulse.
  SA = Address of the sector to be erased. The combination of A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
  BA = Bank Address (A_{20} to A_{18})
- RD = Data read from location RA during read operation.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA = Sector group address to be protected. Set sector group address and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) .
  SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the HiddenROM area
  Top Boot Type : 1FF000h to 1FF07Fh
  Bottom Boot Type : 000000h to 00007Fh
- HRBA = Bank Address of the HiddenROM area
  Top Boot Type : $A_{20} = A_{19} = A_{18} = 1$
  Bottom Boot Type : $A_{20} = A_{19} = A_{18} = 0$
- The system should generate the following address patterns :
  Word Mode : 555h or 2AAh to addresses A_{10} to A_0
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- The command combinations not described in “Command Definitions Table” are illegal.

2. AC Characteristics

- **Read Only Operations Characteristics**

Parameter	Symbol		Test setup	Value*		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	ns
Output Hold Time from Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	µs

* : Test Conditions:
Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 0.5 × Vccf
Output: 0.5 × Vccf

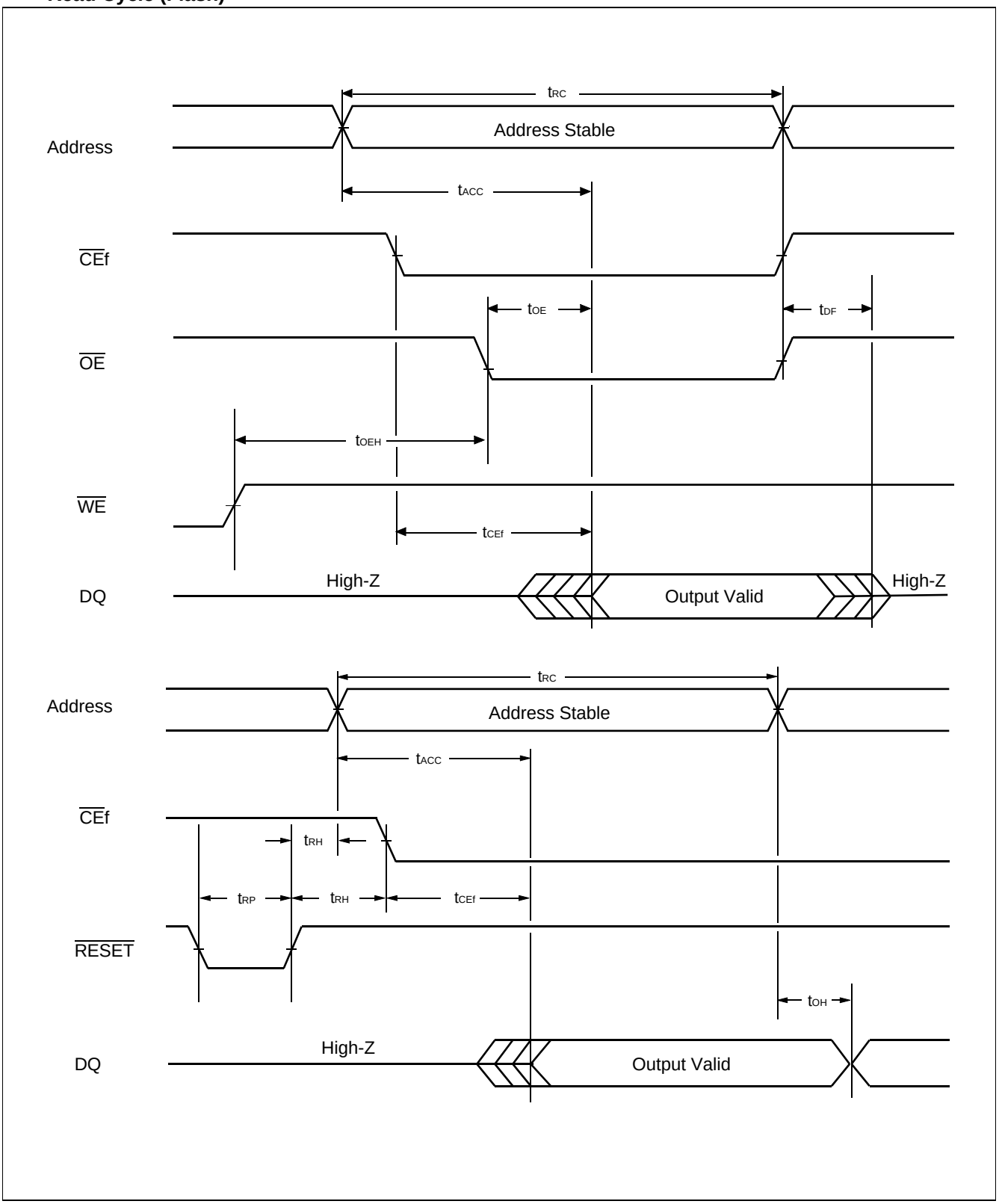
- **Write/Erase/Program Operations**

Parameter		Symbol		Value			Unit
		JEDEC	Standard	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	70	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	12	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	ns
Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	30	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
$\overline{CE}$f High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CE}$f Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$f Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	ns
$\overline{CE}$f Pulse Width		t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	25	—	—	ns
$\overline{CE}$f Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	ns
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
V_{CC}f Setup Time		—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID} *2		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ID} *2		—	t_{VACCR}	500	—	—	ns
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2		—	t_{OESP}	4	—	—	µs
$\overline{CE}$f Setup Time to $\overline{WE}$ Active *2		—	t_{CSP}	4	—	—	µs
Recover Time from RY/$\overline{BY}$		—	t_{RB}	—	—	—	ns
$\overline{RESET}$ Pulse Width		—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Level Period before Read		—	t_{RH}	200	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable		—	t_{EOE}	—	—	70	ns
Erase Time-Out Time		—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time		—	t_{SPD}	—	—	—	µs

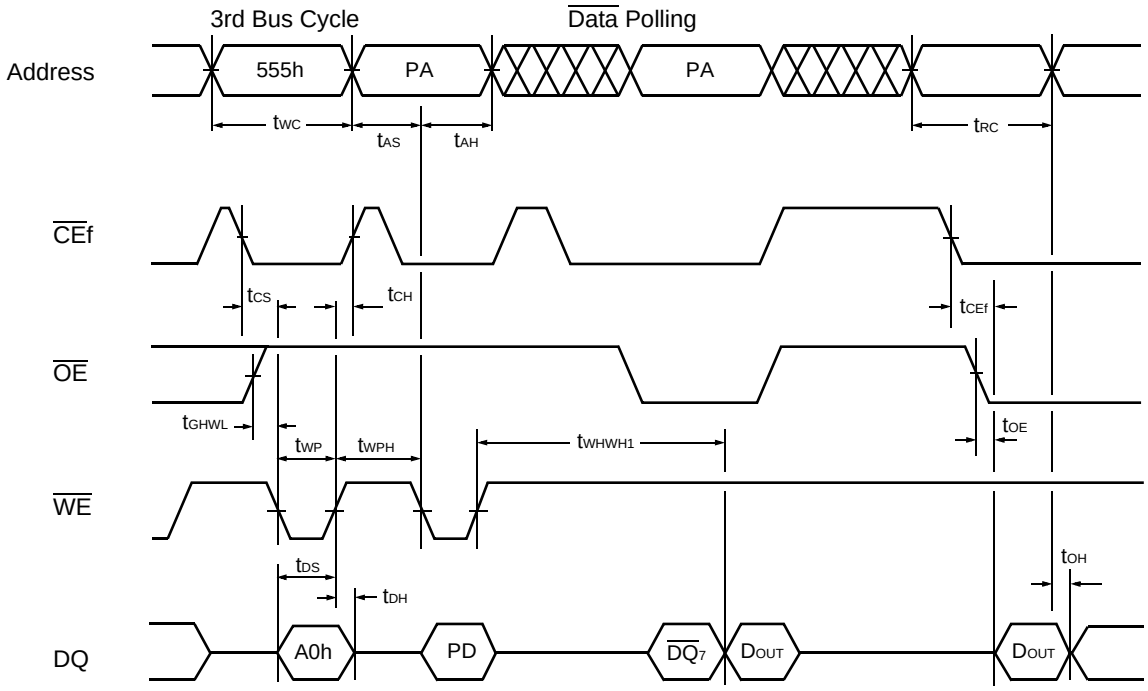
*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Group Protection operation.

- **Read Cycle (Flash)**

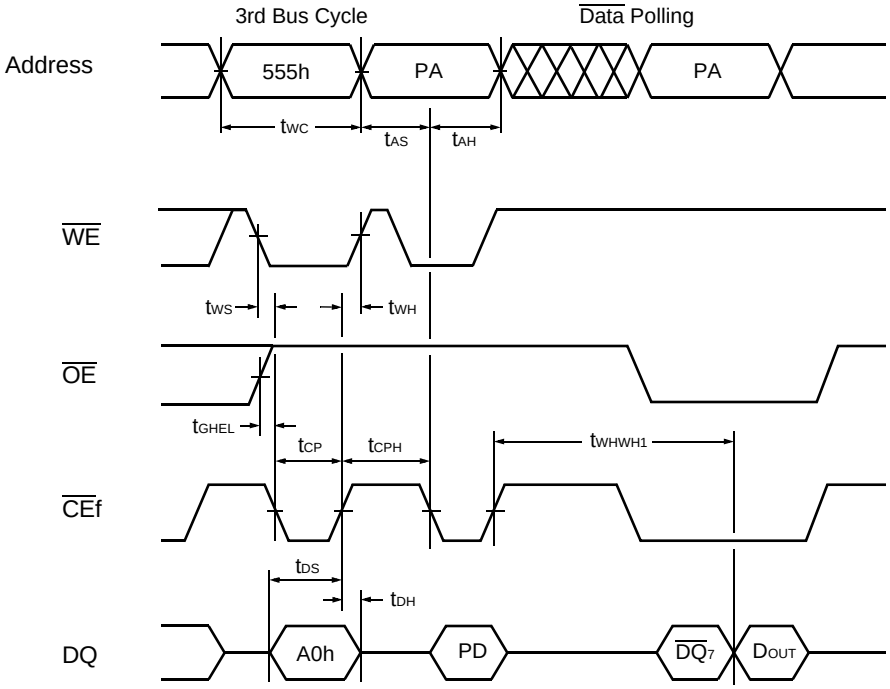


- **Write Cycle ($\overline{WE}$ control) (Flash)**



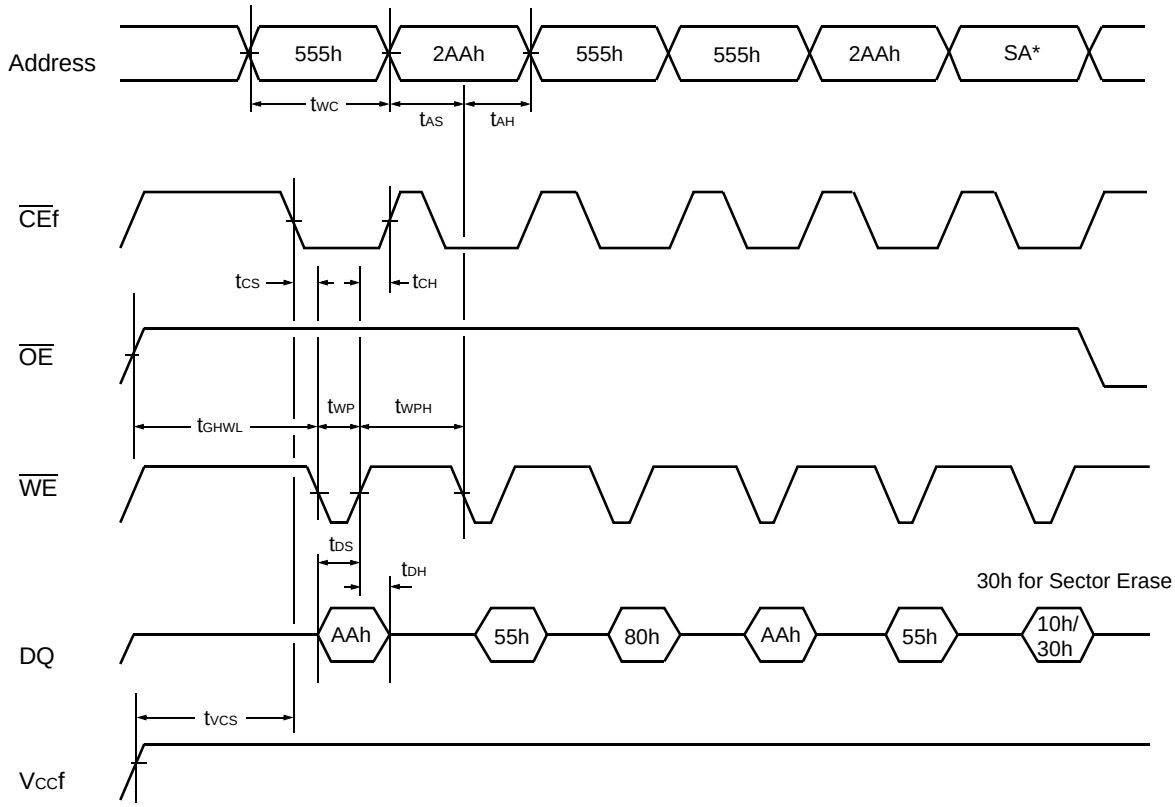
Notes :
- PA is address of the memory location to be programmed.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode.

- **Write Cycle ($\overline{CE}$f control) (Flash)**



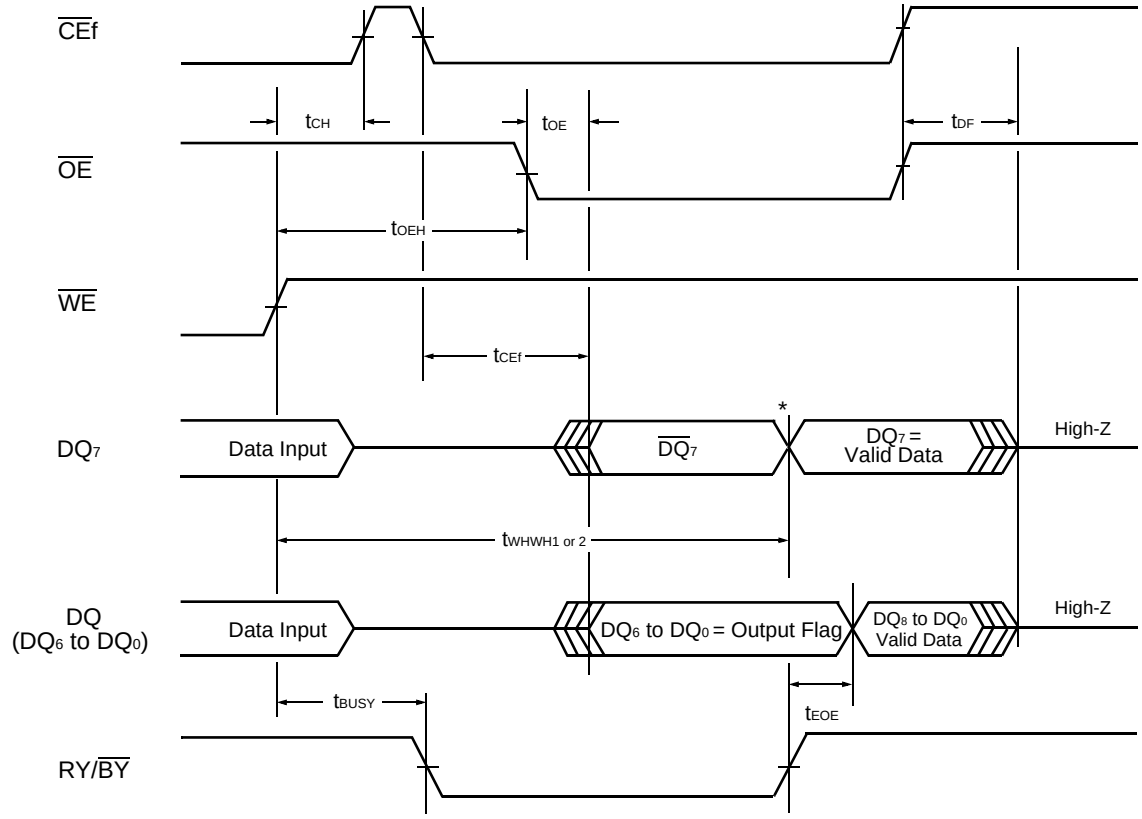
Notes :
- PA is address of the memory location to be programmed.
- $\overline{DQ}_7$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



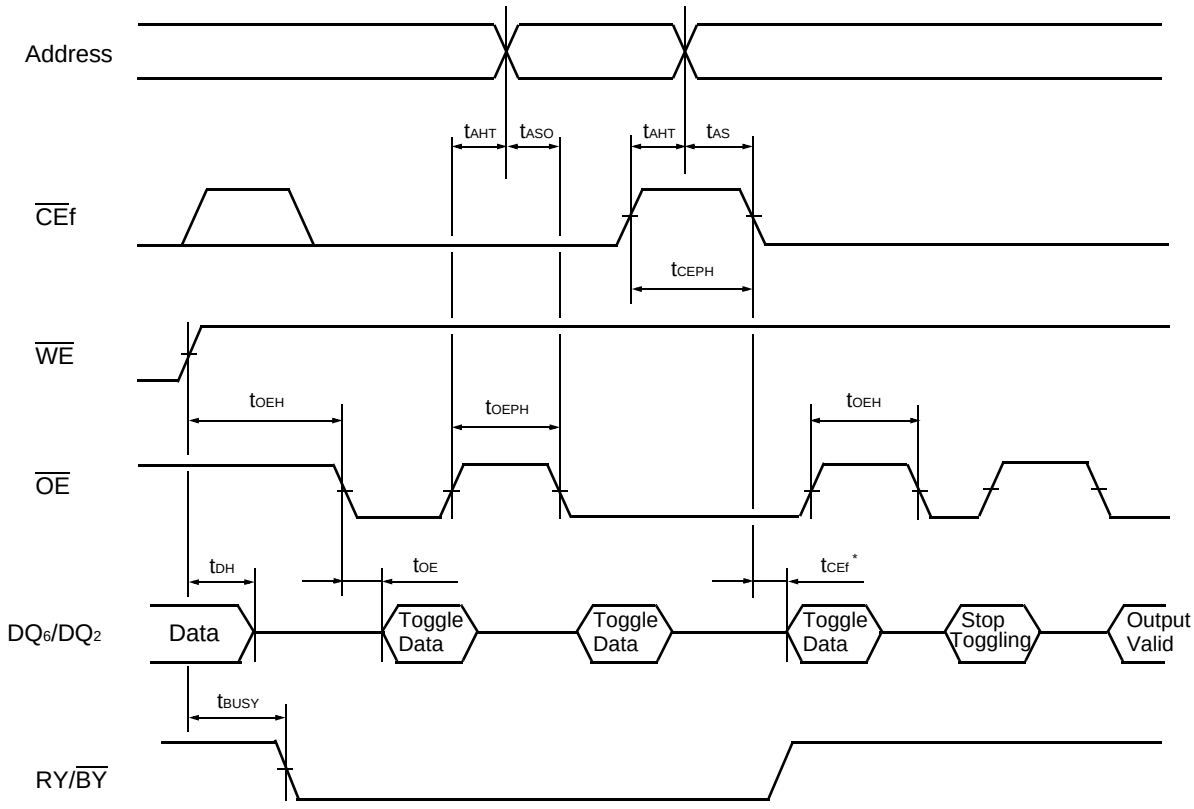
* : SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.
Note : These waveform are for the ×16 mode.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



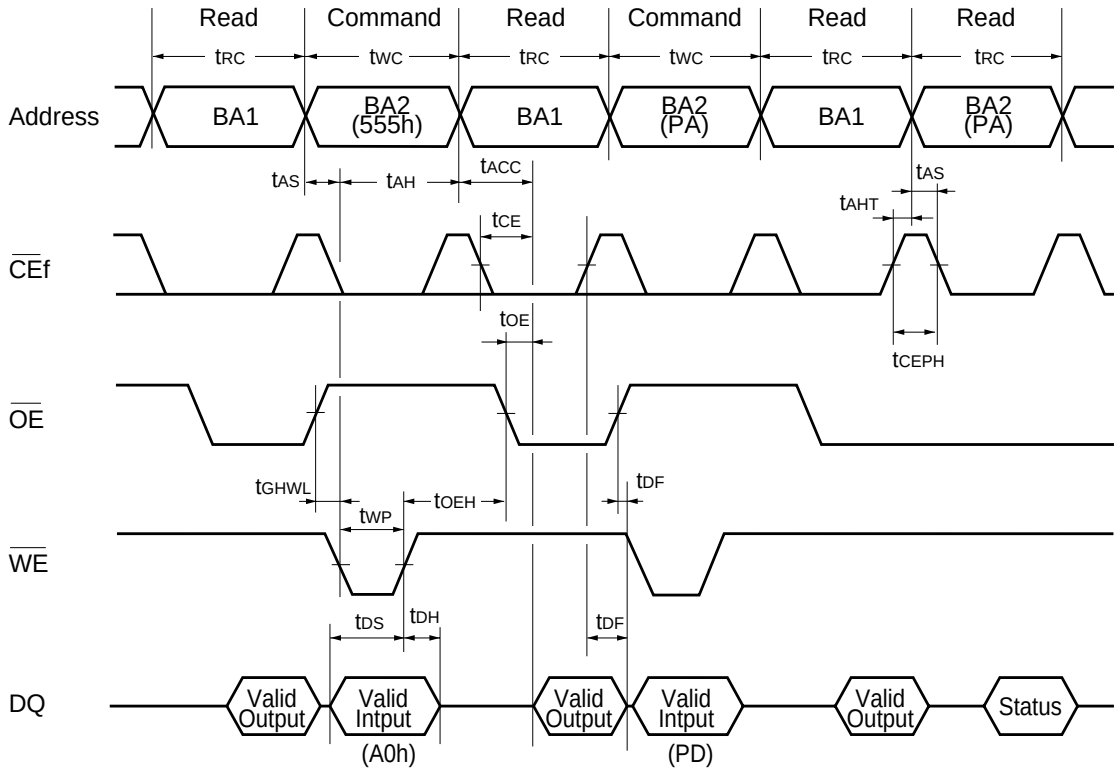
* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



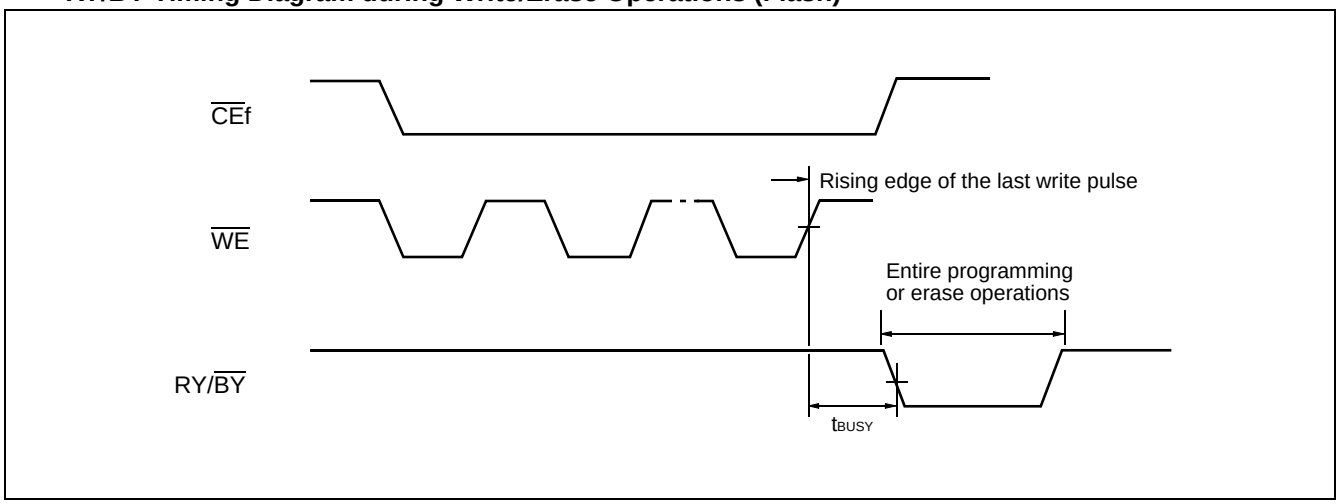
* : DQ_6 stops toggling (The device has completed the Embedded operation).

- **Back-to-back Read/Write Timing Diagram (Flash)**

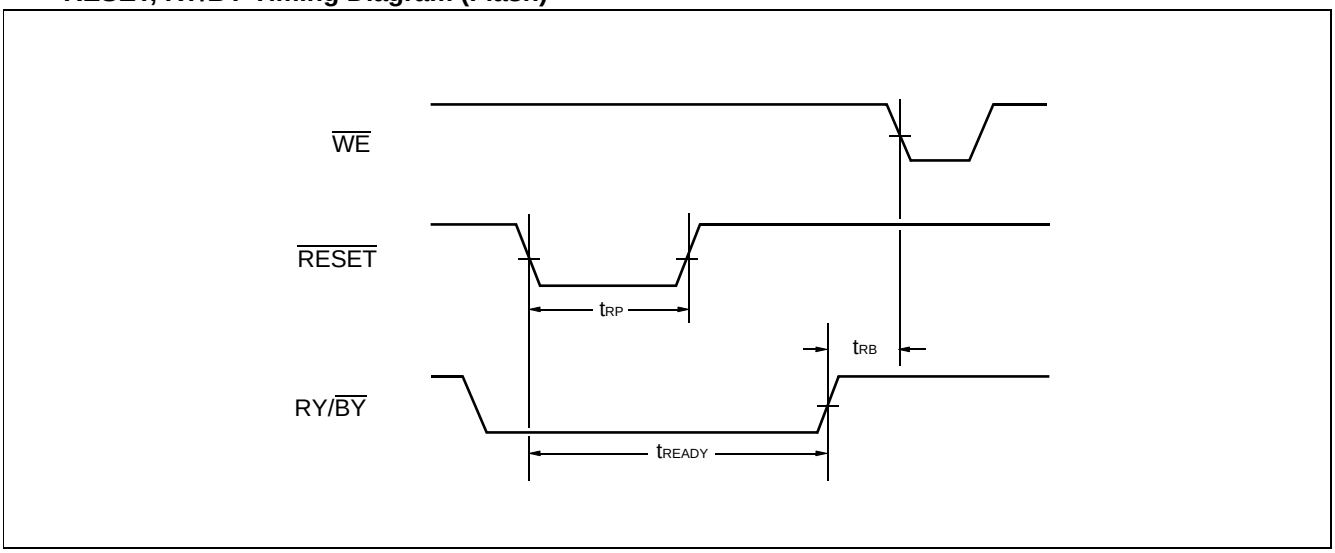


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

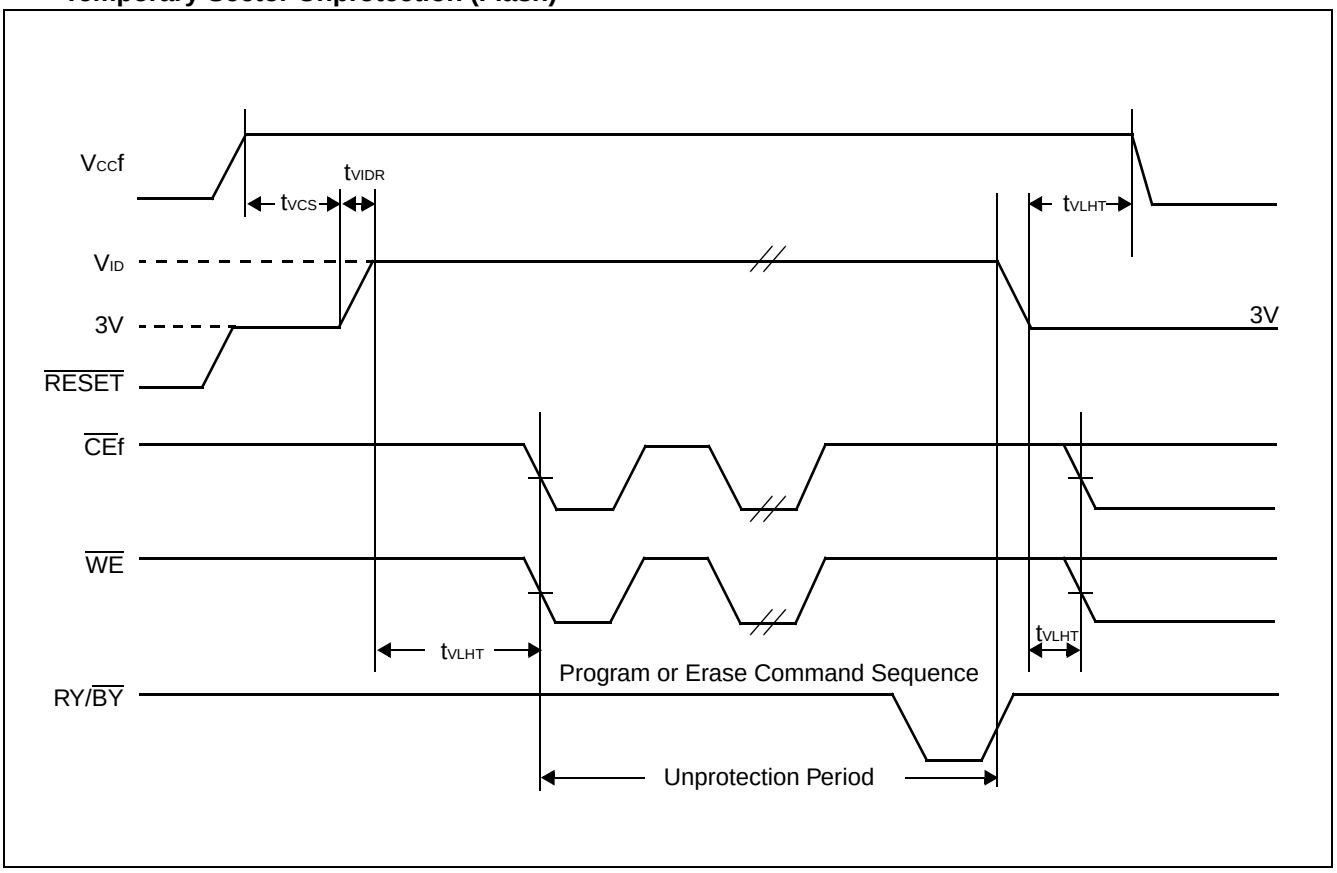
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



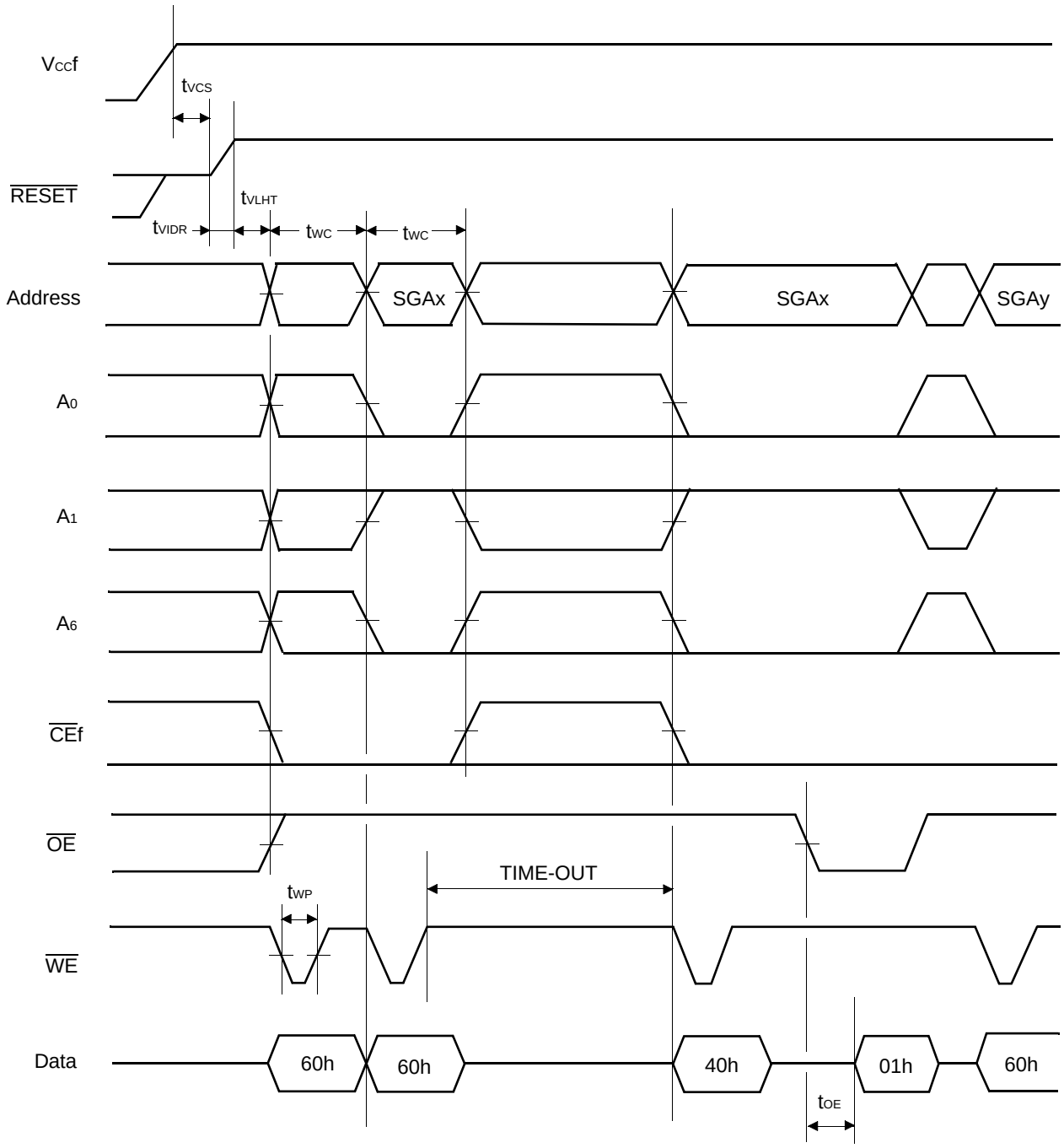
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



- **Temporary Sector Unprotection (Flash)**

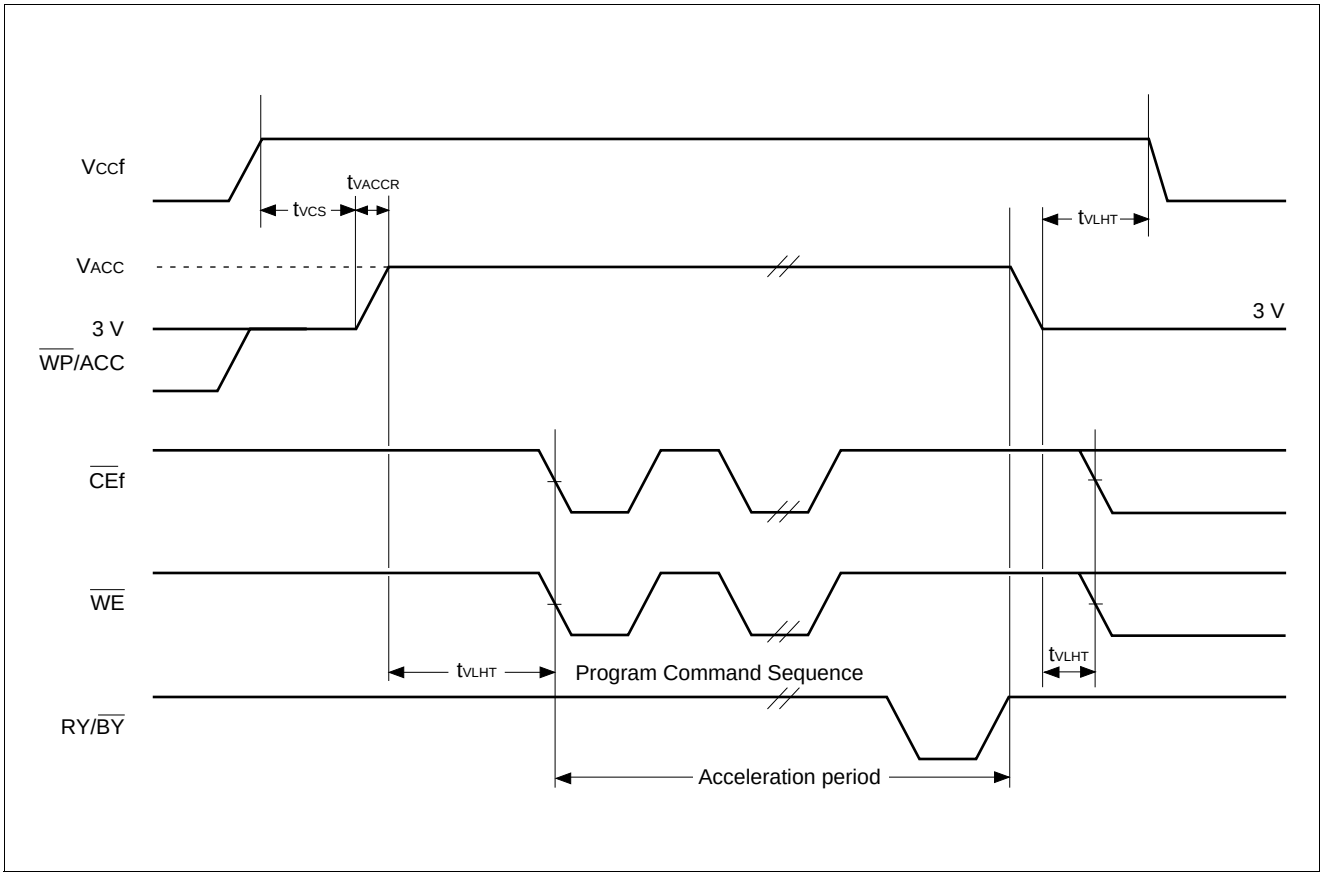


- **Extended Sector Group Protection (Flash)**



SGAx : Sector Group Address to be protected
SGAy : Next Group Sector Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min)

- **Accelerated Program (Flash)**



3. Erase and Programming Performance

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2.0	s	Excludes programming time prior to erasure
Word Programming Time	—	6.0	100	µs	Excludes system-level overhead
Chip Programming Time	—	12.6	50	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ 4 M SRAM for MCP

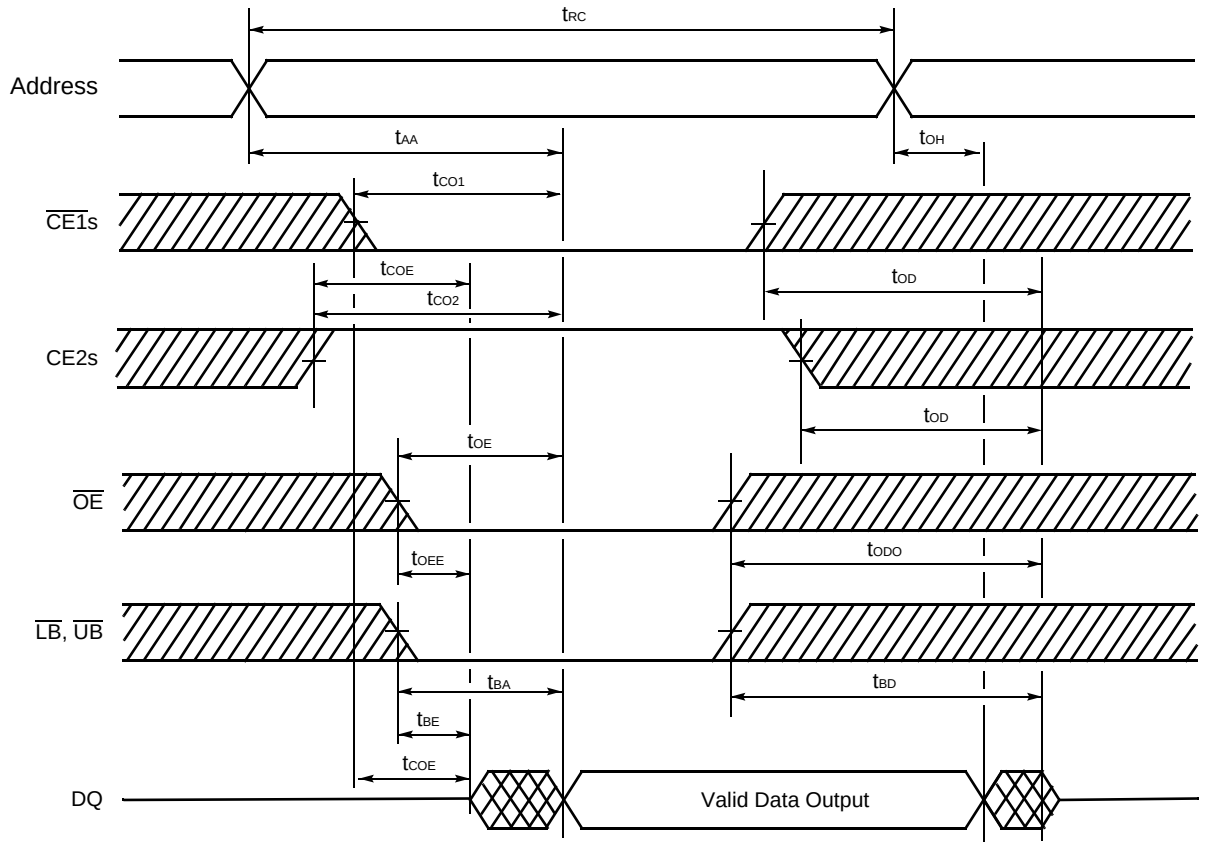
1. AC Characteristics

- **Read Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE1}$s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{UB}$, $\overline{LB}$ Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{UB}$, $\overline{LB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note: Test Conditions– Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to V_{CC}s
Timing measurement reference level
Input: 0.5×V_{CC}s
Output: 0.5×V_{CC}s

- **Read Cycle (SRAM)**

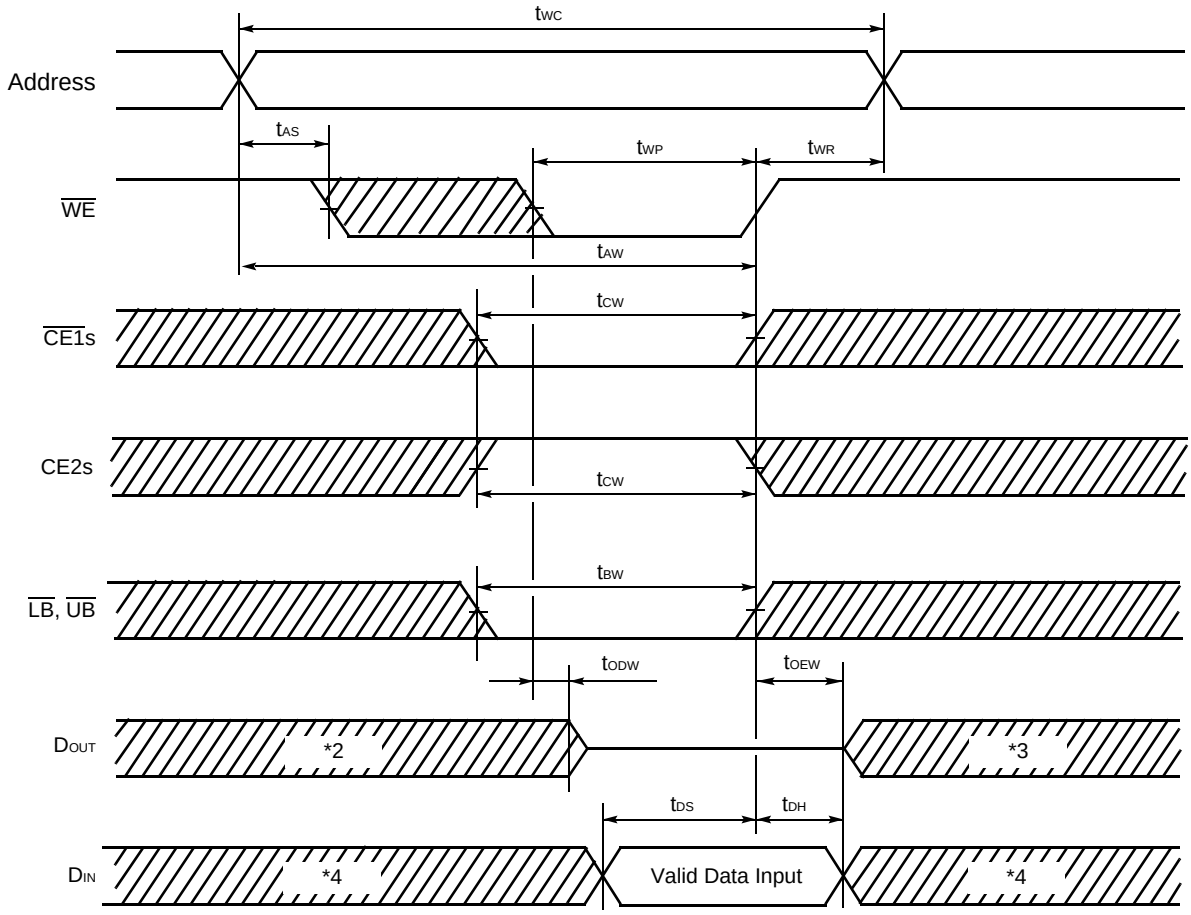


Note: $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	50	—	ns
Chip Enable to End of Write	t_{CW}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{UB}$, $\overline{LB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEW}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

- **Write Cycle *1 ($\overline{WE}$ control) (SRAM)**



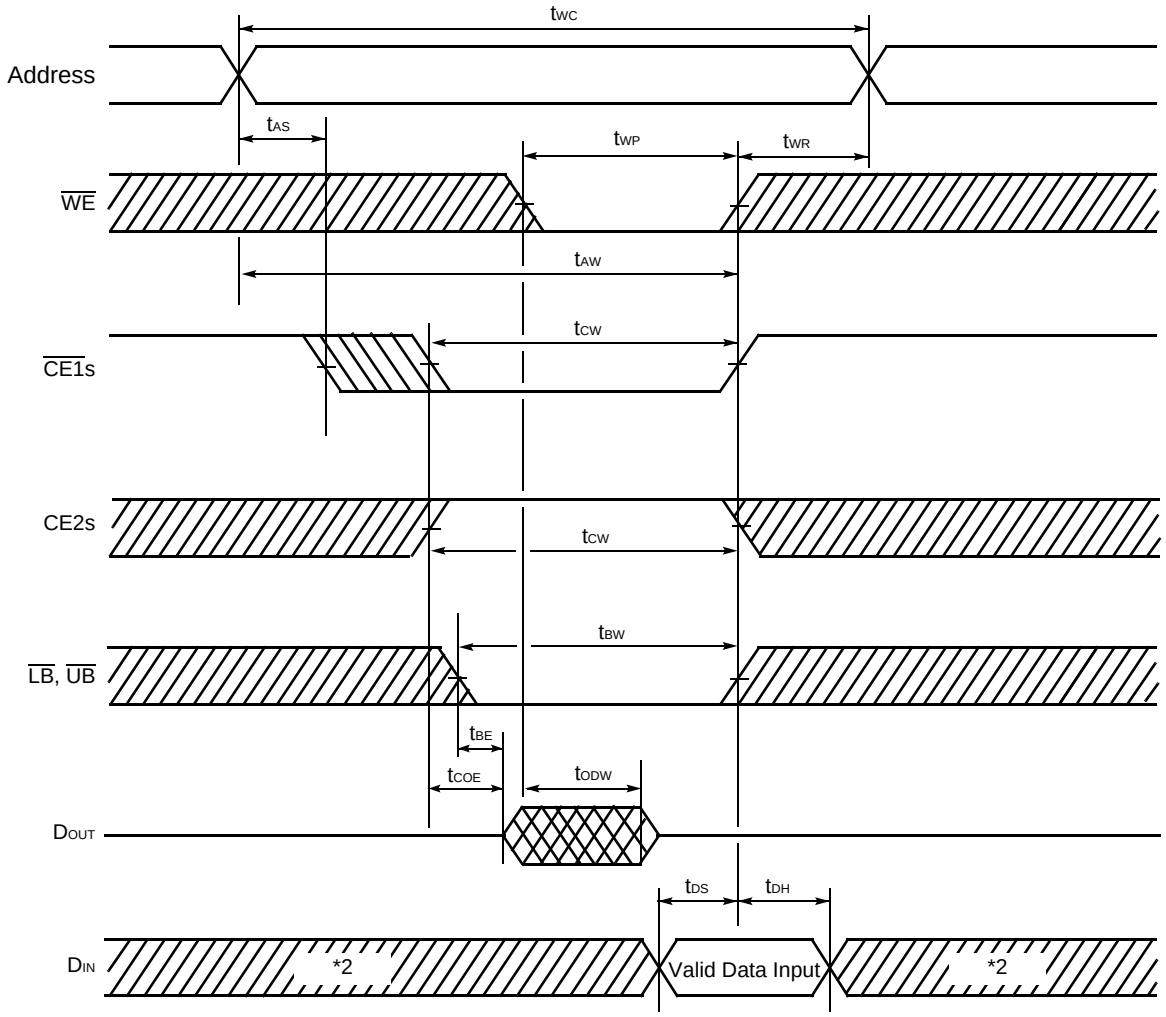
*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

*3 : If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.

*4 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

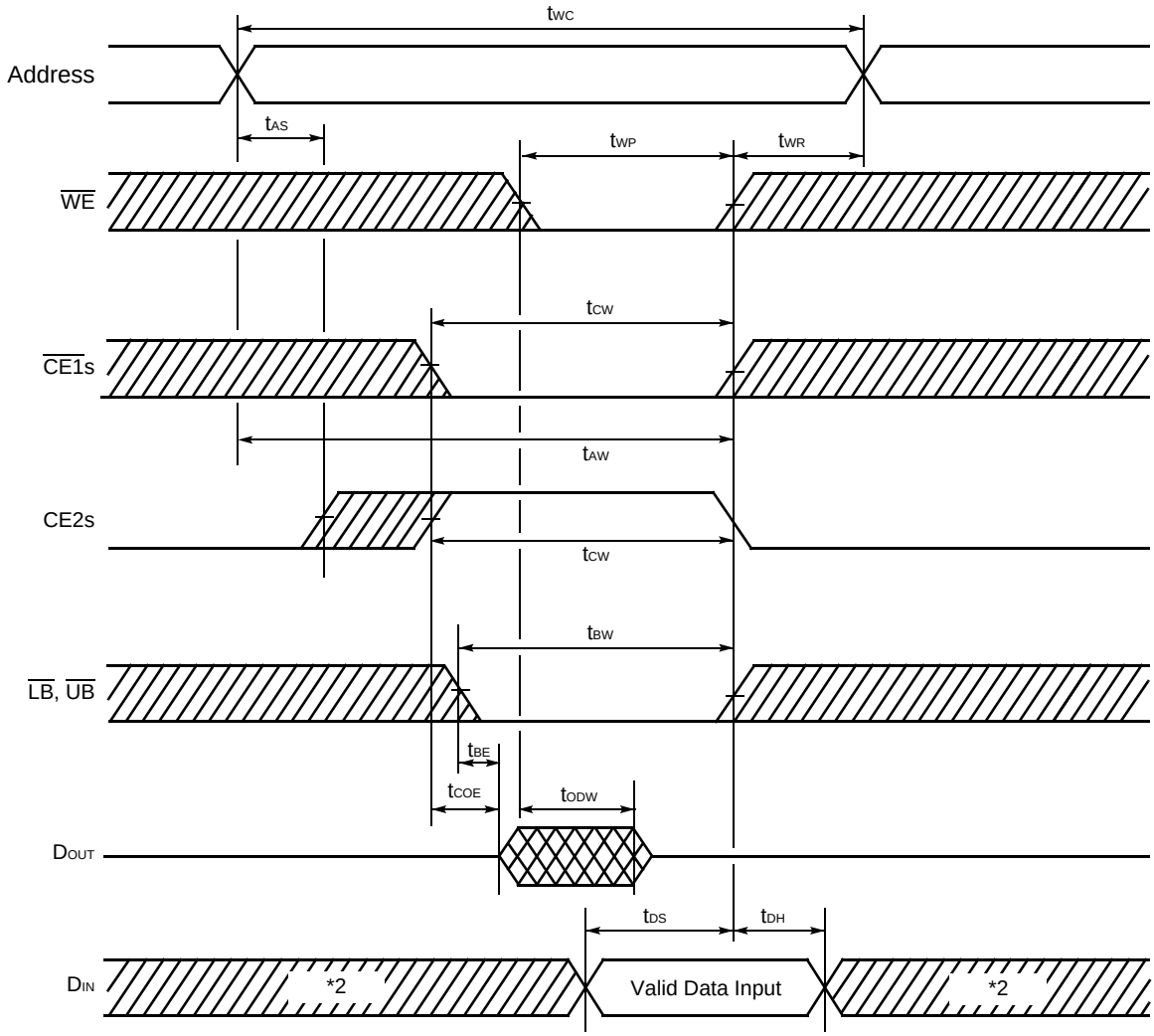
- **Write Cycle *1 ($\overline{CE1}$s control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

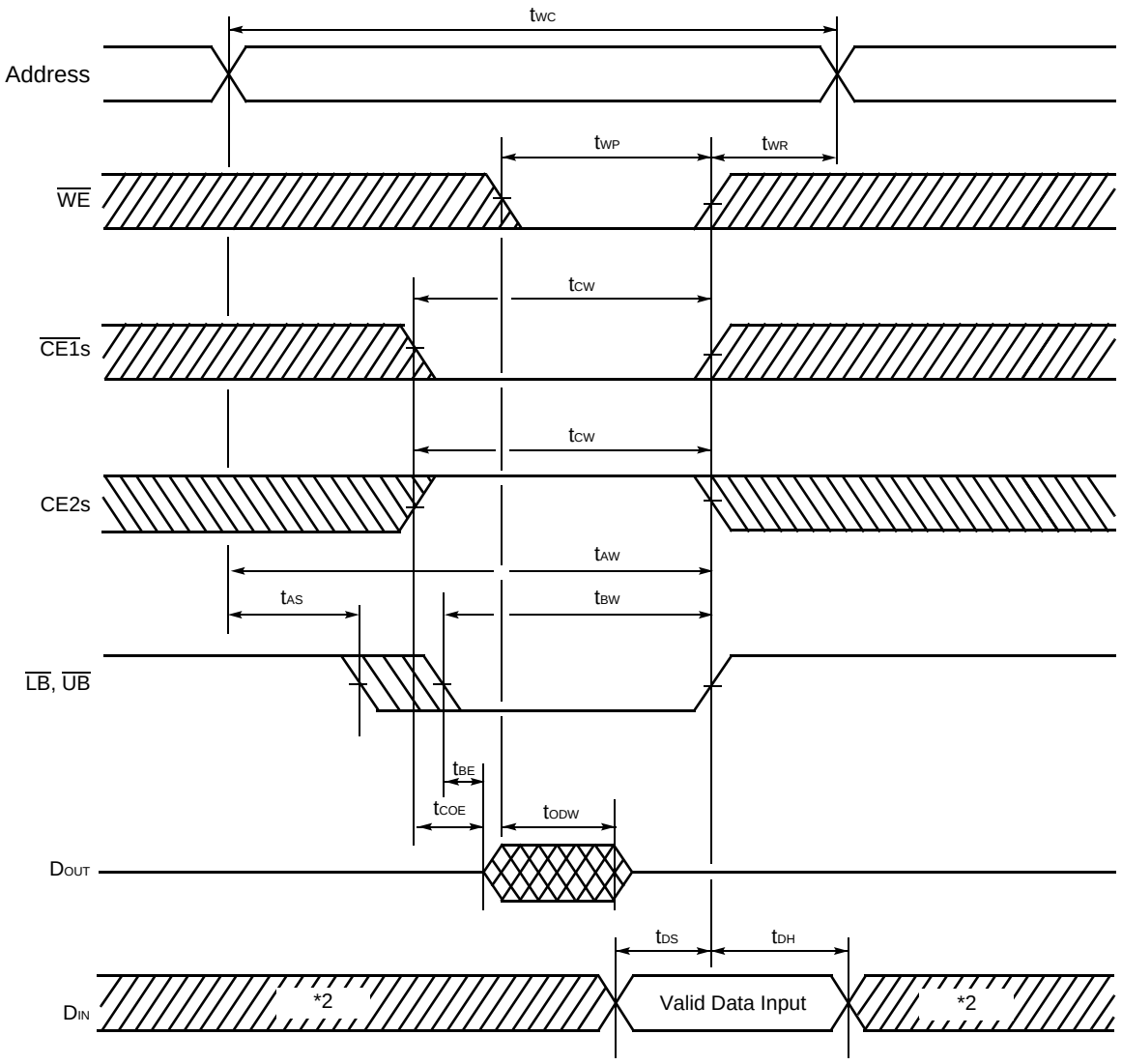
- **Write Cycle *1 (CE2s Control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle *1 ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



*1 : If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

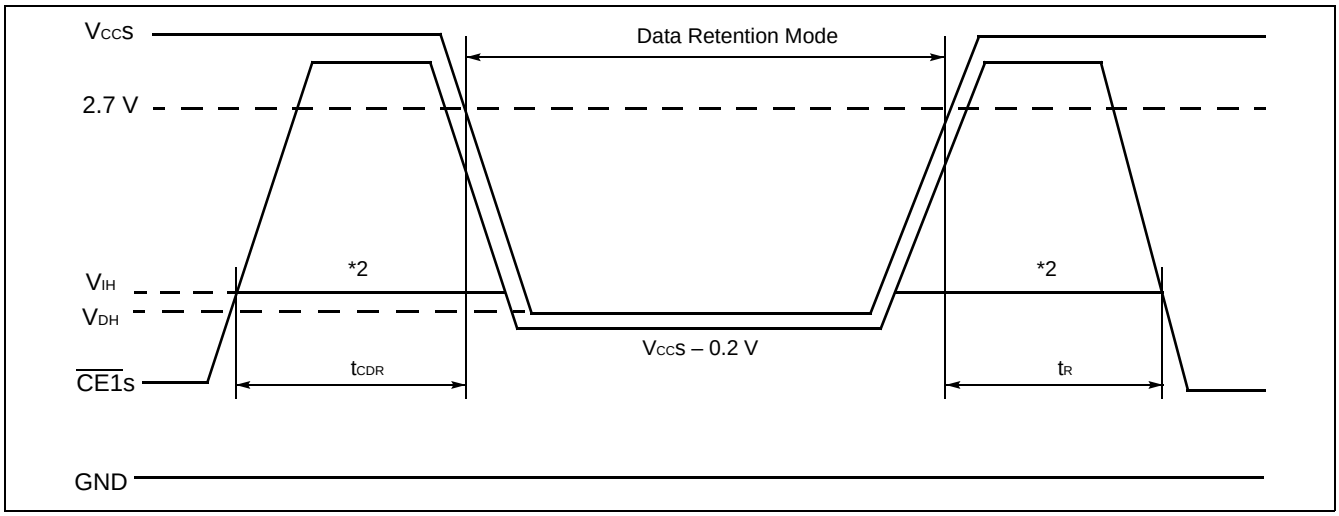
*2 : Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

2. Data Retention Characteristics (SRAM)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Data Retention Supply Voltage		V_{DH}	1.5	—	3.1	V
Standby Current	V_{DH} = 3.0 V	I_{DDS2}	—	—	10	µA
Chip Deselect to Data Retention Mode Time		t_{CDR}	0	—	—	ns
Recovery Time		t_R	t_{RC}	—	—	ns

Note : t_{RC}: Read cycle time

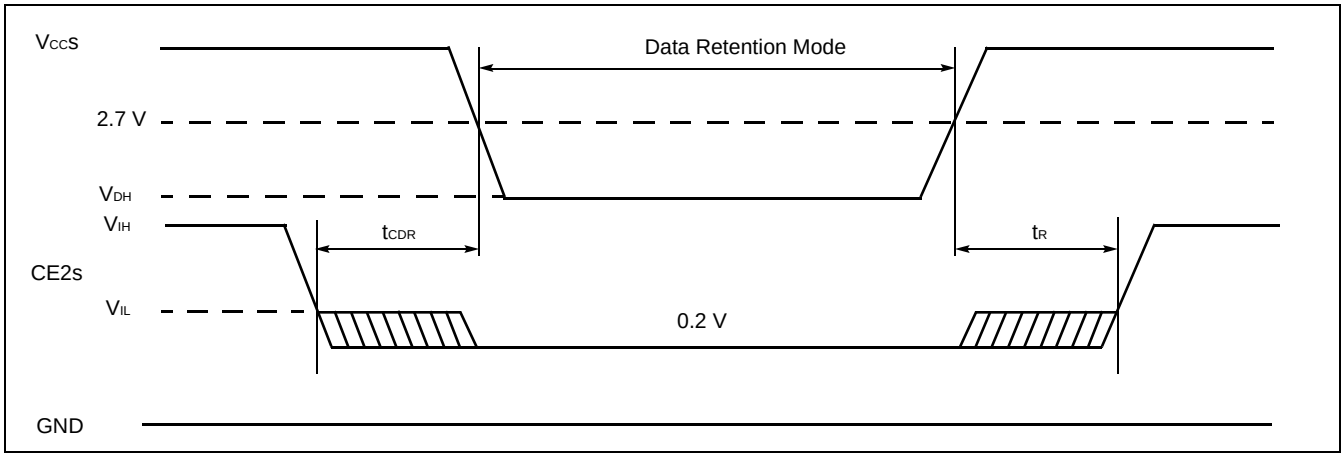
- **$\overline{CE1}$s Controlled Data Retention Mode *1**



*1 : In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs–0.2 V or Vss to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to Vccs+0.3 V.

*2 : When $\overline{CE1}$s is operating at the V_{IH} Min level, the standby current is given by I_{SB1}s during the transition of V_{CC}s from V_{CC}s Max to V_{IH} Min level.

- **CE2s Controlled Data Retention Mode ***



* : In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	11	14	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	12	16	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	14	16	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	21.5	26	pF

Note : Test conditions T_A = + 25°C, f = 1.0 MHz

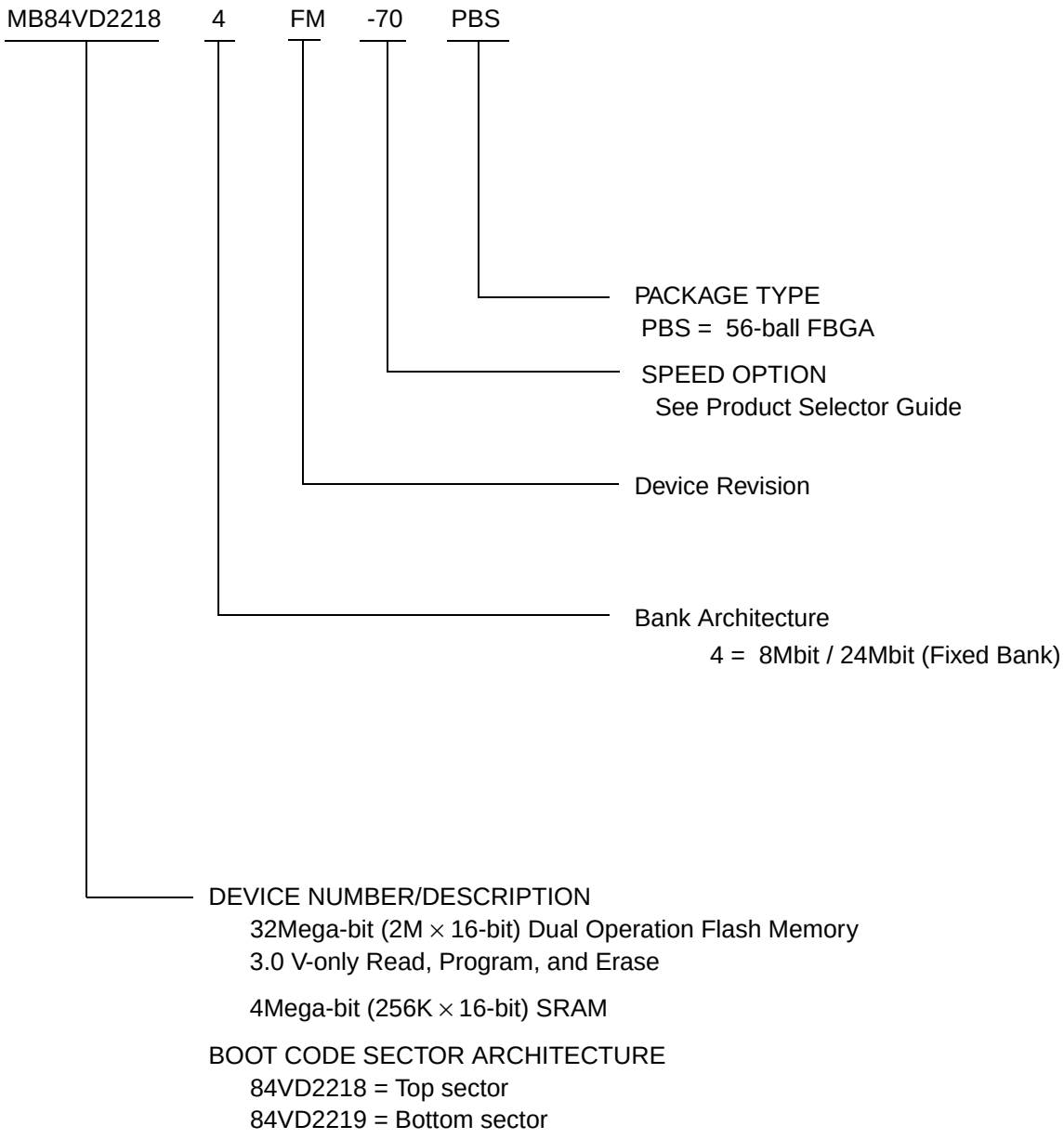
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

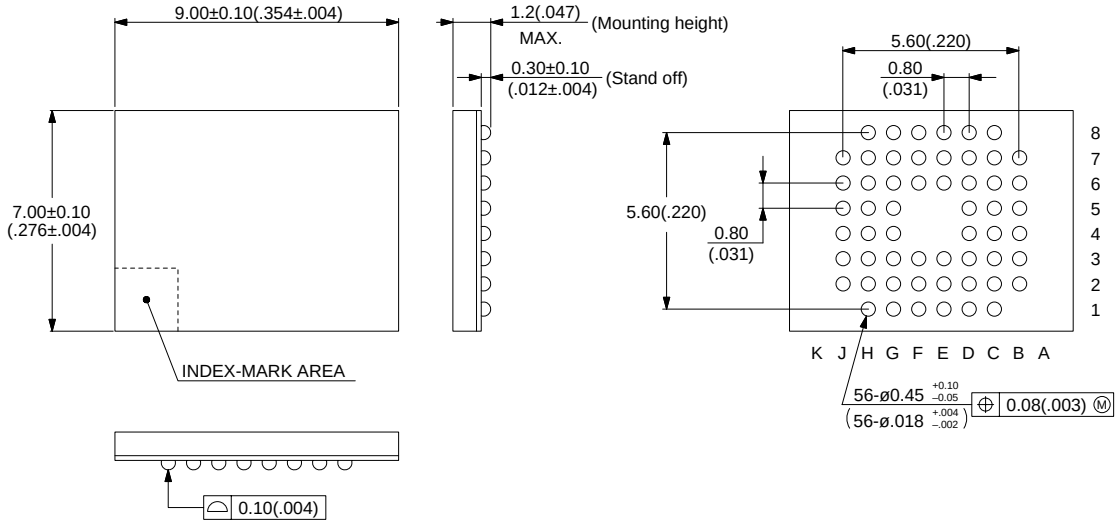
- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{RESET}$.
  Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.
- Without the high voltage (V_{ID}) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

56-ball plastic FBGA
(BGA-56P-M03)



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Dimensions in mm (inches)
Note: The values in parentheses are reference values.

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