

Double 4 mΩ high-side driver with analog CurrentSense for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V _{CC}	41 V
Operating voltage range	V _{CC}	4.5 to 27 V
Max On-State resistance (per ch.)	R _{ON}	4 mΩ
Current limitation (typ)	I _{LIMH}	100 A
Off state supply current	I _S	2 μA ⁽¹⁾

1. Typical value with all loads connected

- AEC-Q100 qualified
- General
 - Inrush current active management by power limitation
 - Very low stand-by current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
- Diagnostic functions
 - Proportional load current sense
 - Current sense disable
 - Thermal shutdown indication
- Protection
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Thermal shutdown
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}



- Reverse battery protection with self switch-on of the PowerMOS
- Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

Description

The device is a double channel high-side driver manufactured using STMicroelectronics proprietary VIPower® M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp and load dump protection circuit protect the devices against transients on the V_{CC} pin.

The device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is high impedance.

Output current limitation protects the devices in overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as a fault condition disappears.

Contents

1	Block diagram and pin configurations	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	15
3	Application information	18
3.1	MCU I/Os protection	18
3.2	Load dump protection	18
3.3	Maximum demagnetization energy (VCC = 13.5 V)	19
4	Package and PC board thermal data	20
4.1	MultiPowerSO-30 thermal data	20
5	Package information	23
5.1	MultiPowerSO-30 package information	23
5.2	MultiPowerSO-30 packing information	24
6	Order codes	26
7	Revision history	27

List of tables

Table 1.	Pin functions	5
Table 2.	Suggested connections for unused and n.c. pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	8
Table 5.	Power section	9
Table 6.	Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$)	9
Table 7.	Logic input	10
Table 8.	Protection and diagnostics	10
Table 9.	CurrentSense ($8\text{ V} < V_{CC} < 16\text{ V}$)	11
Table 10.	Truth table	12
Table 11.	Electrical transient requirements (part 1)	13
Table 12.	Electrical transient requirements (part 2)	13
Table 13.	Electrical transient requirements (part 3)	13
Table 14.	Thermal parameters for MultiPowerSO-30	22
Table 15.	MultiPowerSO-30 mechanical data	23
Table 16.	Device summary	26
Table 17.	Document revision history	27

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (not to scale)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Current sense delay characteristics	11
Figure 5.	Switching characteristics	12
Figure 6.	Waveforms	14
Figure 7.	Off state output current	15
Figure 8.	High level input current	15
Figure 9.	Input clamp voltage	15
Figure 10.	Input low level	15
Figure 11.	Input high level	15
Figure 12.	Input hysteresis voltage	15
Figure 13.	On state resistance vs. T_{case}	16
Figure 14.	On state resistance vs. V_{CC}	16
Figure 15.	Undervoltage shutdown	16
Figure 16.	Turn-On voltage slope	16
Figure 17.	I_{LIMH} vs. T_{case}	16
Figure 18.	Turn-Off voltage slope	16
Figure 19.	CS_DIS high level voltage	17
Figure 20.	CS_DIS clamp voltage	17
Figure 21.	CS_DIS low level voltage	17
Figure 22.	Application schematic	18
Figure 23.	Maximum turn off current versus inductance	19
Figure 24.	MultiPowerSO-30 PC board	20
Figure 25.	$R_{thj-amb}$ vs. PCB copper area in open box free air condition (one channel ON).	20
Figure 26.	MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)	21
Figure 27.	Thermal fitting model of a double channel HSD in MultiPowerSO-30	21
Figure 28.	MultiPowerSO-30 package outline	23
Figure 29.	MultiPowerSO-30 tape and reel shipment (suffix "TR")	25

1 Block diagram and pin configurations

Figure 1. Block diagram

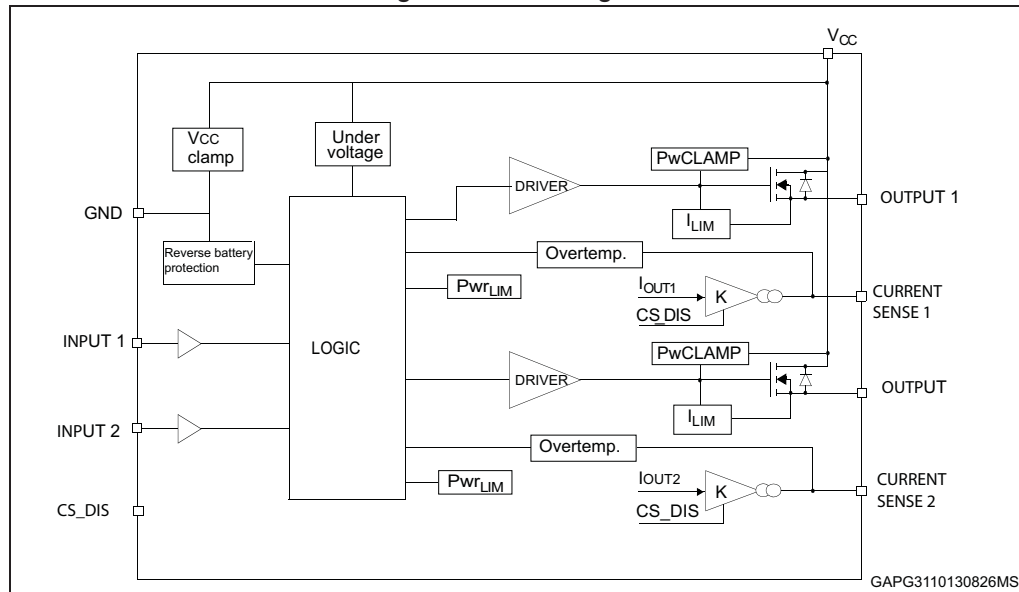


Table 1. Pin functions

Name	Function
VCC	Battery connection
OUTPUT1,2	Power output
GND	Ground connection
INPUT1,2	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE1,2	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pins

Figure 2. Configuration diagram (not to scale)

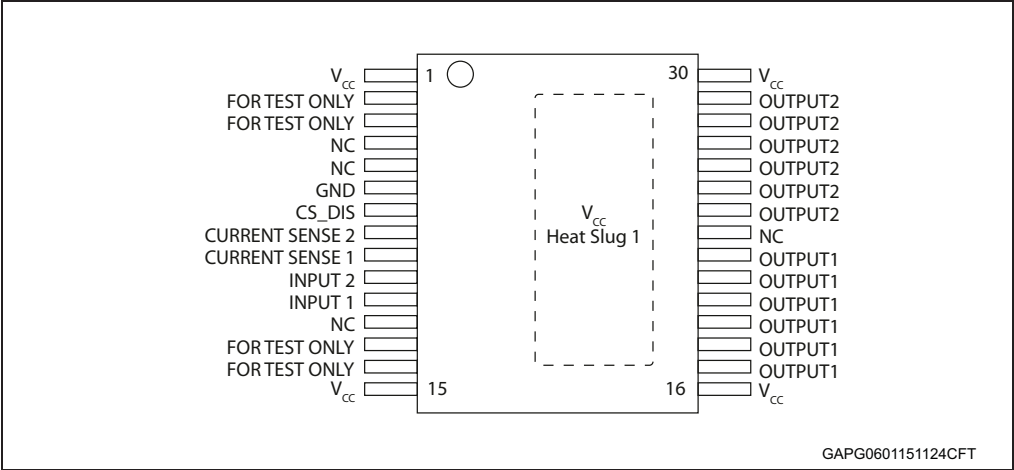


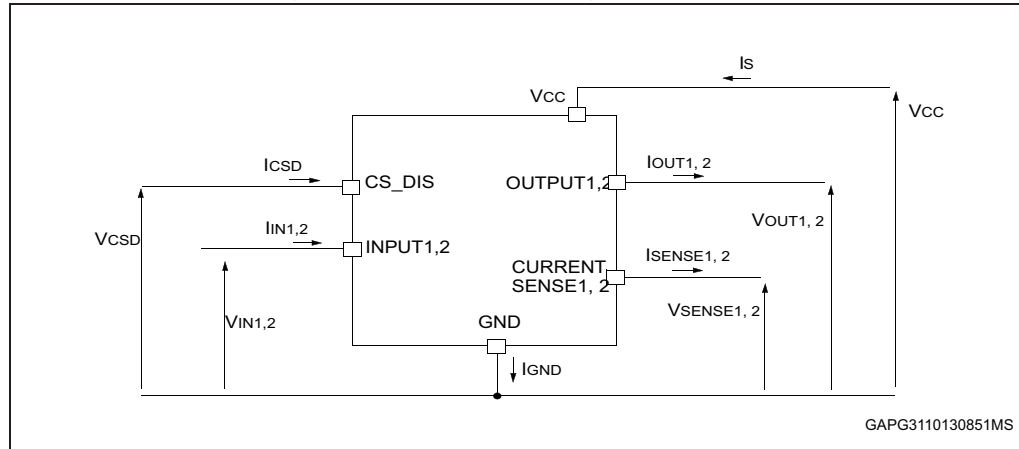
Table 2. Suggested connections for unused and n.c. pins

Connection / pin	Current Sense	N.C.	Output	Input	CS_DIS	For test only
Floating	N.R. ⁽¹⁾	X	X	X	X	X
To ground	Through 1 kΩ resistor	X	N.R.	Through 10 kΩ resistor	Through 10 kΩ resistor	N.R.

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	27	V
V_{CCPK}	Transient supply voltage ($T < 400$ ms, $R_{load} > 0.5 \Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	70	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSense}	Current sense maximum voltage ($V_{CC} > 0$ V)	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.3$ mH; $R_L = 0 \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}(typ.)$)	342	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5$ k Ω ; $C = 100$ pF)	2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	0.35	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	58 ⁽¹⁾	°C/W

1. PCB FR4 area 58 mmX58 mm, PCB thickness 2 mm, Cu thickness 35 μ m, minimum pad layout.

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 24\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	27	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 15\text{ A}$; $T_j = 25\text{ °C}$			4	mΩ
		$I_{OUT} = 15\text{ A}$; $T_j = 150\text{ °C}$			8	mΩ
		$I_{OUT} = 15\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ °C}$			6	mΩ
$R_{ON REV}$	R_{dson} in reverse battery condition	$V_{CC} = -13\text{ V}$; $I_{OUT} = -15\text{ A}$; $T_j = 25\text{ °C}$			4	mΩ
V_{clamp}	V_{CC} clamp voltage	$I_{CC} = 20\text{ mA}$; $I_{OUT1,2} = 0\text{ A}$	41	46	52	V
I_S	Supply current	Off state; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 ⁽²⁾	5 ⁽²⁾	μA
		On state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		3.5	6	mA
$I_{L(off)}$	Off-state output current ⁽¹⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		5	μA

1. For each channel.

2. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 0.87\text{ Ω}$ (see Figure 5)	—	25	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 0.87\text{ Ω}$ (see Figure 5)	—	35	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 0.87\text{ Ω}$	—	See Figure 16	—	V/μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 0.87\text{ Ω}$	—	See Figure 16	—	V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 0.87\text{ Ω}$ (see Figure 5)	—	5.4	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 0.87\text{ Ω}$ (see Figure 5)	—	2.3	—	mJ

Table 7. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL1,2}$	Input low level voltage				0.9	V
$I_{IL1,2}$	Low level input current	$V_{IN}=0.9V$	1			μA
$V_{IH1,2}$	Input high level voltage		2.1			V
$I_{IH1,2}$	High level input current	$V_{IN}=2.1V$			10	μA
$V_{I(hyst)1,2}$	Input hysteresis voltage		0.25			V
$V_{ICL1,2}$	Input clamp voltage	$I_{IN} = 1 \text{ mA}$	5.5		7	V
		$I_{IN} = -1 \text{ mA}$		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9 \text{ V}$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1 \text{ V}$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1 \text{ mA}$	5.5		7	V
		$I_{CSD} = -1 \text{ mA}$		-0.7		V

Table 8. Protection and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	$V_{CC} = 13 \text{ V}$	70	100	140	A
		$5 \text{ V} < V_{CC} < 24 \text{ V}$			140	A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13 \text{ V}; T_R < T_J < T_{TSD}$		40		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS}+1$	$T_{RS}+5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD}-T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2 \text{ A}; V_{IN} = 0;$ $L = 6 \text{ mH}$	$V_{CC}-27$	$V_{CC}-30$	$V_{CC}-33$	V

Note: To ensure long term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. CurrentSense (8 V < V_{CC} < 16 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 15 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C T _j = 25 °C to 150 °C	11530 12730	16000 16000	19340 19270	
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 30 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C T _j = 25 °C to 150 °C	13430 14500	16150 16150	17880 17880	
I _{SENSE0}	Analog sense current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{CSD} = 5 V; V _{IN} = 0 V; T _j = -40 °C to 150 °C	0		5	μA
		I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{CSD} = 0 V; V _{IN} = 5 V; T _j = -40 °C to 150 °C	0		400	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 45 A; V _{CSD} = 0 V; R _{SENSE} = 3.9 kΩ	5			V
V _{SENSEH}	Analog sense output voltage in overtemperature condition	V _{CC} = 13 V; R _{SENSE} = 3.9 kΩ		9		V
I _{SENSEH}	Analog sense output current in overtemperature condition	V _{CC} = 13 V; V _{SENSE} = 5 V		8		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} < 4 V; 5 A < I _{OUT} < 30 A; I _{SENSE} = 90% of I _{SENSE} max (see Figure 4)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} < 4 V; 5 A < I _{OUT} < 30 A; I _{SENSE} = 10% of I _{SENSE} max (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V; 5 A < I _{OUT} < 30 A; I _{SENSE} = 90% of I _{SENSE} max (see Figure 4)		270	600	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4 V; 5 A < I _{OUT} < 30 A; I _{SENSE} = 10% of I _{SENSE} max (see Figure 4)		100	250	μs

Figure 4. Current sense delay characteristics

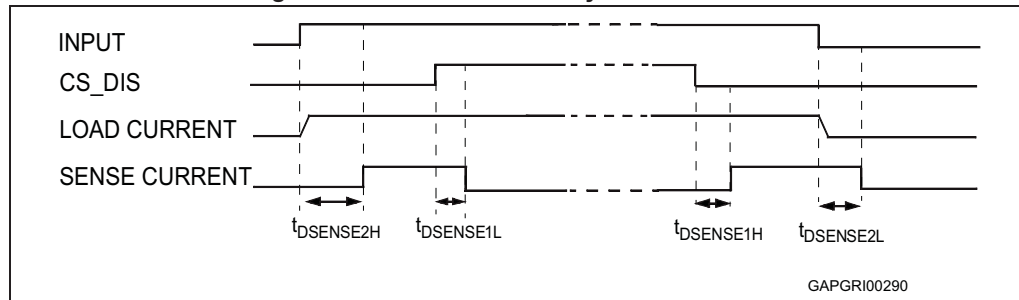


Table 10. Truth table

Conditions	INPUTn	OUTPUTn	SENSEn ($V_{CSD} = 0V$) ⁽¹⁾ (see Figure 3)
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ($R_{SC} \leq 10\text{ m}\Omega$)	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If V_{CSD} is high, the SENSE output is at a high impedance. Its potential depends on leakage currents and the external circuit.

Figure 5. Switching characteristics

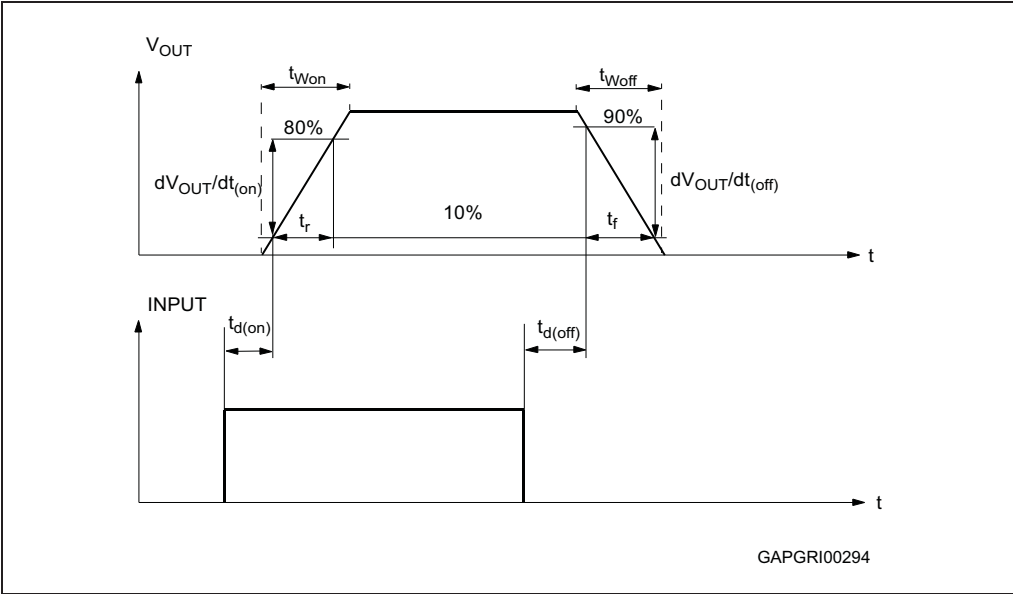


Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 12. Electrical transient requirements (part 2)

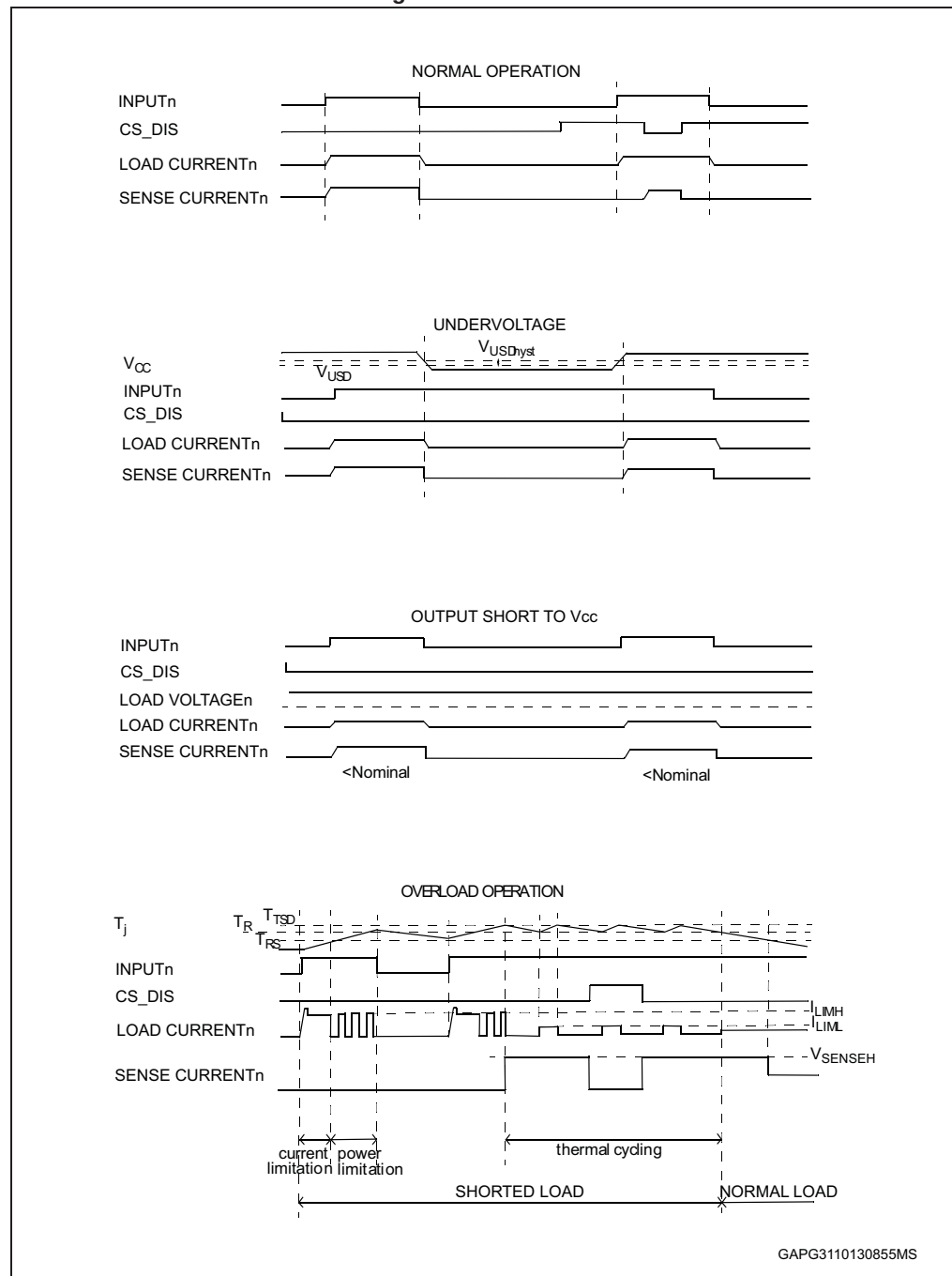
ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ^{(2) (3)}	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3](#): *Absolute maximum ratings*.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off state output current

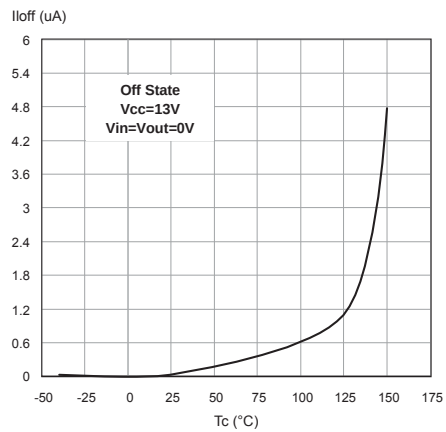


Figure 8. High level input current

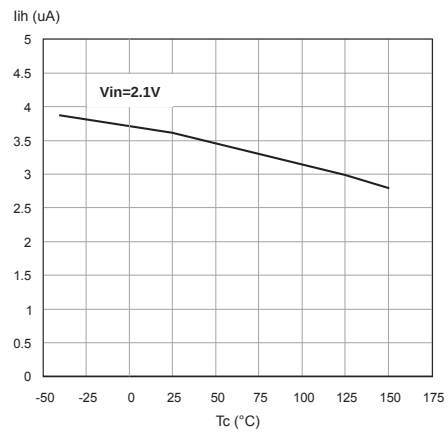


Figure 9. Input clamp voltage

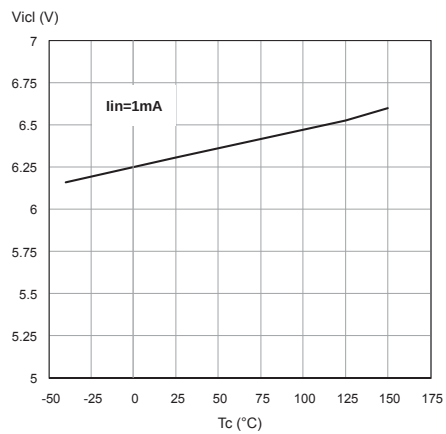


Figure 10. Input low level

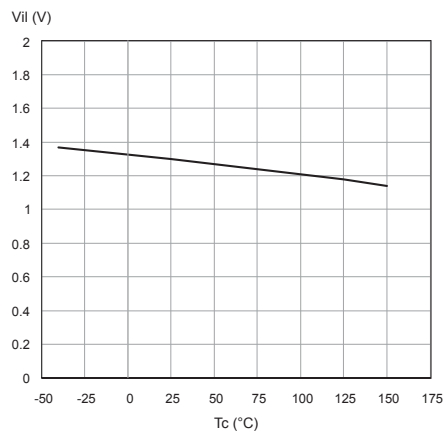


Figure 11. Input high level

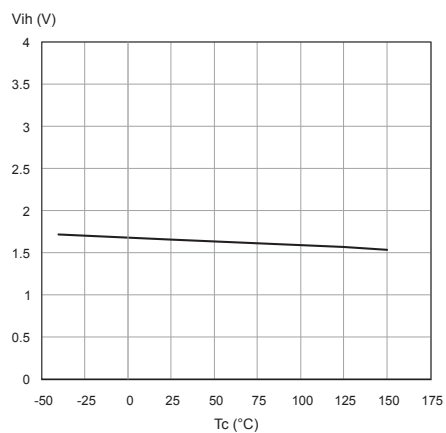


Figure 12. Input hysteresis voltage

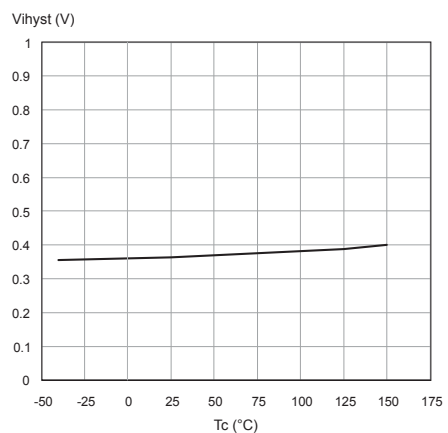


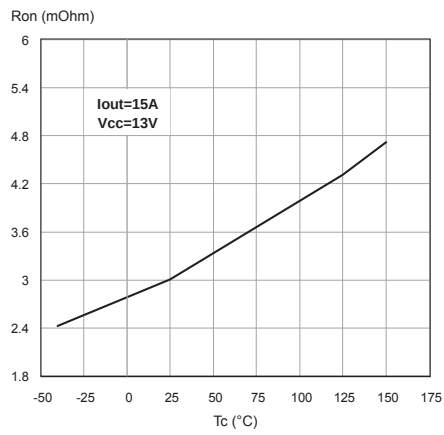
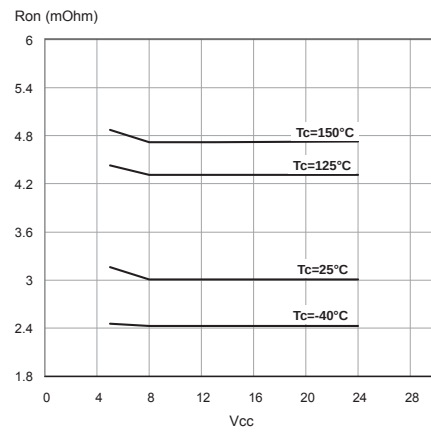
Figure 13. On state resistance vs. T_{case} Figure 14. On state resistance vs. V_{CC} 

Figure 15. Undervoltage shutdown

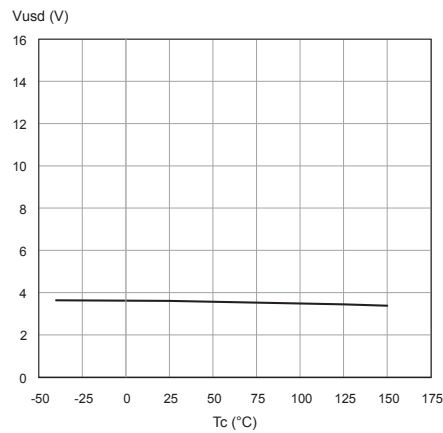


Figure 16. Turn-On voltage slope

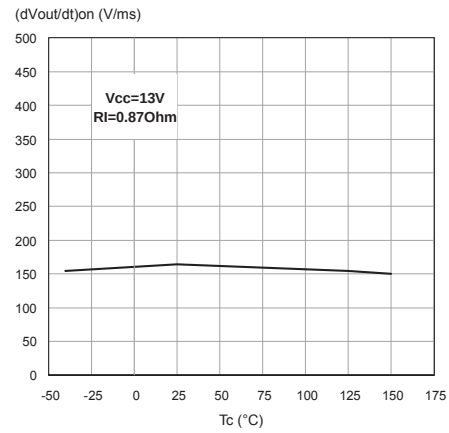
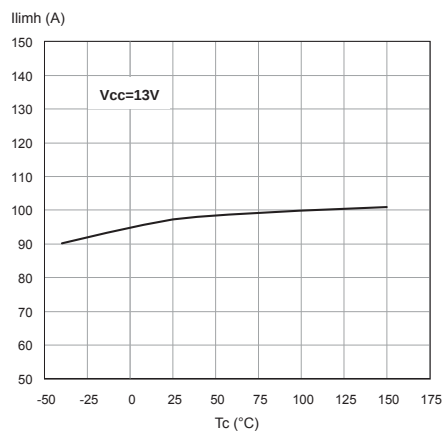
Figure 17. I_{LIMH} vs. T_{case} 

Figure 18. Turn-Off voltage slope

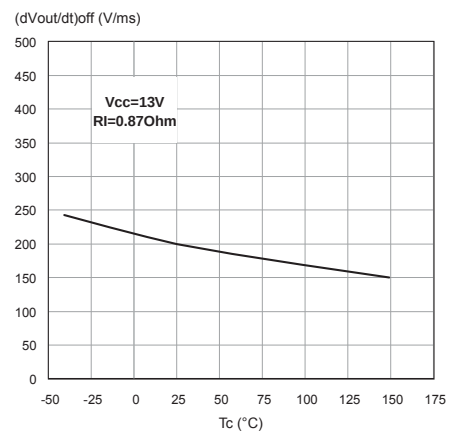


Figure 19. CS_DIS high level voltage

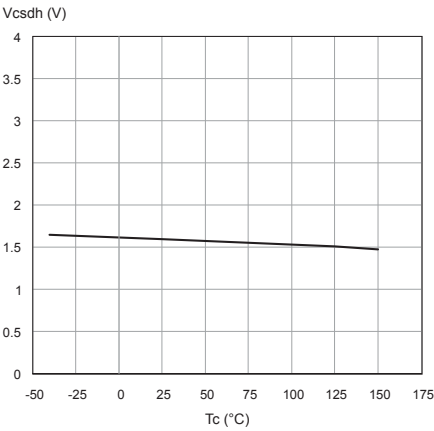


Figure 20. CS_DIS clamp voltage

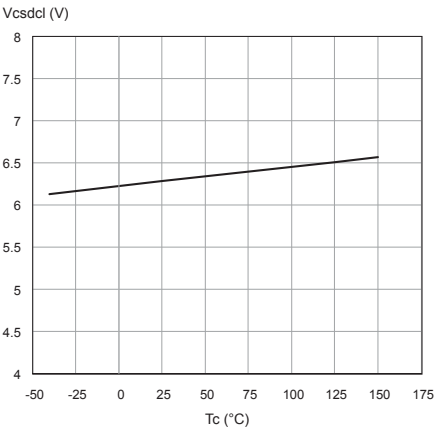
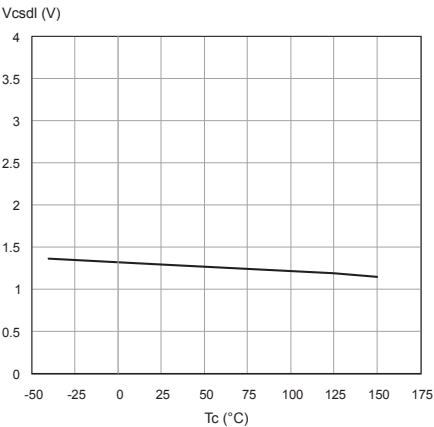
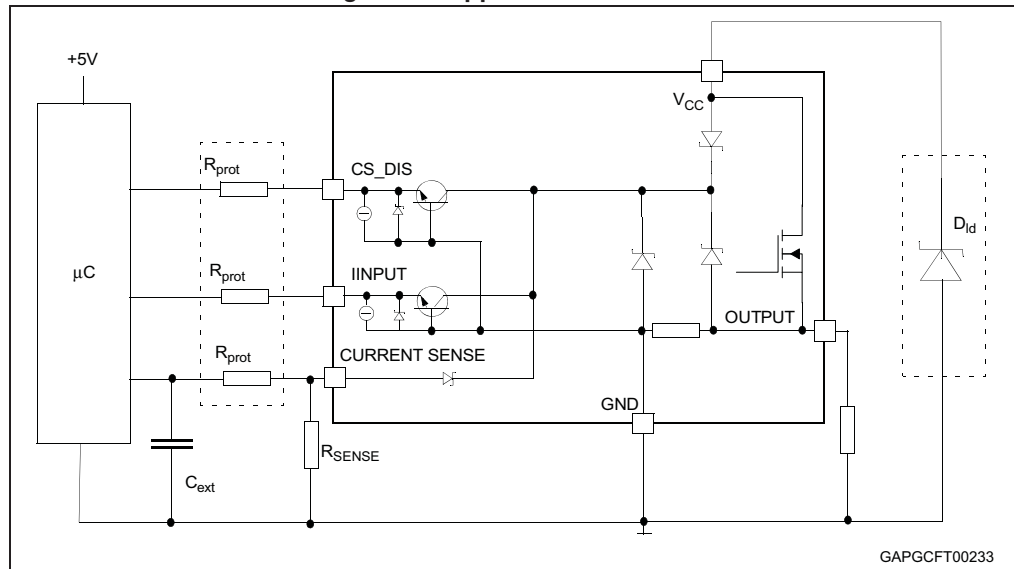


Figure 21. CS_DIS low level voltage



3 Application information

Figure 22. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins will be pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the μC I/Os pins from latching up.

The values of these resistors provide a compromise between the leakage current of the μC , the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -1.5 \text{ V}$ and $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$$75 \Omega \leq R_{prot} \leq 240 \text{ k}\Omega.$$

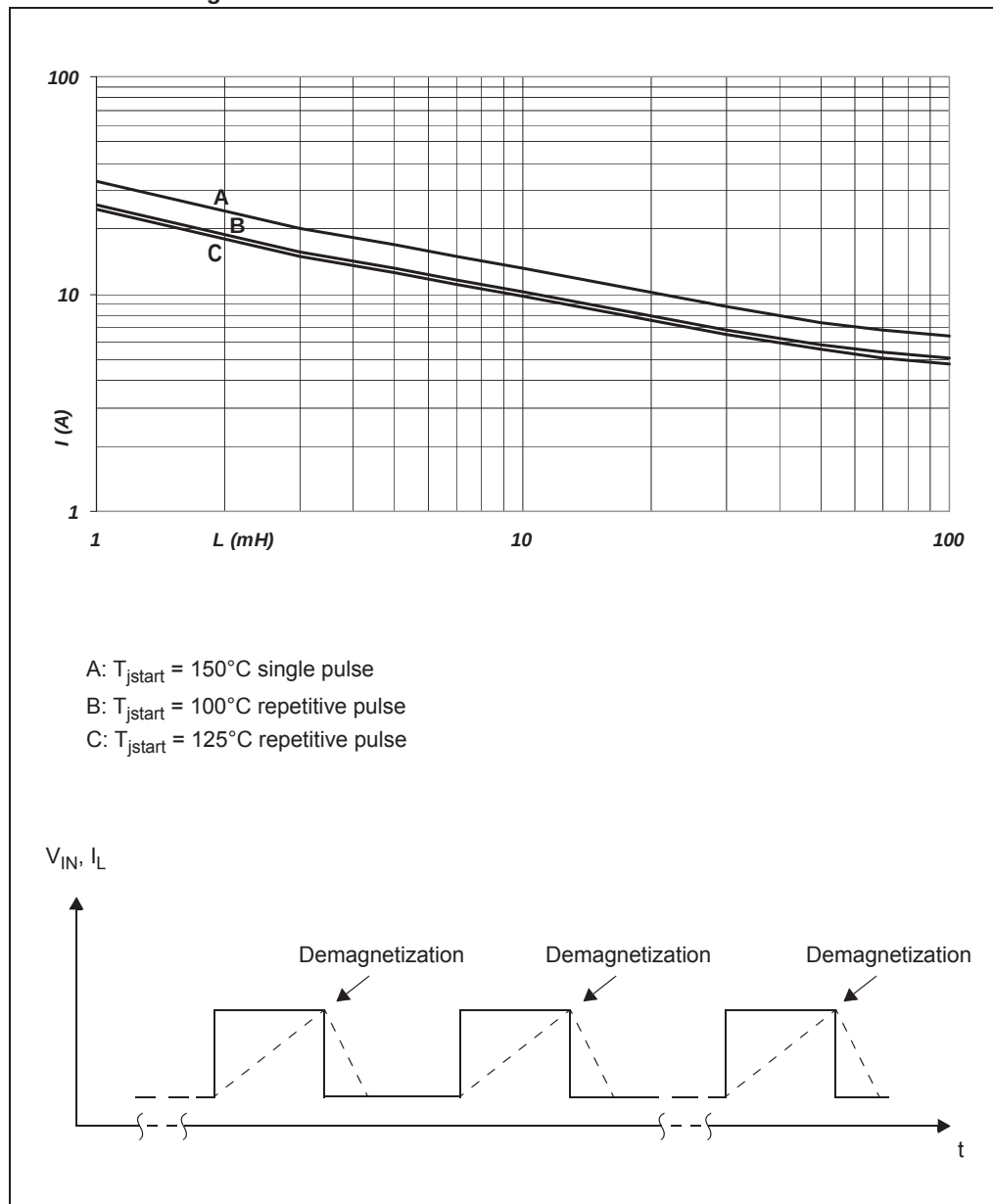
Recommended values: $R_{prot} = 10 \text{ k}\Omega$, $C_{EXT} = 10 \text{ nF}$

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in [Table 11](#).

3.3 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 23. Maximum turn off current versus inductance



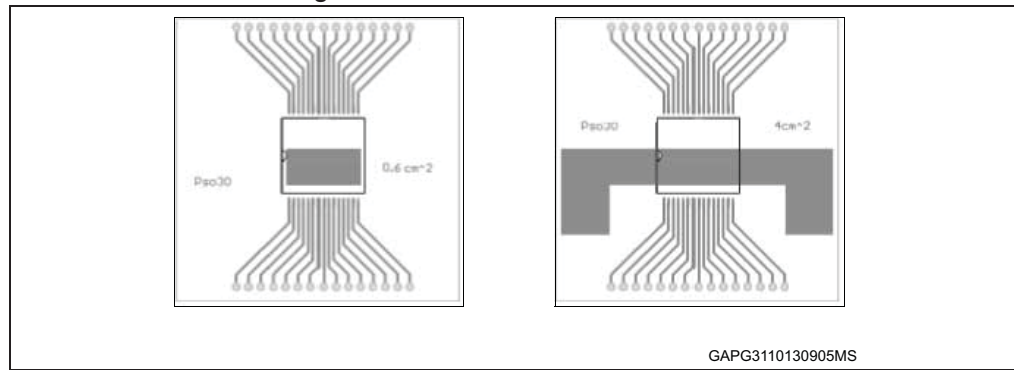
Note: Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 MultiPowerSO-30 thermal data

Figure 24. MultiPowerSO-30 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m (front and back side), Copper areas: from minimum pad layout to 16 cm²).

Figure 25. $R_{thj-amb}$ vs. PCB copper area in open box free air condition (one channel ON)

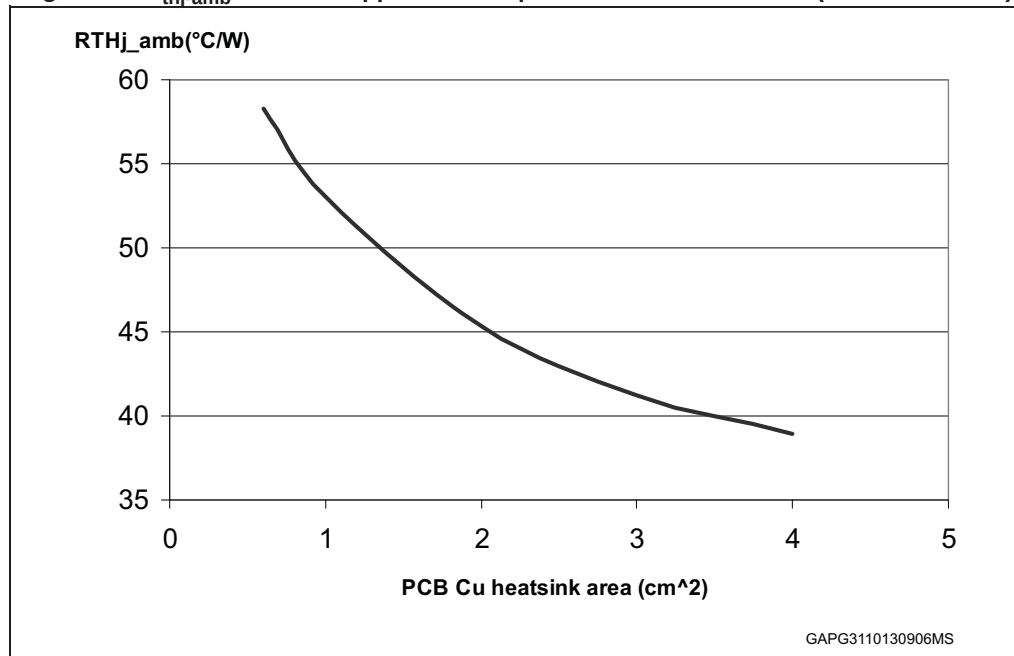


Figure 26. MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)

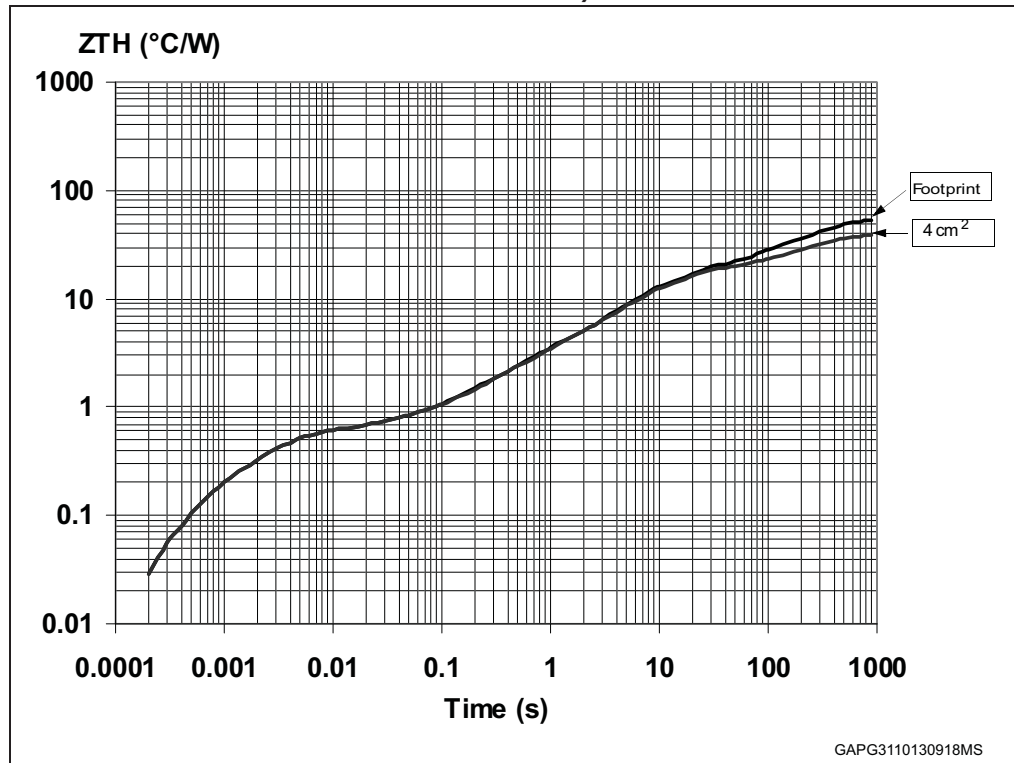
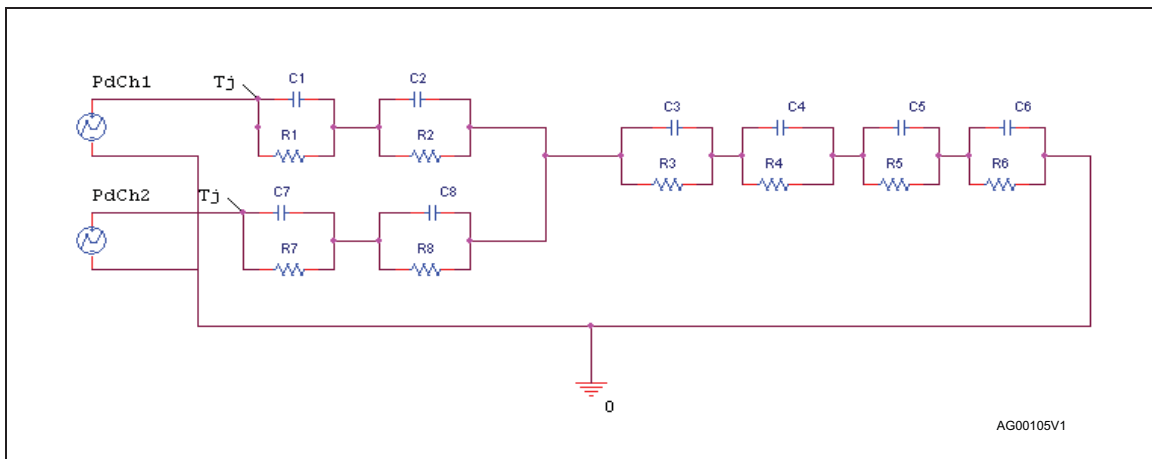


Figure 27. Thermal fitting model of a double channel HSD in MultiPowerSO-30



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 14. Thermal parameters for MultiPowerSO-30

Area/island (cm ²)	Footprint	4
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.5	
R4 (°C/W)	1.3	
R5 (°C/W)	14	
R6 (°C/W)	44.7	23.7
R7 (°C/W)	0.05	
R8 (°C/W)	0.3	
C1 (W.s/°C)	0.005	
C2 (W.s/°C)	0.008	
C3 (W.s/°C)	0.01	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.6	
C6 (W.s/°C)	5	11
C7 (W.s/°C)	0.005	
C8 (W.s/°C)	0.008	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 MultiPowerSO-30 package information

Figure 28. MultiPowerSO-30 package outline

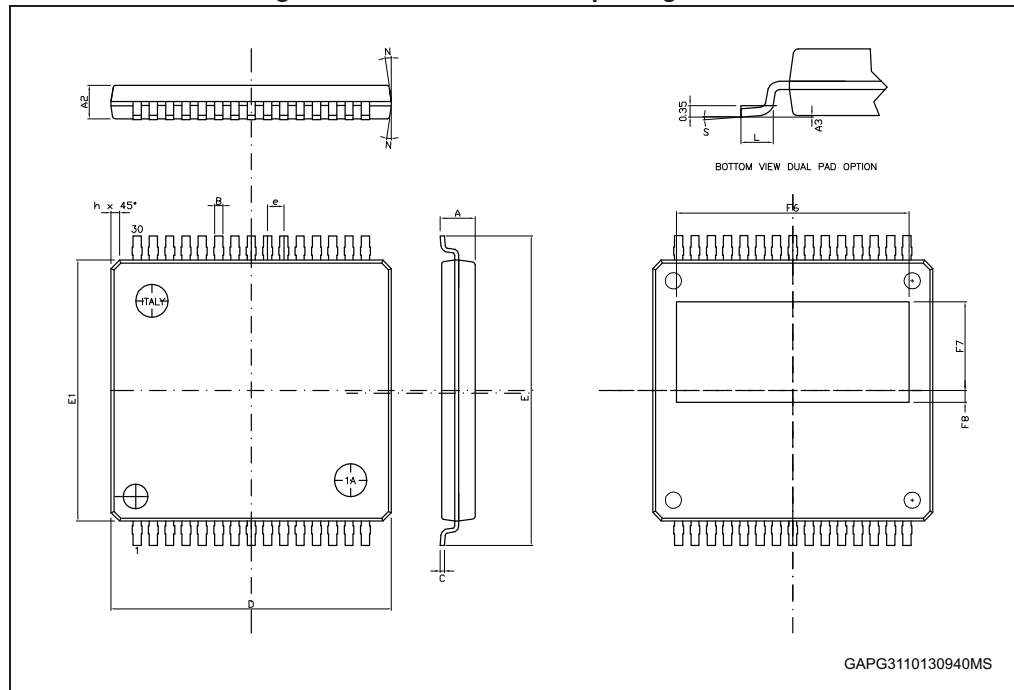


Table 15. MultiPowerSO-30 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1

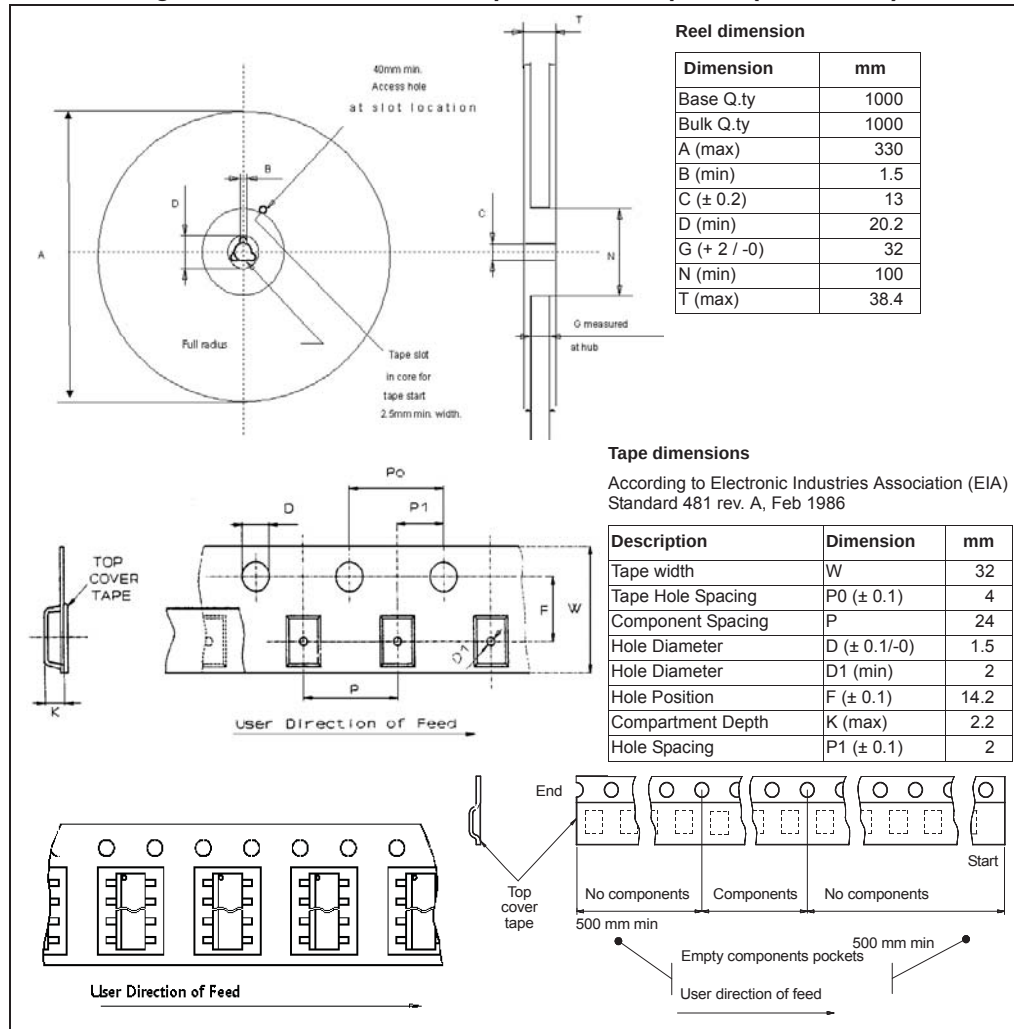
Table 15. MultiPowerSO-30 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
"e"	1		
F6		14.3	
F7		5.45	
F8		0.73	
L	0.8		1.15
N			10 Deg
S	0 Deg		7 Deg

5.2 MultiPowerSO-30 packing information

The devices are packed in tape and reel shipments (see [Table 16: Device summary on page 26](#)).

Figure 29. MultiPowerSO-30 tape and reel shipment (suffix "TR")



6 Order codes

Table 16. Device summary

Package	Order codes
	Tape and reel
MultiPowerSO-30	VND5004CSP30TR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
09-Jun-2015	1	Initial release.
02-Nov-2015	2	Updated <i>Table 16: Device summary</i>
11-Jan-2017	3	– Removed all information relative to tube packing of the product – Modified Section 5: Package information. – Added AEC-Q100 qualified in the Features section – Minor text edits throughout the document

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved