Vocal fader IC with input selector
BH3810FS

The BH3810FS is a vocal fader IC that is serial control compatible. It has mode switching that also includes a voice multiplexing mode, a five-input selector, a gain selector and other such features, which can all be controlled serially. Eight open-collector terminals and two tri-state terminals are provided on the chip to facilitate control by other ICs.

●Applications

Component stereo systems, CD radio cassette players, TVs and car stereos.

●Features

1) Built-in low-pass filter can perform vocal fader function (erasing of vocals from commercially available music software) using just one chip.
2) Serial control can be used to switch between vocal fader, through, multiplex, and mute modes.
3) Built-in gain selector allows selection of gain from 6dB to 20dB in 2dB steps.
4) Five-channel input selector.
5) Mic. mixing amplifier with mute function. Key controller input also provided.
6) SSOP-A32 pin package.

●Absolute maximum ratings (Ta = 25°C)

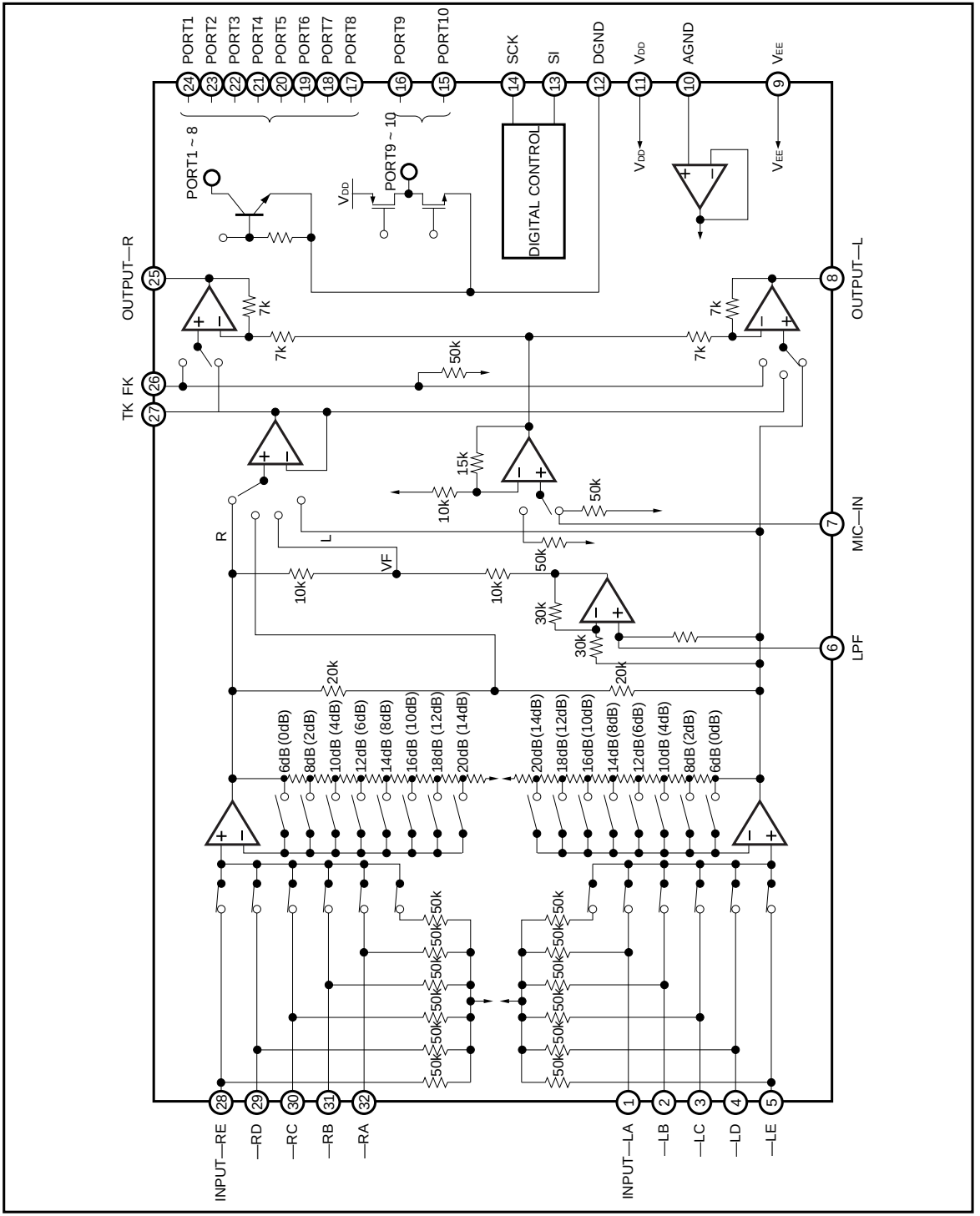
Parameter	Symbol	Limits	Unit
Applied voltages	V_{DD}	+ 5.5	V
	V_{EE}	– 4.5	
Power dissipation	Pd	850*	mW
Operating temperature	Topr	– 40 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 125	°C
Maximum open collector voltage	V_{OP}	14	V

* Reduced by 8.5mW for each increase in Ta of 1°C over 25°C , when mounted on a 50mm × 50mm × 1.6mm board.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	4.0 ~ 5.3	V
	V_{EE}	– 4.3 ~ – 3.0	V

●Block diagram



●Electrical characteristics (unless otherwise notes, Ta = 25°C, V_{DD} = 5V, V_{EE} = – 4V, G = 14dB, f =1kHz, Rg = 600Ω, V_{IN} = 150mV, and R_L = 100kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_{Q1} +	—	4.5	10.0	mA	Through mode V_{DD} current
	I_{Q1} –	—	4.1	10.0	mA	Through mode V_{EE} current
	I_{Q2} +	—	10.0	20.0	mA	Through mode D9 to D16 data1
	I_{Q2} –	—	7.6	20.0	mA	Through mode D9 to D16 data1
Maximum output voltage	Vom	1.5	2.2	—	V_{rms}	THD = 1%, through mode
L, R gain	G_{VT}	11	14	17	dB	Through mode
Low-frequency gain	G_{VF}	8	11	14	dB	Vocal fader mode, f = 100Hz
Microphone gain	G_{VM}	5	8	11	dB	—
Crosstalk	CT	54	64	—	dB	f = 1kHz, through mode
Mute attenuation	MU	60	80	—	dB	f = 1kHz, mute mode or input mute
Vocal suppression ratio	SV	15	20	—	dB	Vocal fader mode, f = 1kHz
Total harmonic distortion	THD	—	0.004	0.05	%	V_O = 1V_{rms}, through mode, BW 400Hz to 30kHz
Noise level	V_N	—	15	22	μV_{rms}	R_g = 0, DIN AUDIO ＊
Mode switch output DC differential	ΔDCB	—	0	18	mV	Between each mode with key controller on
Input impedance	R_{IN}	35	50	65	kΩ	Pins 1 to 5, pins 26, pins 28 to 32
Input selector crosstalk	CT_{IN}	80	—	—	dB	f = 1kHz
Port output current	$I_{PMax.}$	5.0	12	—	mA	Pins 17 to 24, 0.5V between PORT terminal and GND voltage = 0.5V
"L" output voltage	V_{OL}	—	0.15	0.5	V	Pins 17 to 27, I_{OL} = 5mA
"H" output leakage current	I_{OH}	—	0	2.0	μA	Pins 17 to 24, 13V applied to collector
Tri-state "H" output voltage	V_{SOH}	4.5	4.85	—	V	Pins 15 to 16, Io = 1mA
Tri-state "L" output voltage	V_{SOL}	—	0.05	0.5	V	Pins 15 to 16, Io = 1mA
SI pin source current (pin 13)	I_{SI}	—	0.4	10	μA	When SI pin is at DGND potential
SCK pin source current (pin 14)	I_{SCK}	—	0.2	10	μA	When SCK pin is at DGND potential

＊ Measured using a Matsushita VP-9690A (average value detector, effective value display) DIN AUDIO filter.
Operating specifications: same phase for the input and output signals.
○ Not designed for radiation resistance.

●Measurement circuit

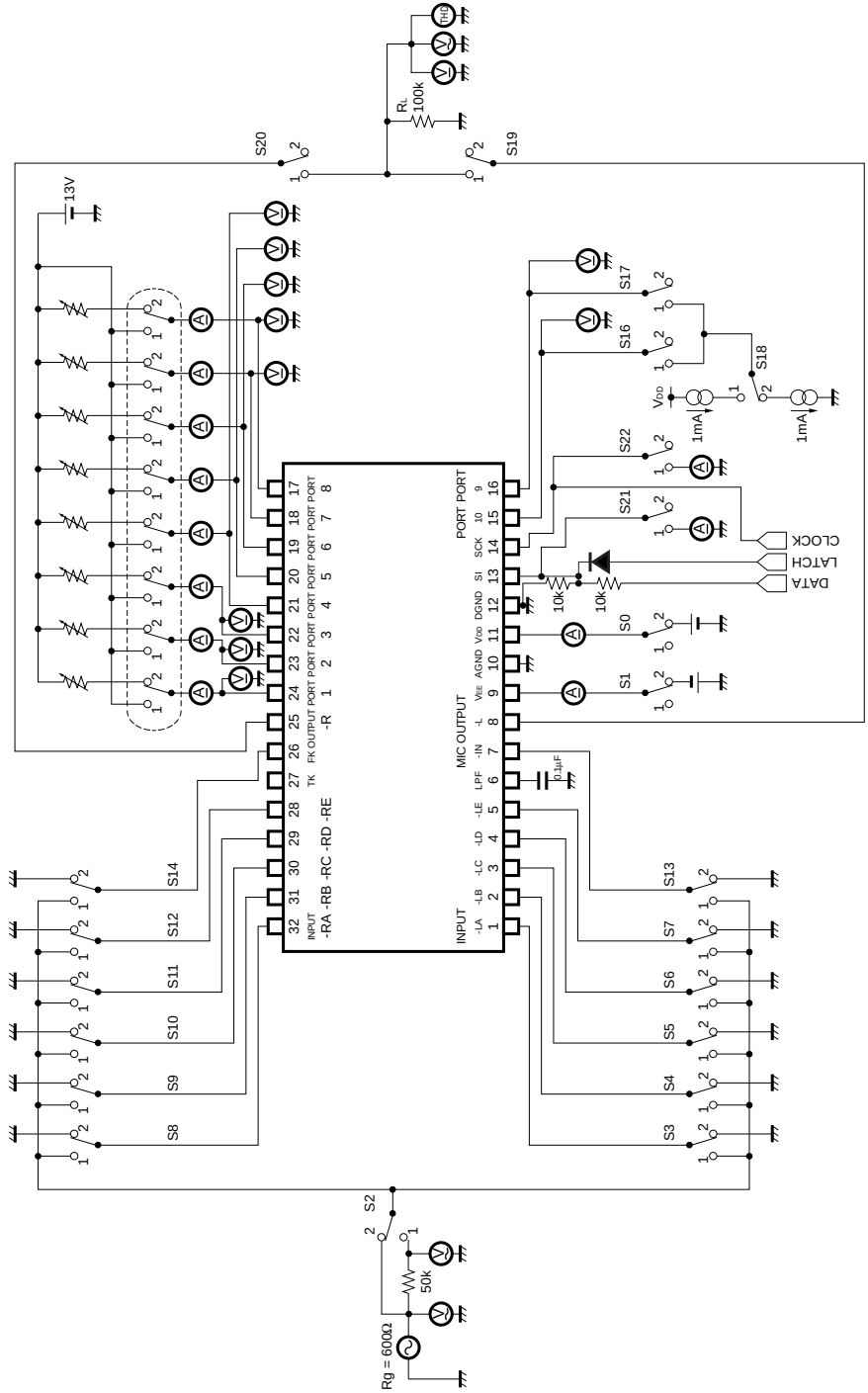


Fig. 1

●Circuit operation

(1) About the data format

Data format

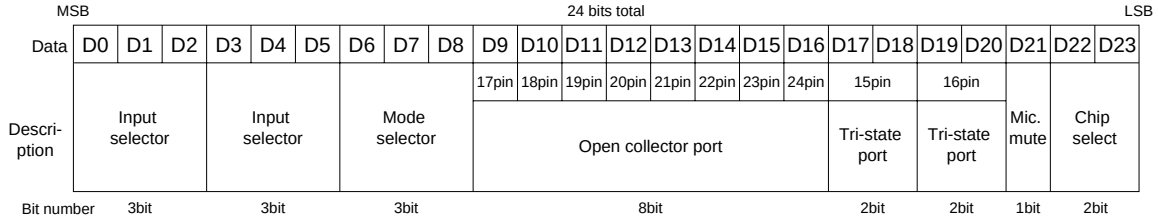


Fig.2

• Address is "00"

D22	D23
0	0

At power on

Gain selector	6dB
Mode selector	Through mode
Mic	Mute OFF
Key controller	OFF
Input selector	LA, RA

Output port: current attraction OFF
Tri-state port: Low

Output port: open collector

Data	D16	D15	D14	D13	D12	D11	D10	D9
Pin name	PORT 1 (24pin)	PORT 2 (23pin)	PORT 3 (22pin)	PORT 4 (21pin)	PORT 5 (20pin)	PORT 6 (19pin)	PORT 7 (18pin)	PORT 8 (17pin)
0	Current sink OFF							
1	Current sink ON							

Tri-state

PORT9 (16pin)

D19	D20	Mode
0	0	LOW
0	1	OPEN
1	0	OPEN
1	1	HI

D19, D20

PORT10 (15pin)

D17	D18	Mode
0	0	LOW
0	1	OPEN
1	0	OPEN
1	1	HI

D17, D18

Mic. mute

D21	Mode
0	Mic. ON
1	Mic. MUTE

Input selector ⟨3 bits⟩ D0 to D2

D0	D1	D2	Mode
0	0	0	MUTE
0	0	1	MUTE
0	1	0	MUTE
0	1	1	INPUT—LA, INPUT—RA
1	0	0	INPUT—LB, INPUT—RB
1	0	1	INPUT—LC, INPUT—RC
1	1	0	INPUT—LD, INPUT—RD
1	1	1	INPUT—LE, INPUT—RE

Gain selector ⟨3 bits⟩ D3 to D5

D3	D4	D5	Gain select
0	0	0	6dB
0	0	1	8dB
0	1	0	10dB
0	1	1	12dB
1	0	0	14dB
1	0	1	16dB
1	1	0	18dB
1	1	1	20dB

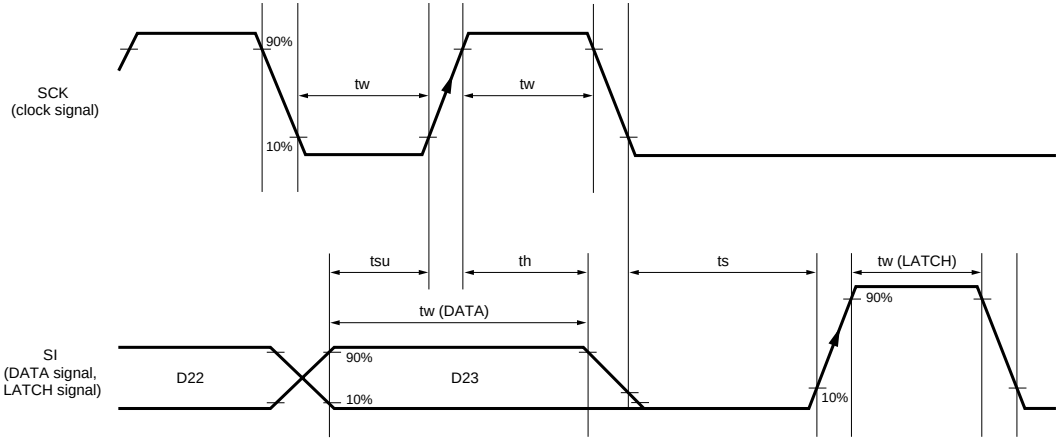
The gain is the total gain from input to output.

Mode selector ⟨3 bits⟩ D6 to D8

D6	D7	D8	LOUT	ROUT	TK	Mode
0	0	0	MUTE	MUTE	MUTE	Mute
0	0	1	VOCALFADE	VOCALFADE	VOCALFADE	Vocal fader
0	1	0	L	L	L	L channel
0	1	1	L	R	L	Through
1	0	0	FK	FK	L + R	Key controller, L + R
1	0	1	FK	FK	R	Key controller, R channel
1	1	0	FK	FK	L	Key controller, L channel
1	1	1	FK	FK	VOCALFADE	Key controller, vocal fader

(2) Timing chart

Serial data timing (timing for the IC terminals)



∗ When LATCH is "H", the DATA signal is forced "L" internally.
∗ The read decision for the DATA signal (SI) is made by the signal when the CLOCK signal rises.
∗ The read decision for the LATCH signal (SI) is made by the signal when the LATCH signal itself rises.
∗ A "L" must follow at the end of each signal to wait for the next signal.

Fig.3

●Timing chart constants (Ta = 25°C, V_{DD} = 5V and V_{EE} = – 4V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
M input voltage	V_{IM}	2.0	2.5	3.0	V
L input voltage	V_{IL}	– 0.3	0	1.0	V
Minimum clock width	tw	2.0	—	—	µs
Minimum data width	tw (DATA)	4.0	—	—	µs
Minimum latch width	tw (LATCH)	2.0	—	—	µs
Setup time (DATA to CLK)	tsu	1.0	—	—	µs
Hold time (CLK to DATA)	th	1.0	—	—	µs
Setup time (DATA, CLK to LATCH)	ts	1.0	—	—	µs

∗ If the voltage between V_{DD} and DGND changes, the values above will change.

●Application circuit

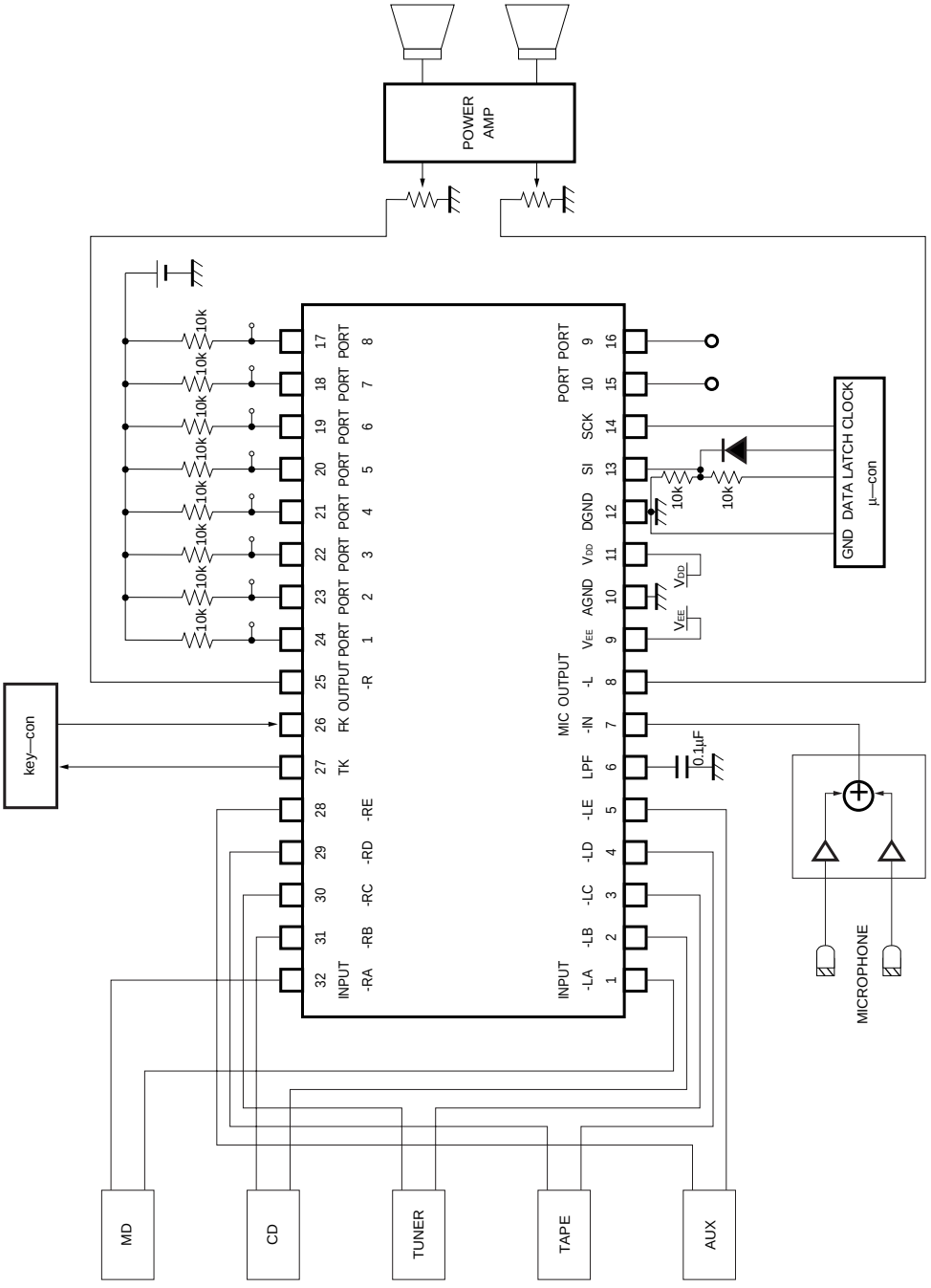


Fig. 4

●Operation notes

(1) We guarantee the application circuit design, but recommend that you thoroughly check its characteristics in actual use.

If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

Note that Rohm has not fully investigated patent rights regarding this product.

(2) The vocal fader function

The effect of the vocal fader is realized by negating the same-phase components. In the bass region, the first-stage low-pass filter leaves the source sound as is, even for the same-phase components. Therefore, depending on the music, the effect may be small.

(3) The low-pass filter that leaves the vocal fader bass

The low-pass filter is formed by connecting a capacitor to pin 6. A 20kΩ resistor (design value) and this capacitor set the cutoff frequency.

$$fc = \frac{1}{2\pi CR} \text{ (Hz)}$$

The optional attenuation of the first-stage low-pass filter frequency is:

$$A(f) = 20 \log \left(\sqrt{\frac{1}{1 + (2\pi fCR)^2}} \right) \text{ (dB)}$$

f: frequency
C: external capacitor
R: 20kΩ (design value)

(4) AGND (pin 10) and DGND (pin 12)

AGND is the ground for the IC's internal analog circuits, and DGND is the ground for the internal ports 1 to 10. Connect the two grounds externally.

(5) Switching noise

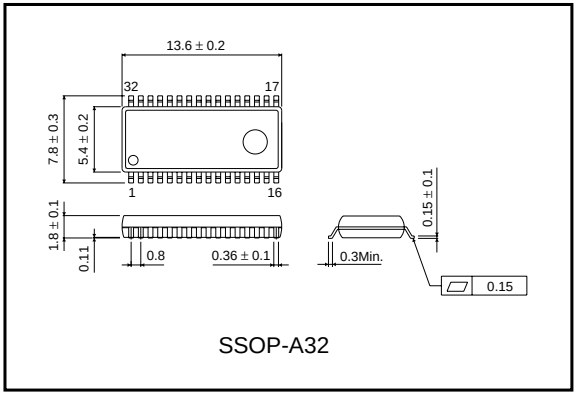
If you are troubled by switching noise that occurs when the input selector, gain selector, or mode selector are switched, use muting, or some other appropriate countermeasure.

(6) Serial control

The LATCH and DATA serial signals are received on the same terminal, and the signals are differentiated by voltage level. A diode and resistor are connected to perform a conversion to logic voltage (0 to 5V). The threshold values will change depending on the external components, so select them carefully.

If the signals are not being received very well, connect a capacitor of about 100pF between the SI terminal (pin 13), and the DGND terminal (pin 12).

●External dimensions (Units: mm)



SSOP-A32