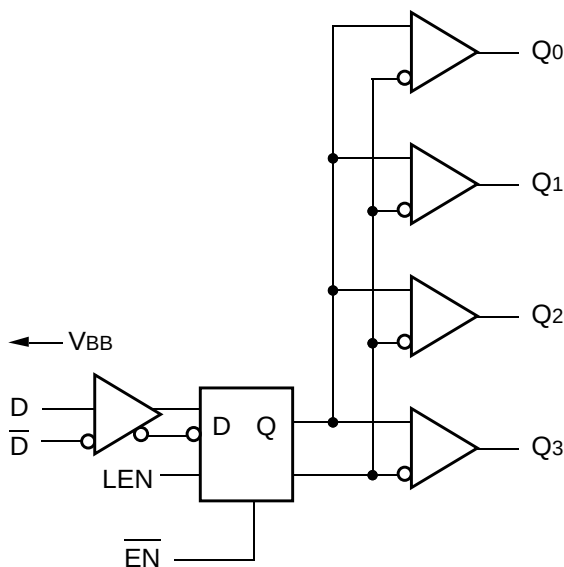


FEATURES

- 3.3V power supply
- Translates positive ECL to TTL (PECL-to-TTL)
- 300ps pin-to-pin skew
- 500ps part-to-part skew
- Differential internal design for increased noise immunity and stable threshold inputs
- VBB reference output
- Single supply
- Enable input
- Latch enable input
- Extra TTL and ECL power/ground pins to reduce cross-talk/noise
- High drive capability: 24mA each output
- Fully compatible with industry standard 10K, 100K I/O levels
- Available in 16-pin SOIC package

BLOCK DIAGRAM



DESCRIPTION

The SY10/100H841L are single supply, low skew translating 1:4 clock drivers.

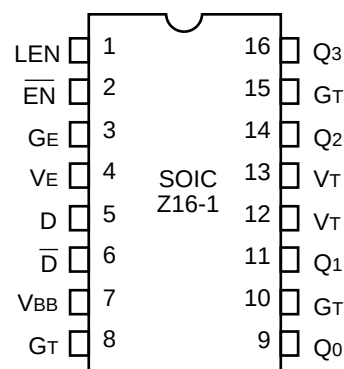
The devices feature a 24mA TTL output stage, with AC performance specified into a 20pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs) the latch is transparent. A HIGH on the enable pin (EN) forces all outputs LOW.

As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H841 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATION



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+3.3V)
VE	ECL Vcc (+3.3V)
GE	ECL Ground (0V)
D, D̄	Signal Input (PECL)
VBB	VBB Reference Output (PECL)
Q0 - Q3	Signal Outputs (TTL)
EN̄	Enable Input (PECL)
LEN	Latch Enable Input

TRUTH TABLE

D	LEN	$\overline{\text{EN}}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V_E (ECL) V_T (TTL)	Power Supply Voltage	−0.5 to +7.0 −0.5 to +7.0	V
V_I (ECL) V_{OUT} (TTL)	Input Voltage	0.0 to V_{EE} 0.0 to V_T	V
T_{store}	Storage Temperature	−65 to +150	°C
T_A	Operating Temperature	0 to +85	°C

NOTE:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{\text{EN}}$	Enable Input (PECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+3.3V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output (PECL)
8	G_T	TTL Ground (0V)
9	Q0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+3.3V)
13	V_T	TTL V_{CC} (+3.3V)
14	Q2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q3	Signal Output (TTL)

DC CHARACTERISTICS

$V_T = V_E = +3.0V$ to +3.6V

Symbol	Parameter		$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = +3.0V$ to +3.6V

Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	V	$I_{OH} = -3.0\text{mA}$
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	$I_{OL} = 24\text{mA}$
I_{OS}	Output Short Circuit Current	−80	—	−80	—	−80	—	mA	$V_{OUT} = 0V$

10H ECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_T = V_E = +3.0V$ to $+3.6V$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V_{IH}	Input HIGH Voltage	2.130	2.460	2.170	2.490	2.240	2.580	V	$V_E = 3.3V$
V_{IL}	Input LOW Voltage	1.350	1.820	1.350	1.820	1.350	1.855	V	$V_E = 3.3V$
V_{BB}	Output Reference Voltage	1.920	2.030	1.950	2.050	1.990	2.110	V	$V_E = 3.3V$

NOTE:

1. ECL V_{IH} , V_{IL} and V_{BB} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for $I_{VT} = I_{VO} = V_{CC} = +3.3V$.

100H ECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_T = V_E = +3.0V$ to $+3.6V$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V_{IH}	Input HIGH Voltage	2.135	2.420	2.135	2.420	2.135	2.420	V	$V_E = 3.3V$
V_{IL}	Input LOW Voltage	1.490	1.825	1.490	1.825	1.490	1.825	V	$V_E = 3.3V$
V_{BB}	Output Reference Voltage	1.920	2.040	1.920	2.040	1.920	2.040	V	$V_E = 3.3V$

NOTE:

1. ECL V_{IH} , V_{IL} and V_{BB} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for $I_{VT} = I_{VO} = V_{CC} = +3.3V$.

AC CHARACTERISTICS

$V_T = V_E = +3.0V$ to $+3.6V$

Symbol	Parameter		$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q0–Q3	2.2	3.2	2.1	3.1	2.0	3.0	ns	$C_L = 20pF$
t_{skpp}	Part-to-Part Skew ^(1,4)	Q0–Q3	—	0.5	—	0.5	—	0.5	ns	$C_L = 20pF$
t_{skew++}	Within-Device Skew ^(2,4)	Q0–Q3	—	0.3	—	0.3	—	0.3	ns	$C_L = 20pF$
t_{skew--}	Within-Device Skew ^(3,4)	Q0–Q3	—	0.3	—	0.3	—	0.3	ns	$C_L = 20pF$
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q0–Q3	2.2	3.2	2.1	3.1	2.0	3.0	ns	$C_L = 20pF$
t_{PLH} t_{PHL}	Propagation Delay EN to Output	Q0–Q3	2.2	3.2	2.1	3.1	2.0	3.0	ns	$C_L = 20pF$
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q0–Q3	—	1.5	—	1.5	—	1.5	ns	$C_L = 20pF$
f_{MAX}	Max. Input Frequency ^(5,6)	Q0–Q3	160	—	160	—	160	—	MHz	$C_L = 20pF$
—	Pulse Width	Q0–Q3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q0–Q3	1.0	—	1.0	—	1.0	—	ns	—
t_s	Set-up Time D, $\overline{EN}$	Q0–Q3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, EN	Q0–Q3	0.75	—	0.75	—	0.75	—	ns	—

NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

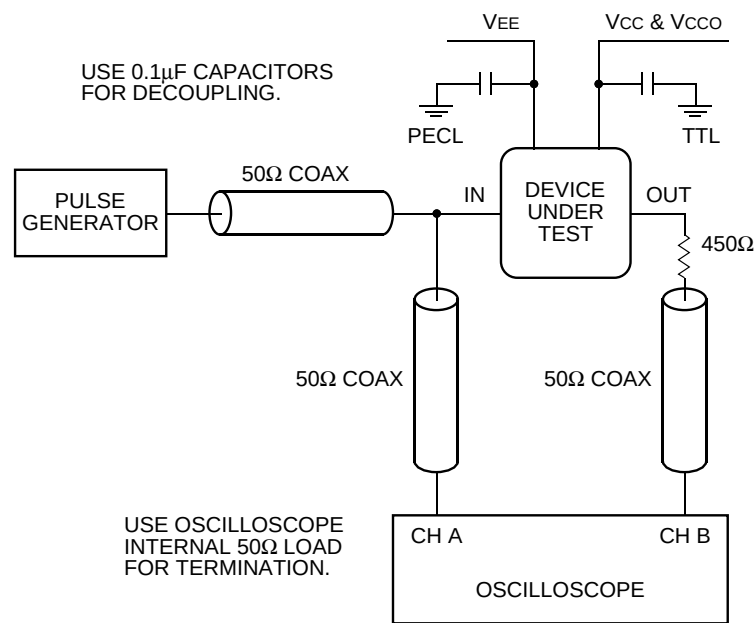
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.

4. All skew parameters are guaranteed but not tested.

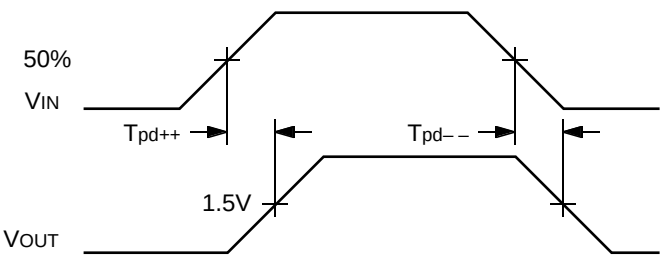
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

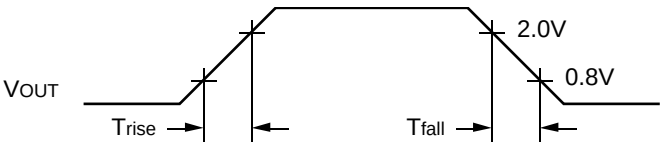
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



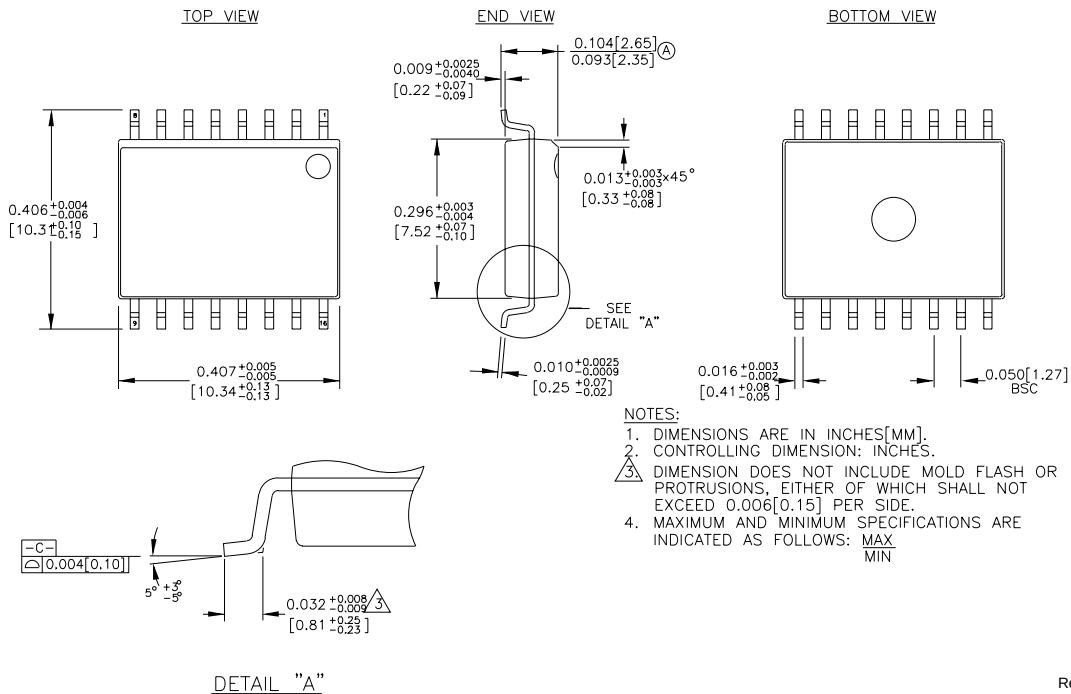
ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H841LZC	Z16-1	Commercial
SY10H841LZCTR	Z16-1	Commercial
SY100H841LZC	Z16-1	Commercial
SY100H841LZCTR	Z16-1	Commercial

16 LEAD SOIC .300" WIDE (Z16-1)



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