Data Sheet | April 22, 2009 | FN6413.1

Power Sequencing Controllers

The Intersil ISL8723 and ISL8724 are 4 channel sequencers controlling the on and off sequence of voltages with undervoltage supply fault protection and a “sequence completed” signal ($\overline{\text{RESET}}$). For larger systems, more than 4 voltages can be sequenced by a simple connection of multiple IC's. These sequencers use an integrated charge pump to drive 4 external low-cost N-channel MOSFET switch gates above the IC bias voltage by 5.3V. These IC's can be biased from and control any supply from 2.5V to 5V and additionally monitor any voltage above 0.7V. Individual product descriptions follow.

The four channel **ISL8723** (ENABLE input), **ISL8724** ($\overline{\text{ENABLE}}$ input) offer the designer 4 voltage control when it is required that all four rails are in minimal compliance prior to turn on and that compliance must be maintained during operation. The **ISL8723** has a low power standby mode when it is disabled suitable for battery powered applications.

External resistors provide flexible voltage threshold programming of monitored voltages. Delay and sequencing timing are programmable by external capacitors for both ramp up and ramp down.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8723IRZ*	87 23IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL8724IRZ*	87 24IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL8723EVAL1	Evaluation Platform			

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

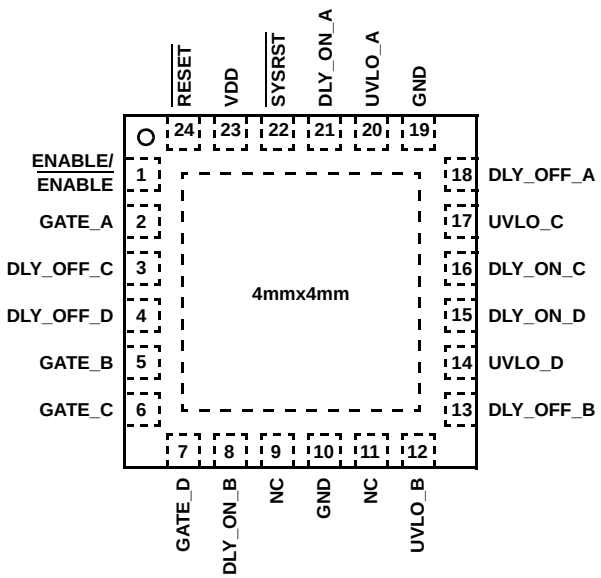
- Enables arbitrary turn-on and turn-off sequencing of up to four power supplies (0.7V to 5V)
- Operates from 2.5V to 5V supply voltage
- Supplies V_{DD} +5.3V of charge pumped gate drive
- Adjustable voltage slew rate for each rail
- Multiple sequencers can be easily daisy-chained to sequence an infinite number of independent voltages
- Glitch immunity
- Undervoltage lockout for each monitored supply voltage
- 30µA Sleep State (**ISL8723**)
- Active high (**ISL8723**) or low (**ISL8724**) $\overline{\text{ENABLE}}$ input
- Pb-free (RoHS compliant)

Applications

- Graphics cards
- FPGA/ASIC/microprocessor/PowerPC supply sequencing
- Network Routers
- Telecommunications Systems

Pinout

ISL8723, ISL8724
(24 LD QFN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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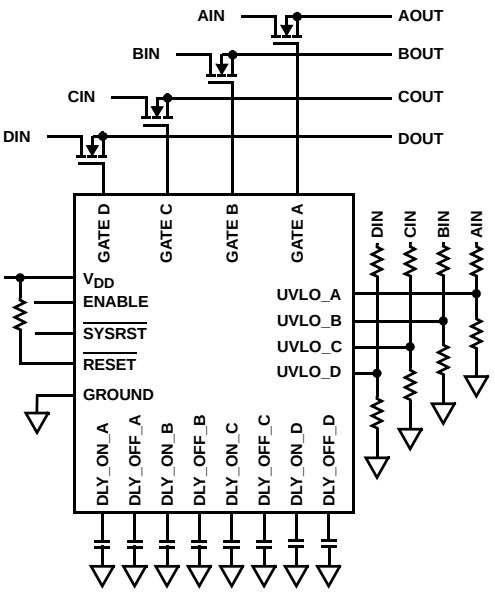


FIGURE 1. TYPICAL ISL8723 APPLICATION USAGE

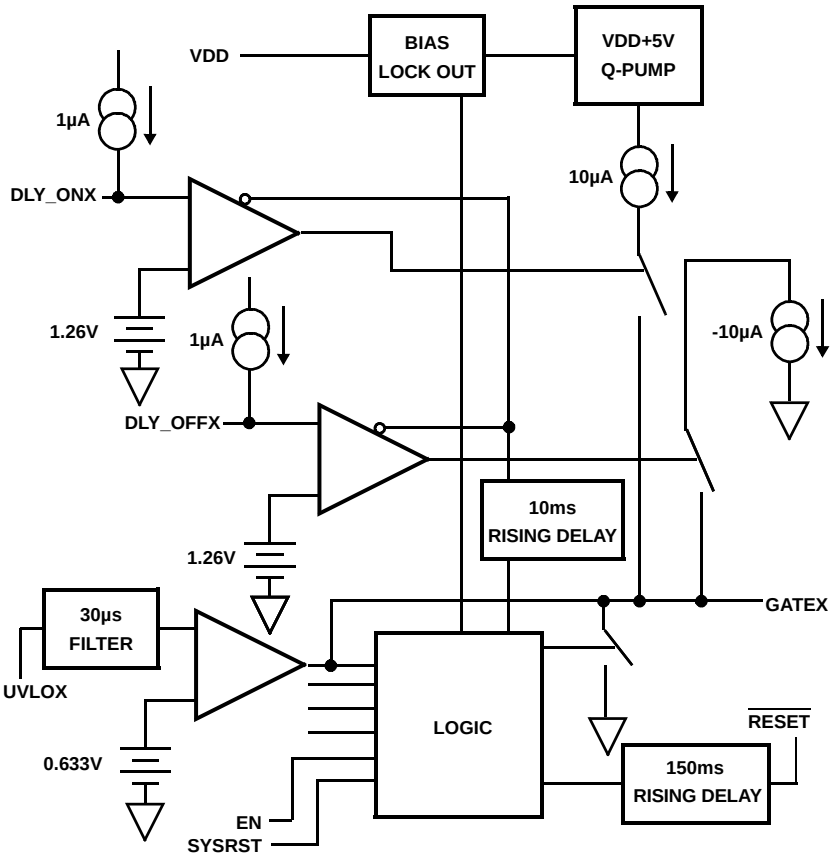


FIGURE 2. ISL8723 BLOCK DIAGRAM (1/4)

Pin Descriptions

PIN #	PIN NAME	FUNCTION	DESCRIPTION
23	VDD	Chip Bias	Bias IC from nominal 2.5V to 5V
10, 19	GND	Bias Return	IC ground. NOTE: Pin 19 internally tied to GND with 6kΩ. This pin can be tied to GND or left open.
1	ENABLE/$\overline{\text{ENABLE}}$	Input to start on/off sequencing	Input to initiate the start of the programmed sequencing of supplies on or off. Enable functionality is disabled for 10ms after UVLO is satisfied. ISL8723 has ENABLE. ISL8724 has $\overline{\text{ENABLE}}$.
24	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output	$\overline{\text{RESET}}$ provides a high signal ~160ms after all GATEs are fully enhanced. This delay is for stabilization of output voltages. $\overline{\text{RESET}}$ will assert low upon any UVLO not being satisfied or ENABLE/$\overline{\text{ENABLE}}$ being deasserted. The $\overline{\text{RESET}}$ output is an open drain N-channel FET and is guaranteed to be in the correct state for VDD down to 1V and is filtered to ignore fast transients on VDD and UVLO_X.
20	UVLO_A	Undervoltage Lock Out/Monitoring Input	These inputs provide for a programmable UV lockout referenced to an internal 0.631V reference and are filtered to ignore short (<7µs) transients below programmed UVLO level.
12	UVLO_B		
17	UVLO_C		
14	UVLO_D		
21	DLY_ON_A	Gate On Delay Timer Output	Allows for programming the delay and sequence for V_{OUT} turn-on using a capacitor to ground. Each cap is charged with 1µA, 10ms after turn-on initiated by ENABLE/$\overline{\text{ENABLE}}$ with an internal current source providing delayed enhancement of the associated FETs GATE to turn-on.
8	DLY_ON_B		
16	DLY_ON_C		
15	DLY_ON_D		

Pin Descriptions (Continued)

PIN #	PIN NAME	FUNCTION	DESCRIPTION
18	DLY_OFF_A	Gate Off Delay Timer Output	Allows for programming the delay and sequence for V_{OUT} turn-off through ENABLE/$\overline{\text{ENABLE}}$ via a capacitor to ground. Each cap is charged with a 1µA internal current source to an internal reference voltage causing the corresponding gate to be pulled down thus turning-off the FET.
13	DLY_OFF_B		
3	DLY_OFF_C		
4	DLY_OFF_D		
2	GATE_A	FET Gate Drive Output	Drives the external FETs with a 10µA current source to soft start ramp into the load. During sequence off, 10µA is sunk from this pin to control the FET turn-off. During a turn-off due to a fault, the gate will sink ~75mA to ensure a rapid turn-off.
5	GATE_B		
6	GATE_C		
7	GATE_D		
22	$\overline{\text{SYSRST}}$	System Reset I/O	As an input, allows for immediate and unconditional latch-off of all GATE outputs when driven low. This pin can also be used to initiate the programmed sequence with ‘zero’ wait (no 10ms stabilization delay) from input signal on this pin being driven high to first GATE. As an output when there is a UV condition this pin pulls low. If common to other $\overline{\text{SYSRST}}$ pins in a multiple IC configuration it will cause immediate and unconditional latch-off of all other GATEs on all other ISL872x sequencers. This pin is released to go high once all UVLO and enable conditions are satisfied and is pulled low concurrent with the last GATE being turned off after EN disabled.
9, 11	No Connect	No Connect	No Connect

Absolute Maximum Ratings

V_{DD} . . . . . +6.0V
GATE . . . . . -0.3V to V_{DD}+6V
UVLO, ENABLE, $\overline{\text{ENABLE}}$, $\overline{\text{SYSRST}}$ . . . . . -0.3V to V_{DD} +0.3V
$\overline{\text{RESET}}$, DLY_ON, DLYOFF . . . . . -0.3V to V_{DD} +0.3V

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +2.5V to +5.0V
Temperature Range (T_A) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package	48	9

Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 3.3V to +5V, T_A = T_J = -40°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
Undervoltage Lockout Falling Threshold	$V_{UVLOvth}$	T_A = T_J = +25°C	619	631	647	mV
Undervoltage Lockout Falling Threshold	$V_{UVLOvth}$		604	631	656	mV
Undervoltage Lockout Hysteresis	$V_{UVLOhys}$		-	9	-	mV
Undervoltage Lockout Threshold Range	RUVLOvth	Max $V_{UVLOvth}$- Min $V_{UVLOvth}$	-	6	18	mV
Undervoltage Lockout Delay	$t_{UVLOdel}$	ENABLE satisfied	-	10	-	ms
Transient Filter Duration	tFIL	V_{DD}, UVLO, ENABLE glitch filter	-	7	-	µs
DELAY ON/OFF						
Delay Charging Current	DLY_ichg	V_{DLY} = 0V	0.9	1	1.115	µA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)	-	0.01	0.05	µA
Delay Threshold Voltage	DLY_Vth		1.21	1.273	1.32	V
ENABLE/$\overline{\text{ENABLE}}$, $\overline{\text{RESET}}$ AND $\overline{\text{SYSRST}}$ I/O						
ENABLE Threshold	V_{ENh}	Measured at V_{DD} = 5V	-	1.28	1.35	V
$\overline{\text{ENABLE}}$ Threshold	V_{ENh}		-	0.5 V_{DD}	-	V
ENABLE/$\overline{\text{ENABLE}}$ Hysteresis	V_{ENh} -V_{ENl}	Measured at V_{DD} = 5V	-	0.1	0.2	V
ENABLE/$\overline{\text{ENABLE}}$ Lockout Delay	t_{delEN_LO}	UVLO satisfied, EN to DLY_ON	-	10	-	ms
ENABLE/$\overline{\text{ENABLE}}$ Input Capacitance	C_{IN_EN}		-	5	-	pF
$\overline{\text{RESET}}$ Pull-up Voltage	V_{PU_RST}		-	V_{DD}	-	V
$\overline{\text{RESET}}$ Pull-Down Current	$I_{\overline{RST}pd5}$	V_{DD} = 5V, $\overline{\text{RST}}$ = 0.1V	-	13	-	mA
$\overline{\text{RESET}}$ Delay after GATE High	$T_{\overline{RST}del}$	GATE = V_{DD} + 5V	-	160	-	ms
$\overline{\text{RESET}}$ Output Low	$V_{\overline{RST}l}$	Measured at V_{DD} = 5V, 1mA sourcing current	-	-	0.1	V
RESET Output Capacitance	C_{OUT_RST}		-	10	-	pF
$\overline{\text{SYSRST}}$ Pull-up Voltage	V_{PU_SRST}		-	V_{DD} - 0.5V	-	V
$\overline{\text{SYSRST}}$ Pull-up Current	I_{PU_SRST}	V_{DD} = 3.3V, $\overline{\text{SYSRST}}$ = 0.5V	-	12	-	µA
$\overline{\text{SYSRST}}$ Pull Down Current	I_{PU_5}	V_{DD} = 5V	-	2.7	-	µA

Electrical Specifications V_{DD} = 3.3V to +5V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{SYSRST}$ Low Output Voltage	V_{OL_SRST}	V_{DD} = 5V, I_{OUT} = 100µA	-		0.1	V
$\overline{SYSRST}$ Output Capacitance	C_{OUT_SRST}		-	10	-	pF
$\overline{SYSRST}$ Low to GATE Turn-off	$t_{delSYS_G_1}$	GATE = 80% of V_{DD}+5V	-	40	-	ns
$\overline{SYSRST}$ High to GATE Turn-on	$t_{delSYS_G_2}$	GATE = 50% of V_{DD}+5V	-	0.4	-	ms
GATE						
GATE Turn-On Current	I_{GATEon}	GATE = 0V	8.3	10.2	12.5	µA
GATE Turn-Off Current	$I_{GATEoff_l}$	GATE = V_{DD}, Disabled	-12.5	-10.2	-8.3	µA
GATE Current Range	I_{GATE_range}	Within IC I_{GATE} max-min	-	0.6	3	µA
GATE Pull-Down High Current	$I_{GATEoff_h}$	GATE = V_{DD}, UVLO = 0V	-	75	-	mA
GATE High Voltage	V_{GATEh5}	V_{DD} = 5V	V_{DD} + 5.3V	V_{DD} + 5.6V	-	V
GATE Low Voltage	V_{GATEl}	Gate Low Voltage, V_{DD} = 1V	-	0.01	0.1	V
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V, Enabled and static	-	0.48	0.6	mA
ISL8723 Stand By IC Supply Current	I_{VDD_sb}	V_{DD} = 5V, ENABLE = 0V	-	30	40	µA
V_{DD} Power On Reset	$V_{DD_}POR$	V_{DD} rising	-	2.2	2.41	V

ISL8723, ISL8724 Descriptions and Operation

The ISL8723 and ISL8724 sequencers are quad voltage sequencing controllers designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to ~V_{DD} +5.6V (VQP) in a user programmed sequence.

With the ISL8723, the ENABLE must be asserted high and all four voltages to be sequenced must be above their respective user programmed Undervoltage Lock Out (UVLO) levels before programmed output turn on sequencing can begin. Sequencing and delay determination is accomplished by the choice of external capacitor values on the DLY_ON and DLY_OFF pins. The $\overline{SYSRST}$ goes high once all 4 UVLO inputs and ENABLE are satisfied. Once all 4 UVLO inputs and ENABLE are satisfied for 10ms, the four DLY_ON capacitors are simultaneously charged with 1µA current sources to the DLY_Vth level of 1.28V. As each DLY_ON pin reaches the DLY_Vth level, its associated GATE will then turn-on with a 10µA source current to the VQP voltage of V_{DD} + 5.6V. Thus, all four GATEs will sequentially turn on. Once at DLY_Vth the DLY_ON pins will discharge to be ready when next needed. After the entire turn on sequence has been completed and all GATEs have reached the charge pumped voltage (VQP), a 160ms delay is started to ensure stability after which the $\overline{RESET}$ output will be released to go high. Subsequent to turn-on, if any input falls below its UVLO point for longer than the glitch filter period, t_{FIL} (~7µs) this is considered a fault. $\overline{RESET}$, $\overline{SYSRST}$ and all GATEs are simultaneously pulled low. In this mode the GATEs are pulled low with ~75mA. Normal shutdown mode is entered when no UVLO is violated and the ENABLE is deasserted. When ENABLE is deasserted, $\overline{RESET}$ is asserted and pulled low. Next, all four shutdown ramp capacitors on the DLY_OFF pins are charged with a 1µA source and when any ramp-capacitor reaches DLY_Vth, a latch is set and a 10µA current is sunk on the respective GATE pin to turn off its external MOSFET. When the falling GATE voltage is approximately 1.5V, the GATE is pulled down the rest of the way at a higher current level to ensure a hard turn-off. Each individual external FET is thus turned off removing the voltages from the load in the programmed sequence. The $\overline{SYSRST}$ will pull low concurrent with the last GATE being pulled low.

The ISL8723 and ISL8724 have the same functionality except for the complimentary ENABLE active polarity with the ISL8724 having an $\overline{ENABLE}$ input. Additionally, the ISL8723 also has a low power sleep state when disabled.

Upon bias, the $\overline{SYSRST}$ and $\overline{RESET}$ pins are held low before bias voltage = 1V.

The $\overline{SYSRST}$ has both an input and output function. As an output, the $\overline{SYSRST}$ pin is useful when implementing multiple sequencers in a design needing simultaneous shutdown as with a kill switch across all sequencers. Once any UVLO is unsatisfied for longer than t_{FIL}, the related $\overline{SYSRST}$ will pull low and pull all other $\overline{SYSRST}$ pins low

that are on a common connection thus unconditionally shutting down all outputs across multiple sequencers. As an input, if it is pulled low all GATEs will be unconditionally shut off and $\overline{\text{RESET}}$ pulled low (see Figure 18). This pin can also be used as a 'no wait' enabling input if all inputs (ENABLE and UVLO) are satisfied; it does not wait through the ~10ms enable delay to initiate the DLY_ON capacitor charging when released to go high. This feature can be used where 4 voltages can be monitored in addition to a on-off switch position or, in the case of the ISL8724, a present pin pull-down.

Restart of the turn on sequence is automatic once all requirements are met. This allows for no interaction between the sequencer and a controller IC if so desired. If no capacitors are connected between DLY_ON or DLY_OFF pins and ground then all such related GATEs start to turn on immediately after the 10ms ($t_{UVLOdel}$) ENABLE stabilization time out has expired and the GATEs start to immediately turn off when ENABLE is deasserted.

Table 1 illustrates the nominal time delay from the start of charging to the 1.27V reference for various capacitor values on the DLY_X pins. This table does not include the 10ms of enable lock out delay during a start-up sequence but represents the time from the end of the enable lock out delay to the start of GATE transition. There is no enable lock out delay for a sequence off, so this table illustrates the delay to GATE transition from a disable signal.

TABLE 1.

NOMINAL DELAY TO SEQUENCING THRESHOLD	
DLY PIN CAPACITANCE	**TIME (ms)**
Open	0.02
100pF	0.135
1000pF	1.35
0.01µF	13.5
0.1µF	135
1µF	1350

NOTE: Nom. T_{DEL_SEQ} = dly_cap (µF)x1.35MΩ

Figure 3 illustrates the turn-on and Figure 4 the nominal turnoff timing diagrams of the **ISL8723** and **ISL8724** product.

Note the delay and flexible sequencing possibilities. Multiple series, parallel or adjustable capacitors can be used to easily fine tune timing between that offered by standard value capacitors.

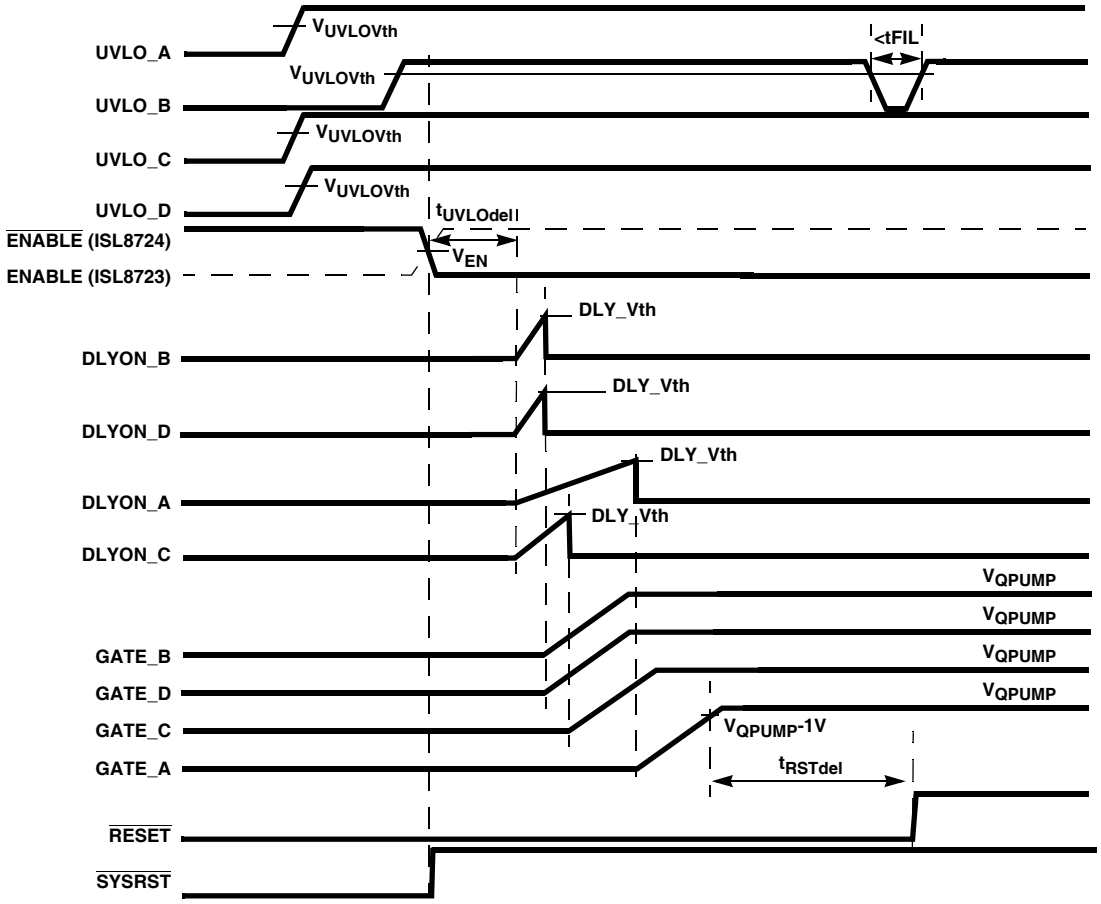


FIGURE 3. ISL8723, ISL8724 TURN-ON AND GLITCH RESPONSE TIMING DIAGRAM

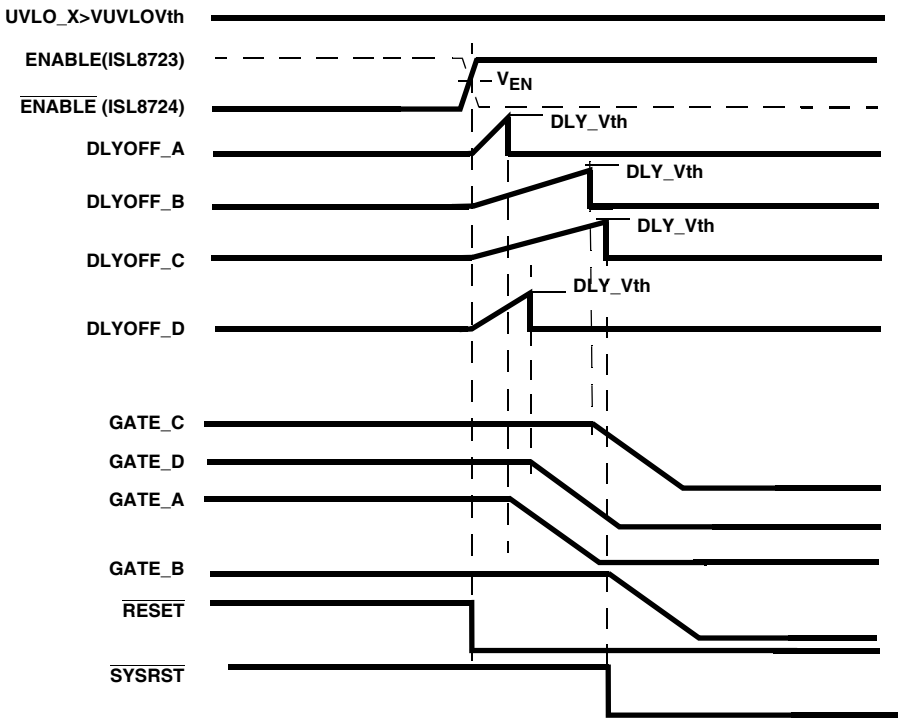


FIGURE 4. ISL8723, ISL8724 TURN-OFF TIMING DIAGRAM

Typical Performance Curves

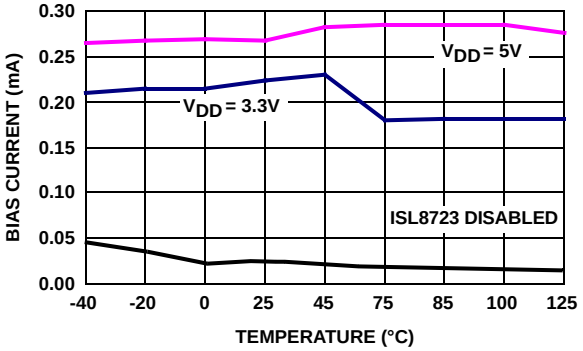


FIGURE 5. BIAS CURRENT

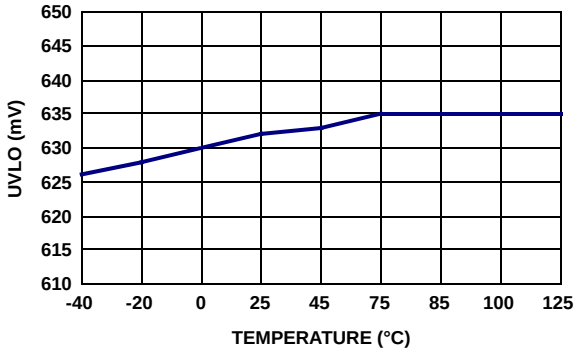


FIGURE 6. UVLO THRESHOLD VOLTAGE

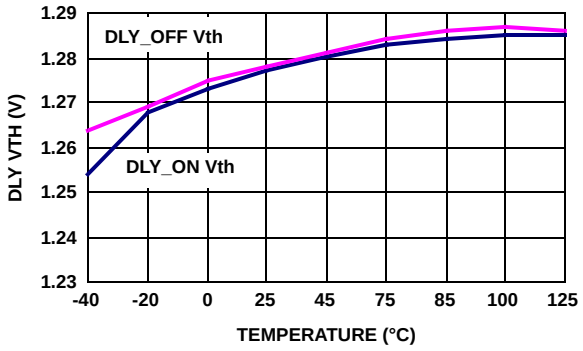


FIGURE 7. DLY THRESHOLD VOLTAGE

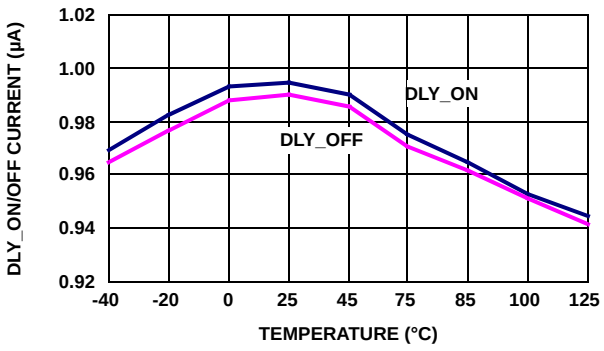


FIGURE 8. DLY CHARGE CURRENT

Typical Performance Curves (Continued)

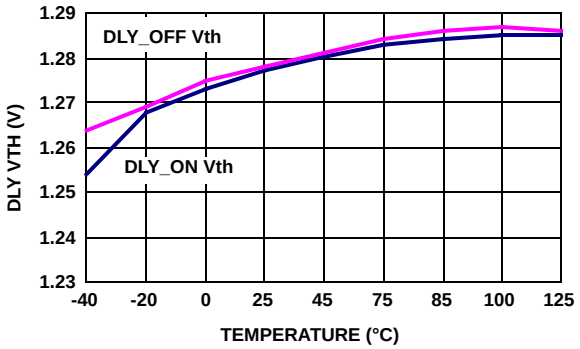


FIGURE 9. BIAS POWER ON RESET

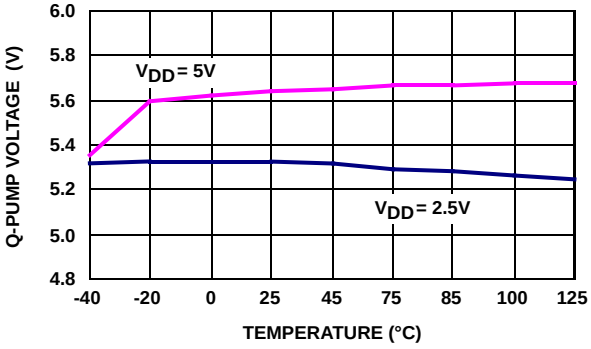


FIGURE 10. CHARGE PUMP VOLTAGE

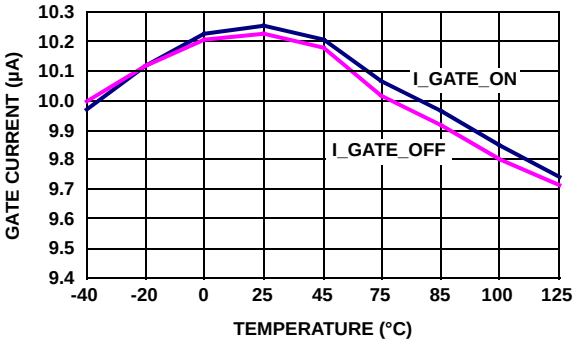


FIGURE 11. GATE TURN-OFF/ON (DIS)CHARGE CURRENT

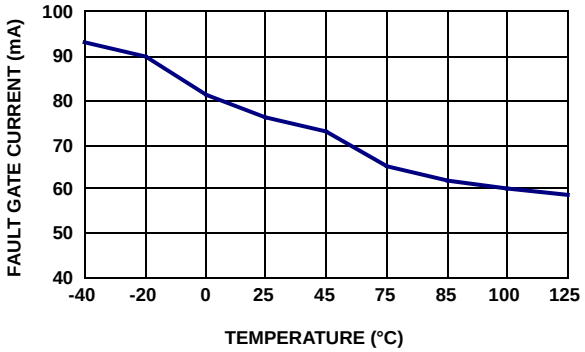


FIGURE 12. FAULT GATE TURN-OFF SINK CURRENT

Using the ISL8723EVAL1 Platform

The **ISL8723EVAL1** platform allows evaluation of the ISL8723, easily providing access to the critical nodes (see Figure 22 for schematic and Figure 23 for a photograph of the evaluation platform).

The board has a SMD layout with a **ISL8723** illustrating the possible small implementation size for a typical four rail sequencing application. There are bias and function labeled test points to give access to the IC pins for evaluation. Remember that significant current or capacitive loading of particular I/O pins will affect functionality and performance.

The default configuration of the **ISL8723EVAL1** circuit was built around the following design assumptions:

1. Using the **ISL8723IR**
2. The four supplies being sequenced are 5V (IN_A), 3.3V (IN_B), 2.5V (IN_D) and 1.5V (IN_C), the UVLO levels are ~80% of nominal voltages. Resistors chosen such that the total resistance of each divider is ~ 10k using standard value resistors to approximate 80% of nominal voltage supply = 0.63V on UVLO input.
3. The desired order turn-on sequence is 5V first, then 3.3V about 12ms later then the 2.5V supply about 19ms later and lastly the 1.5V supply about 40ms later.
4. The desired turn-off sequence is first the 2.5V, the 3.3V 12ms later, then the 1.5V supply about 36ms later and lastly the 5V supply about 72ms after that.
5. LED off indicates sequence has completed and $\overline{\text{RESET}}$ has released and pulled high.

All scope shots are taken from ISL8723EVAL1 board. Figures 13 and 14 illustrate the desired turn-on and turn-off sequences respectively. The sequencing order and delay between voltages sequencing is set by external capacitance values so other than that illustrated can be accomplished.

Figures 15 and 16 illustrate the timing relationships between the EN input, $\overline{\text{RESET}}$, DLY and GATE outputs and the VOUT voltage for a single channel being turned on and off respectively.

$\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ functionality and relationships are shown in Figures 17 through 21.

Figure 17 illustrates that with a rising VDD, EN tied to VDD, and all UVLO configured to be satisfied, both the $\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ are held low before V_{DD} = 1V. $\overline{\text{SYSRST}}$ is released to go high once the last UVLO is satisfied and $\overline{\text{RESET}}$ is released to go high at $t_{\overline{\text{RST}}\text{del}}$ after the last GATE is high.

Figure 18 shows GATE and $\overline{\text{RESET}}$ response to $\overline{\text{SYSRST}}$ being pulled low.

Figure 19 shows EN high to $\overline{\text{SYSRST}}$ delay with all UVLO inputs satisfied.

Figure 20 shows $\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ delay to EN pulled low.

Figure 21 shows ~8µs of glitch filter duration, t_{FIL} during which the $\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ do not react.

Typical Performance Waveforms

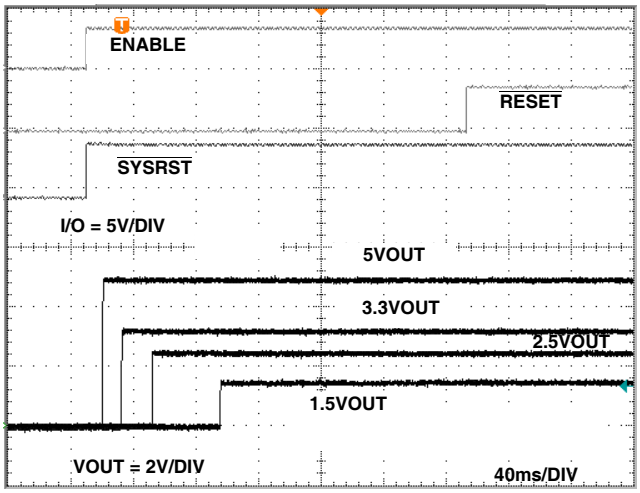


FIGURE 13. ISL8723 SEQUENCED TURN-ON

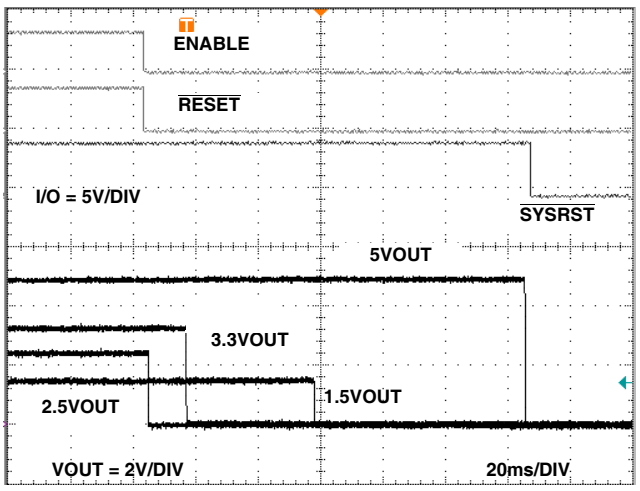


FIGURE 14. ISL8723 SEQUENCED TURN-OFF

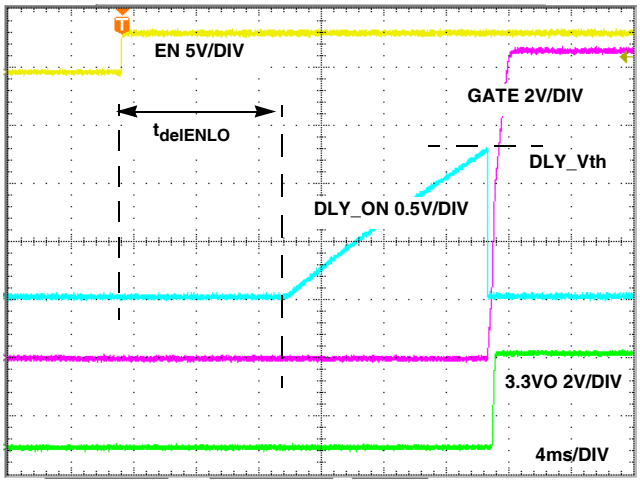


FIGURE 15. ISL8723 3.3V TURN-ON

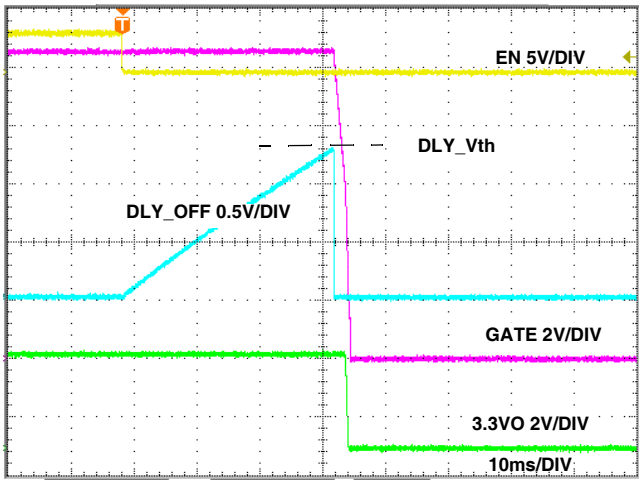


FIGURE 16. ISL8723 3.3V TURN-OFF

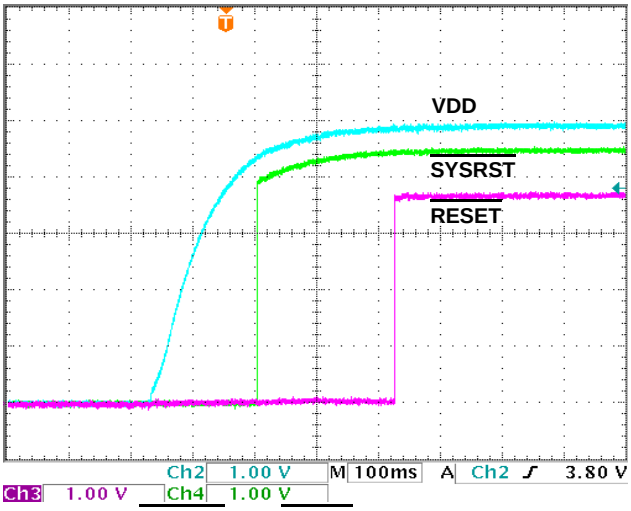


FIGURE 17. SYSRST AND RESET vs VDD (EN = VDD, 4 UVLO > UVLO Vth)

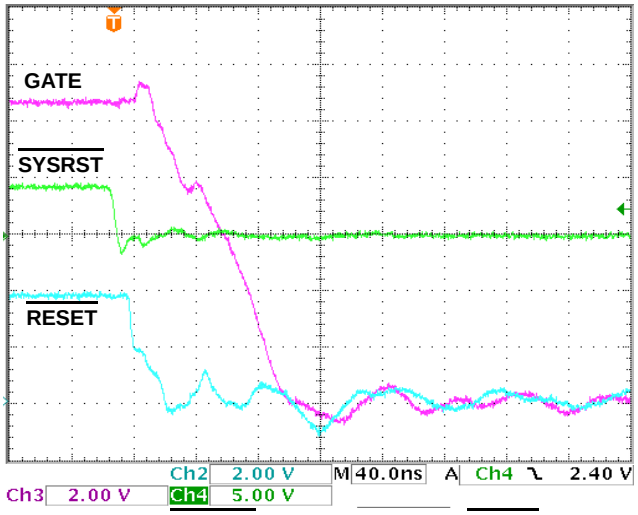


FIGURE 18. SYSRST LOW TO GATE AND RESET LOW

Typical Performance Waveforms (Continued)

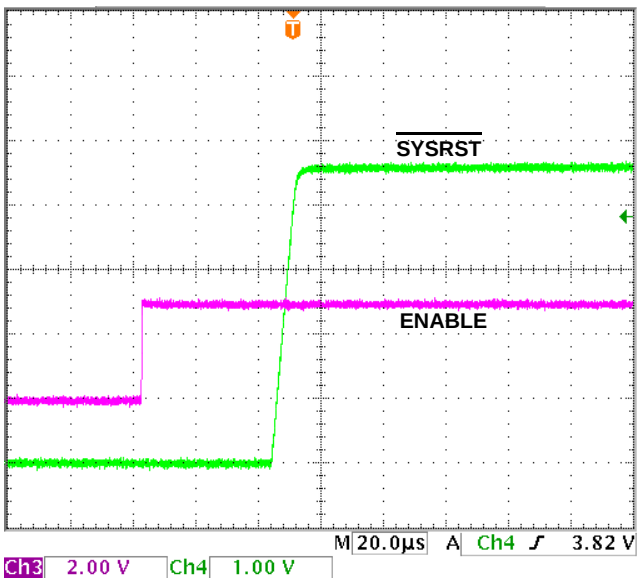


FIGURE 19. 4 UVLOs VALID, ENABLE HIGH TO SYSRST HIGH

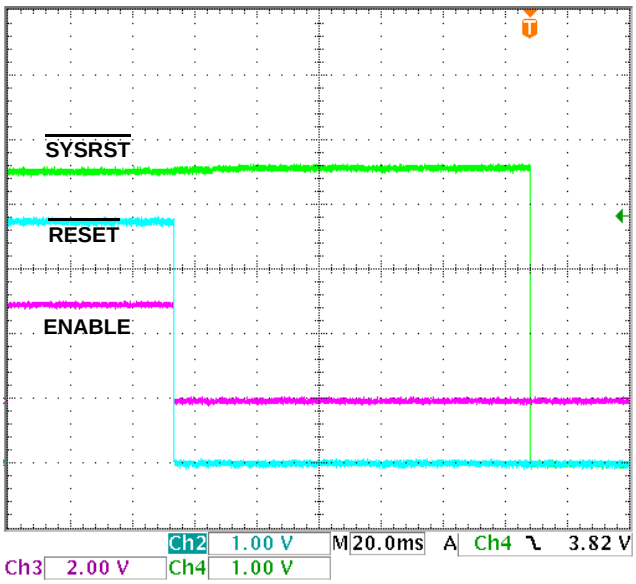


FIGURE 20. ENABLE LOW TO $\overline{\text{RESET}}$ AND SYSRST LOW

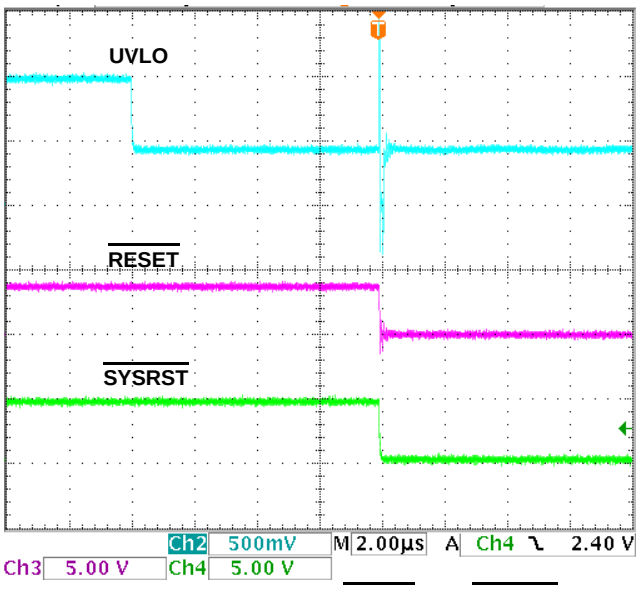


FIGURE 21. UVLO INVALID TO $\overline{\text{RESET}}$ AND $\overline{\text{SYSRST}}$ LOW

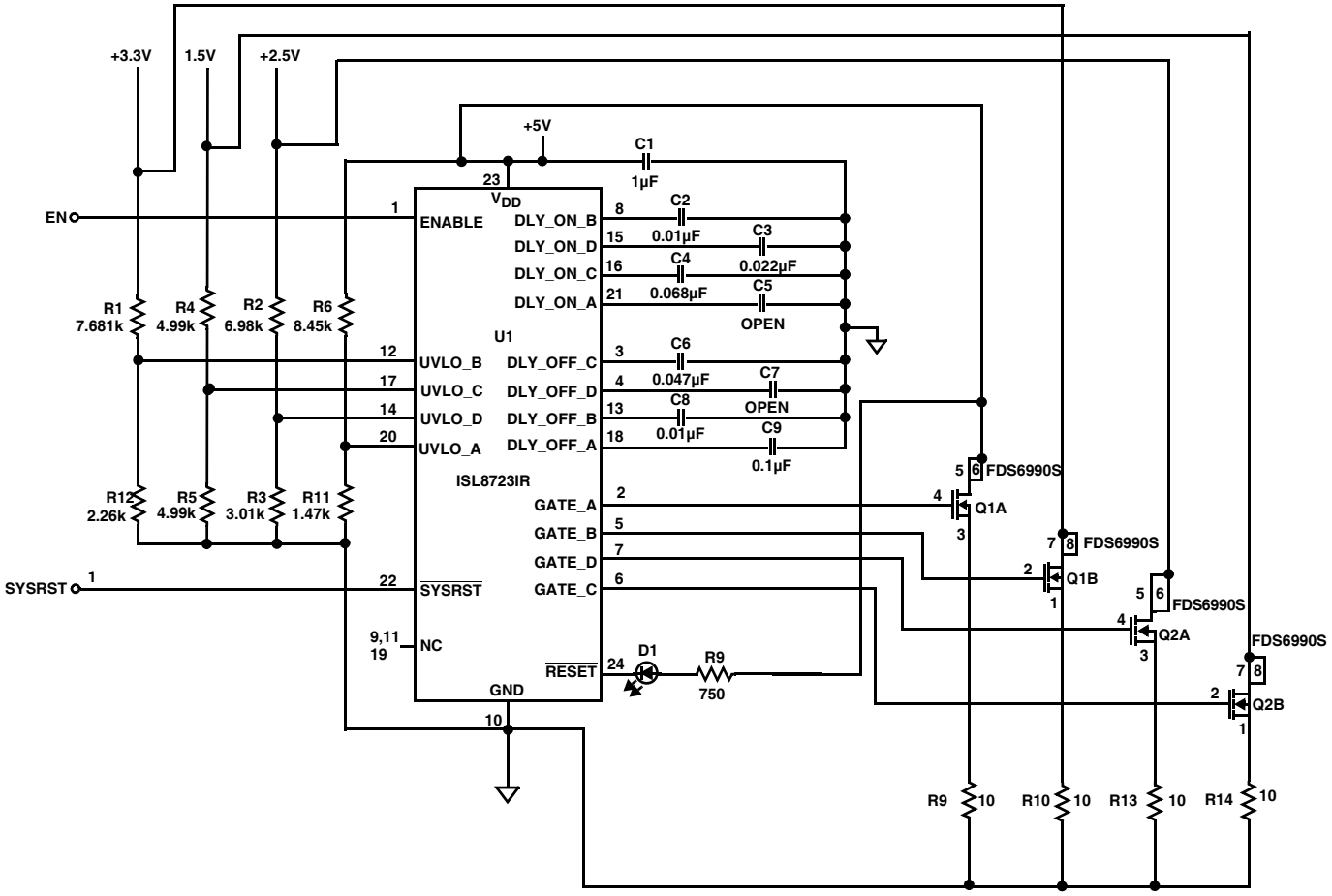


FIGURE 22. ISL8723EVAL1 BOARD SCHEMATIC

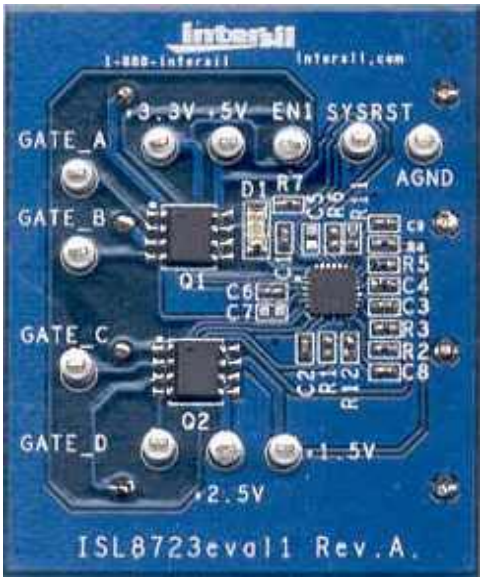


FIGURE 23. EVAL BOARD PHOTOGRAPH

TABLE 2. ISL872XSEQEVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	**ISL8723**, 4 Supply Sequencer	Intersil, **ISL8723IR** 4 Supply Sequencer
Q1, Q2	Voltage Rail Switches	FDS6990S or equivalent, Dual N-Channel MOSFET
R6	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R11	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R12	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R2	2.5V to UVLO_D Resistor for Divider String	6.98kΩ 1%, 0402
R3	UVLO_D to GND Resistor for Divider String	3.01kΩ 1%, 0402
R4	1.5V to UVLO_C Resistor for Divider String	4.99kΩ 1%, 0402
R5	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	RESET LED Current Limiting Resistor	750Ω 10%, 0805
C5	5V turn-on Delay Capacitor A (~10ms)	DNP, 0402
C9	5V turn-off Delay Capacitor A (~140ms)	0.1µF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Capacitor B (~13ms)	0.01µF 10%, 6.3V, 0402
C8	3.3V turn-off Delay Capacitor B (~13ms)	0.01µF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Capacitor D (~25ms)	0.022µF 10%, 6.3V, 0402
C7	2.5V turn-off Delay Capacitor D (0ms)	DNP, 0402
C4	1.5V turn-on Delay Capacitor C (~100ms)	0.068µF 10%, 6.3V, 0402
C6	1.5V turn-off Delay Capacitor C (~60ms)	0.047µF 10%, 6.3V, 0402
C1	Decoupling Capacitor	1µF, 0805
D1	RESET Indicating LED	0805, SMD LEDs Red
R9	5V Load Resistor	10Ω 20%, 3W Carbon
R10	3.3V Load Resistor	10Ω 20%, 3W Carbon
R13	2.5V Load Resistor	10Ω 20%, 3W Carbon
R14	1.5V Load Resistor	10Ω 20%, 3W Carbon
	Test Points Labeled as to Function	

Application Implementations

Multiple Sequencer Implementations

In order to control the sequencing of more than 4 voltages in applications where the integrity of these critical voltages must be assured prior to sequencing, several of the ISL8723 or ISL8724 devices can configured together to accomplish this.

Figure 24 shows a typical multi sequencer implementation; note the common $\overline{\text{SYSRST}}$ signal that asserts once all monitored voltages are valid allowing the sequence to initiate. The sequencing is straight forward across multiple sequencers as all DLY_ON capacitors will simultaneously start charging once all monitored voltages area valid and ~10ms after the common ENABLE input signal is delivered. This allows the choice of capacitors to be related to each other no different than using a single sequencer. When the common enabling signal is deasserted, this configuration will then execute the turn-off sequence across all sequencers as programmed by the DLY_OFF capacitor values.
With all the $\overline{\text{SYSRST}}$ pins bused together, once the on sequence is complete, simultaneous shutdown upon any UVLO input failure is assured as the $\overline{\text{SYSRST}}$ output will pull low, simultaneously turning off all GATE outputs.

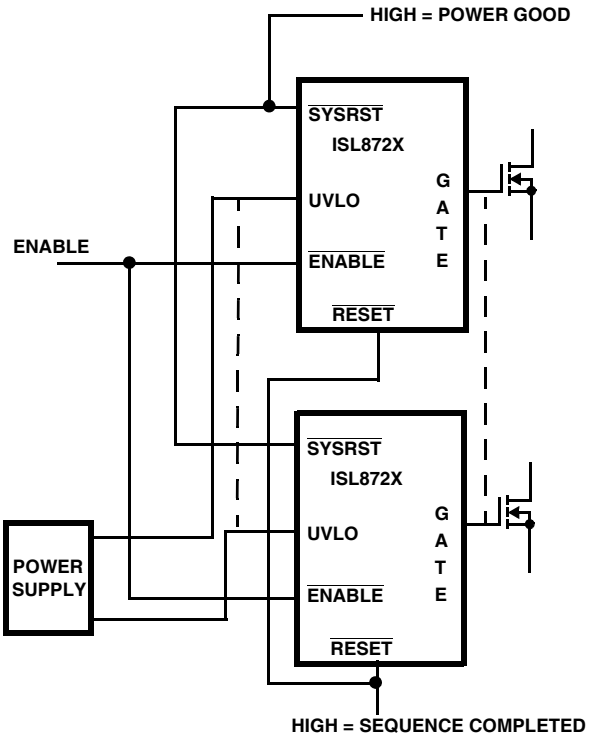


FIGURE 24. MULTIPLE ISL872X CONFIGURATION

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

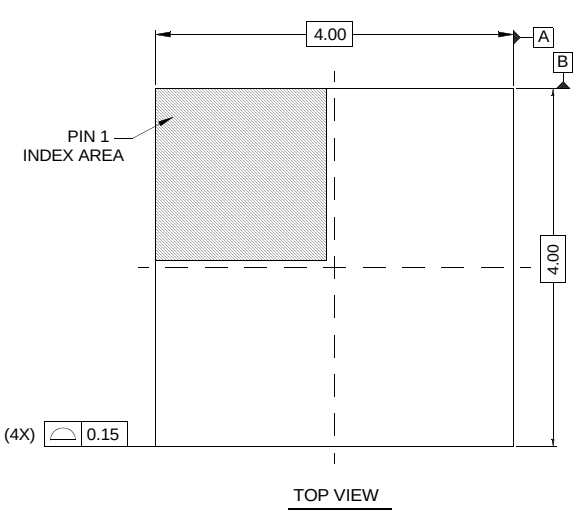
Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

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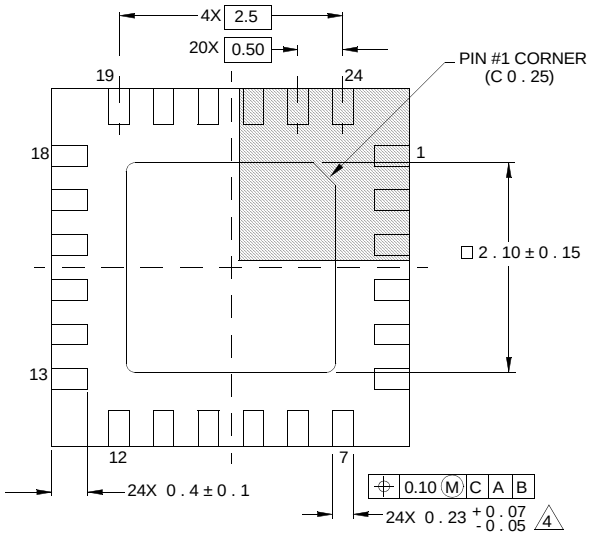
Package Outline Drawing

L24.4x4

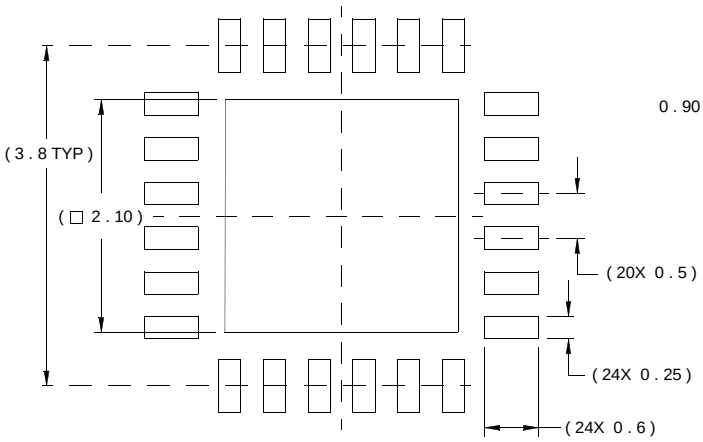
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



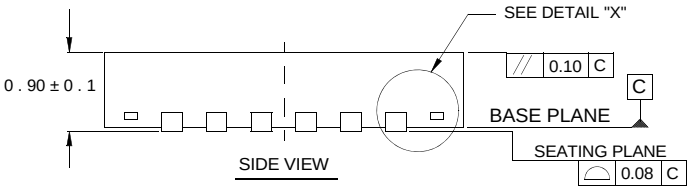
TOP VIEW



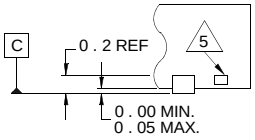
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.