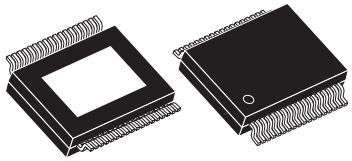
STA559BWQS

5-V, 2-A, 2.1-channel high-efficiency digital audio system with QSound QHD®

Features

- Wide supply voltage range (4.5 - 9 V)
- 3 Power output configurations:
  - 2 channels of ternary PWM (stereo mode) (2 x 3 W) into 4 Ω at 5 V
  - 3 channels - left,right using binary and LFE using ternary PWM (2.1 mode) (2 x 0.7 W + 1 x 3 W) into 4 Ω at 5 V (2 x 1.4 W + 1 x 6 W) into 2 Ω at 5 V
  - 2 channels of ternary PWM (2 x 3 W) + PWM driver for SW
- 2.1 channels of 24-bit DDX®
- 100-dB SNR and dynamic range
- Selectable 32 kHz to 192 kHz input sample rates
- I^2C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB in 0.5-dB steps
- Soft volume update
- Individual channel and master gain/attenuation
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- AutoModes
  - 15 preset crossover filters
  - 2 preset anti-clipping modes
  - Preset night-time listening mode
- Individual channel and master soft and hard mute
- Independent channel volume and DSP bypass



PowerSSO-36 slug down

- Automatic zero-detect mute
- Automatic invalid input detect mute
- 2-channel I^2S input data interface
- Input and output channel mapping
- 4 28-bit user programmable biquads (EQ) per channel
- DC blocking selectable high-pass filter
- Selectable de-emphasis
- Sub channel mix into left and right channels
- Advanced AM interference frequency switching and noise-suppression modes
- Selectable high or low bandwidth noise-shaping topologies
- Variable max power correction for lower full-power THD
- Thermal overload and short-circuit protection
- Video application supports 576 x fs input mode
- QSound QHD®
  - Field proven stereo soundfield enhancement technology
  - Provides improved audio image width, seperation and depth for stereo signals
  - Synthesizes a 3-D stereo soundfield
- PowerSSO-36 slug down package

Table 1. Order codes

Part number	Temp range, °C	Package	Packing
STA559BWQS	0 to 150	PowerSSO-36 slug down	Tube
STA559BWQS13TR	0 to 150	PowerSSO-36 slug down	Tape&Reel

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1 Description and block diagram

1.1 Description

The STA559BWQS is an integration of digital audio processing, digital amplifier control, DDX® power-output stage and QSound QHD® technology to create a high-power single-chip DDX solution with high-quality, high-efficiency and all digital amplification.

The STA559BWQS power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. 2.1 channels can be provided by two half-bridges and a single full-bridge, providing up to 2 x 0.7 W + 1 x 3 W of power output. 2 channels can be provided by two full-bridges, providing up to 2x3W of power. The IC can also be configured as a 2.1 channels with 2 x 3 W provided by the device and external power for DDX® power drive. Also provided in the STA559BWQS are a full assortment of digital processing features. This includes up to 4 programmable 28-bit biquads (EQ) per channel, and bass/treble tone control. AutoModes enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions, for instance, auto volume loudness, preset volume curves and preset EQ settings. New advanced AM radio interference reduction modes. The serial audio data input interface accepts all possible formats, including the popular I^2S format. Three channels of DDX® processing are provided. This high quality conversion from PCM audio to DDX patented 3-state PWM switching waveform provides over 100 dB of SNR and dynamic range.

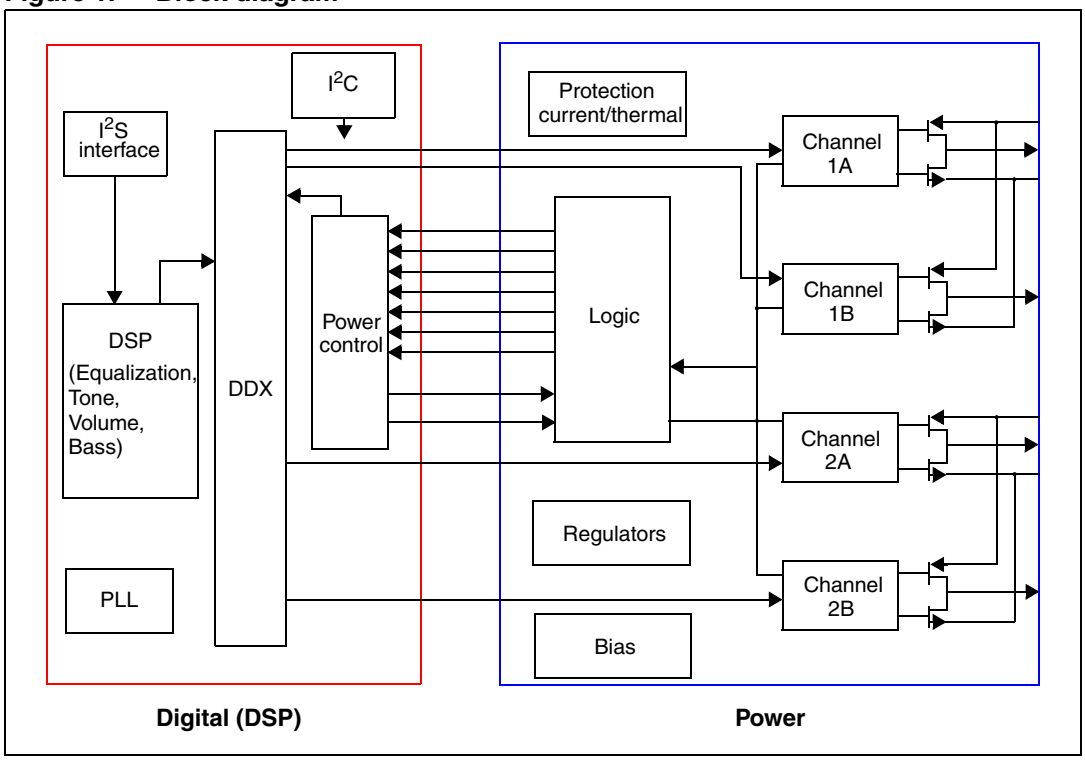
1.2 QSound QHD®

Normally, reduced audio clarity is experienced due to the digital compression of music (and video-sound) combined with various audio processing techniques used in broadcast transmission. This is most apparent in products such as digital televisions and audio players. These devices are faced with a multitude of audio challenges, primarily associated with the small speakers, that are limited in location and cabinet housing, plus economized speaker drivers and components. As such digital televisions and audio players are ideal candidates to benefit from stereo soundfield enhancement in order to deliver a full surround-like experience.

QSound QHD® and its industry recognized QXpander® technology is a field-proven stereo soundfield enhancement technology that provides a broader stereo image width with greater separation and depth for stereo signals and synthesizes a 3-D stereo soundfield. QHD® removes the small centralized audio sweet spot by creating a very wide stereo image with full immersive audio. QHD® and its QXpander® technology have been incorporated into hundreds of QSound and third party hardware and software products, with total shipments in the millions.

1.3 Block diagram

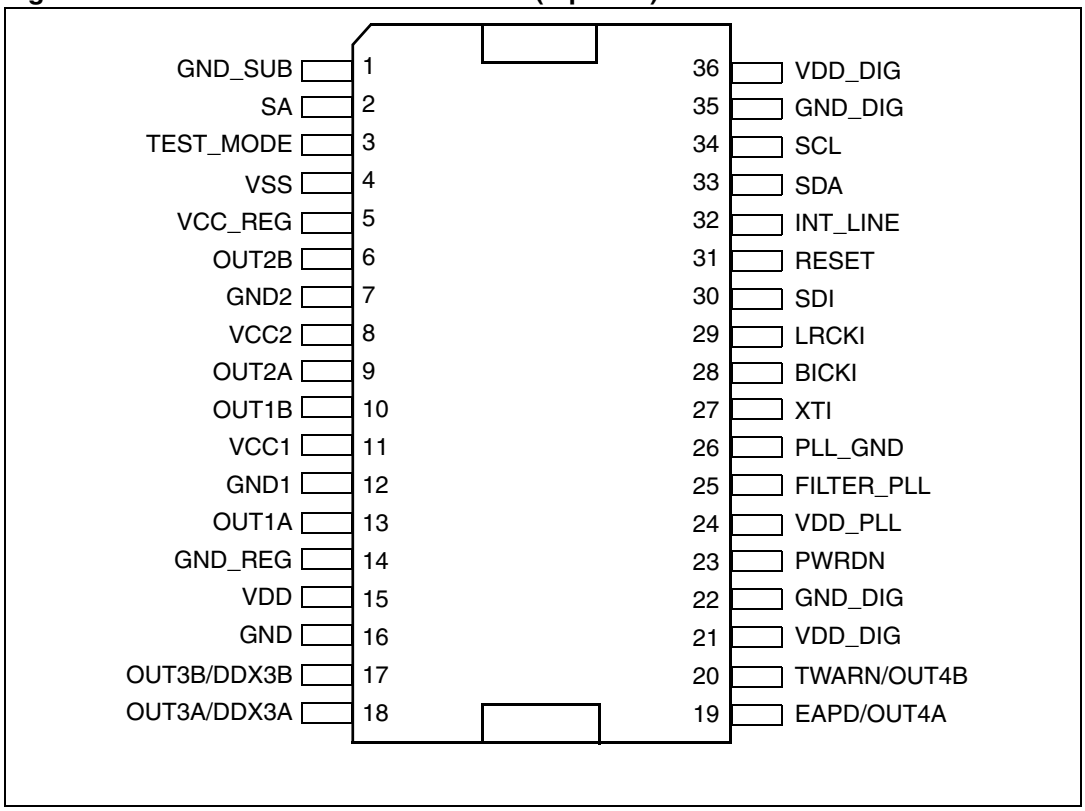
Figure 1. Block diagram



2 Connections diagram and pins description

2.1 Connections diagram

Figure 2. Pin connection PowerSSO-36 (top view)



2.2 Pins description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I^2C select address
3	I	TEST_MODE	This pin must be connected to ground
4	I/O	VSS	Internal reference at Vcc - 3.3 V
5	I/O	VCC_REG	Internal Vcc reference
6	O	OUT2B	Output half bridge 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A

Table 2. Pin description (continued)

Pin	Type	Name	Description
10	O	OUT1B	Output half bridge 1B
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	I/O	OUT1A	Output half bridge 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I/O	GND	Power negative supply
17	O	OUT3B/DDX3B	PWM out CH3B - external bridge
18	O	OUT3A/DDX3A	PWM out CH3A - external bridge
19	O	EAPD/OUT4A	Power down for external bridge
20	I	TWARN/OUT4B	Thermal warning from external bridge
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I^2S serial clock
29	I	LRCKI	I^2S left/right clock
30	I	SDI	I^2S serial data channels 1 and 2
31	I	RESET	Reset
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I^2C serial data
34	I	SCL	I^2C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient PowerSSO-36 (1)		24		°C/W
$T_{th\text{-}sdj}$	Thermal shut-down junction temperature		150		°C
$T_{th\text{-}w}$	Thermal warning temperature		130		°C
$T_{th\text{-}sdh}$	Thermal shut-down hysteresis temperature		25		°C

1. See *Chapter 7: Package thermal characteristics on page 61* for details.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{cc}	Power supply voltage (VCC1, VCC2)			18	V
Vdd	Logic supply	-0.3		4	V
T_{op}	Operating junction temperature	-20		150	°C
T_{stg}	Storage temperature	-40		150	°C

Note: Stresses beyond those listed under "Absolute maximum ratings" make cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating condition" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supply with nominal value rated inside recommended operating conditions, may experience some rising beyond the maximum operating condition for short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum rating is not exceeded.

3.2 Recommended operating condition

Table 5. Recommended operating condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{cc}	Power supply voltage (VCC1, VCC2)	5.0		16.0	V
Vdd	Logic supply	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	-20		70	°C

3.3 Electrical specifications - digital section

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low level input current without pull device	Vi = 0 V	-10		10	µA
I_{ih}	High level input current without pull device	Vi = VDD_DIG = 3.6 V	-10		10	µA
V_{il}	Low level input voltage				0.2 * VDD_DIG	V
V_{ih}	High level input voltage		0.8 * VDD_DIG			V
V_{ol}	Low level output voltage	I_{ol} = 2 mA			0.4 * VDD_DIG	V
V_{oh}	High level output voltage	I_{oh} = 2 mA	0.8 * VDD_DIG			V
I_{pu}	Pull current		-25	66	125	µA
R_{pu}	Equivalent pull resistance			50		kΩ

3.4 Electrical specifications - power Section

The specifications given in this section are with the operating conditions VCC = 5 V, f_{sw} = 384 kHz, T_{amb} = 25° C, R_L = 4 Ω unless otherwise specified.

Table 7. Electrical specifications - power Section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET RdsON	Id = 1 A		180	250	mΩ
I_{dss}	Power Pchannel/Nchannel leakage Idss	Vcc = 9 V			10	µA
g_P	Power Pchannel RdsON Matching	Id = 1 A	95			%
g_N	Power Nchannel RdsON Matching	Id = 1 A	95			%
I_{LDT}	Low current dead time (static)	Resistive load(1)		5	10	ns
I_{HDT}	High current dead time (dynamic)	I_{load} = 2 A(2)		10	20	ns
t_r	Rise time	Resistive load(1)		8	10	ns
t_f	Fall time	Resistive load(1)		8	10	ns
V_{cc}	Supply operating voltage		4.5		16	V
I_{cc}	Supply current from Vcc in power down	Power Down = 0			10	µA
	Supply current from Vcc in 3-state	TRISTATE = 0		15		mA
	Supply current from Vcc in operation	PCM input signal = -60 dBFS Switching frequency = 384 kHz No LC filters		30		mA
	Supply current DDX processing (reference only) on VDD_DIG	Internal clock = 49.152 MHz		80		mA

Table 7. Electrical specifications - power Section (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Ilim	Overcurrent limit			2.2	3.0		A
Isc	Short circuit protection			2.7	3.6		A
UVL	Under voltage protection threshold				3.5	4.3	V
t_{min}	Output minimum pulse width	No Load		20	30	60	ns
Po	Output power BTL	THD = 1%, f = 1 kHz			2.3		W
		THD = 10%, f = 1 kHz			3		
	Output power SE	THD = 1%, f = 1 kHz			0.5		W
		THD = 10%, f = 1 kHz			0.7		
	Output power BTL	R_L = 8 Ω Vcc = 9 V f = 1 kHz	THD = 1%		4.2		W
			THD = 10%		5.3		
	Output power SE		THD = 1%		0.9		W
			THD = 10%		1.2		
	Output power BTL	R_L = 2 Ω Vcc = 5 V f = 1 kHz	THD = 1%		4.2		W
			THD = 10%		5.3		
	Output power SE		THD = 1%		1		W
			THD = 10%		1.3		
SNR	Signal to noise ratio, ternary mode	A-weighted			100		dB
	Signal to noise ratio binary mode				90		
PSSR	Power Supply Rejection Ratio	Stereo DDX mode, <5 kHz V_{RIPPLE} = 1 V RMS Audio input = dither only			80		dB
THD+N	Total harmonic distortion + noise	DDX stereo mode, Po = 1 W, f = 1 kHz			0.2		%
X_{TALK}	Crosstalk	Stereo DDX mode, <5 kHz One channel driven @ 1 W Other channel measured			80		dB
η	Peak efficiency, DDX mode	Po = 2 x 3 W, 4 Ω			90		%
	Peak efficiency, Binary modes	Po = 2 x 0.7 W + 1 x 3 W, 4 Ω			87		

1. Refer to Test Circuit 1 *Figure 3*
2. Refer to Test Circuit 2 *Figure 4*

3.5 Testing

3.5.1 Functional pin status

Table 8. Functional pin status

Pin name	Pin #	Logic value	IC status
PWRDN	23	0	Low absorption
PWRDN	23	1	Normal operation
TWARN	20	0	From external power stage is indicated a temperature warning.
TWARN	20	1	Normal operation
EAPD	19	0	Low absorption for power stage. All internal regulators are switched off.
EAPD	19	1	Normal operation

Figure 3. Test circuit 1

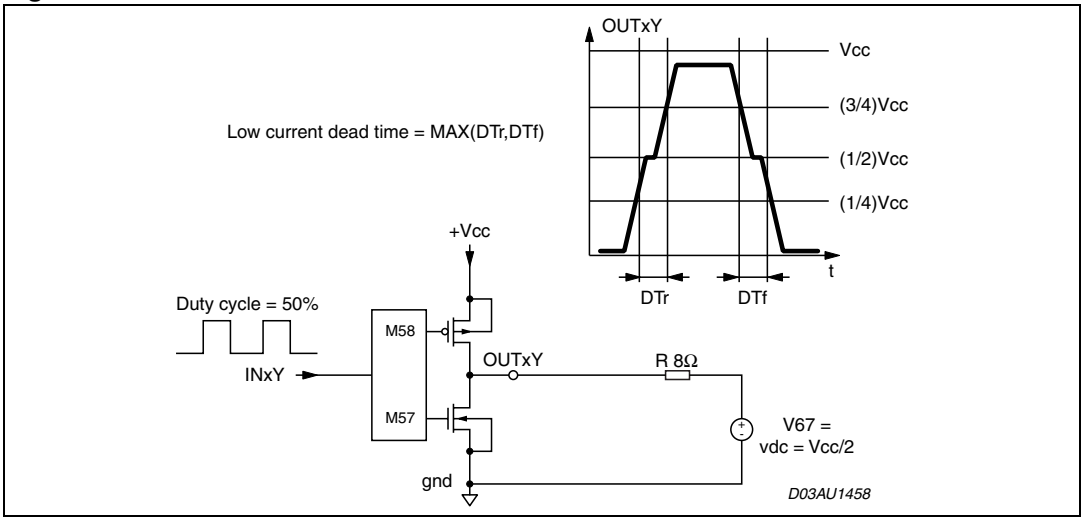
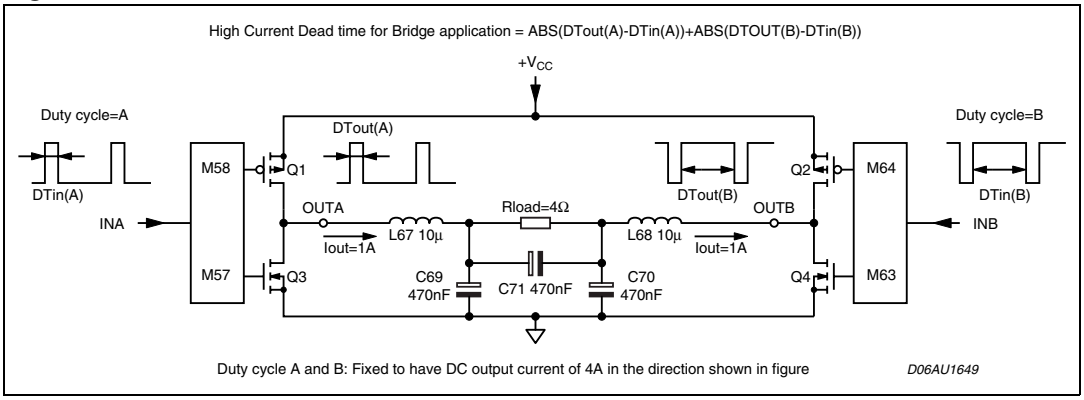


Figure 4. Test circuit 2



3.6 Electrical characteristics curves

Figure 5. Output power vs supply voltage (R_L = 2 Ω)

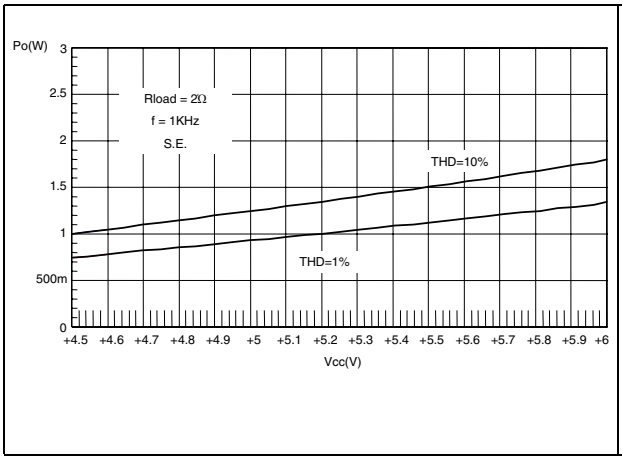


Figure 6. Output power vs. supply voltage (R_L = 2 Ω)

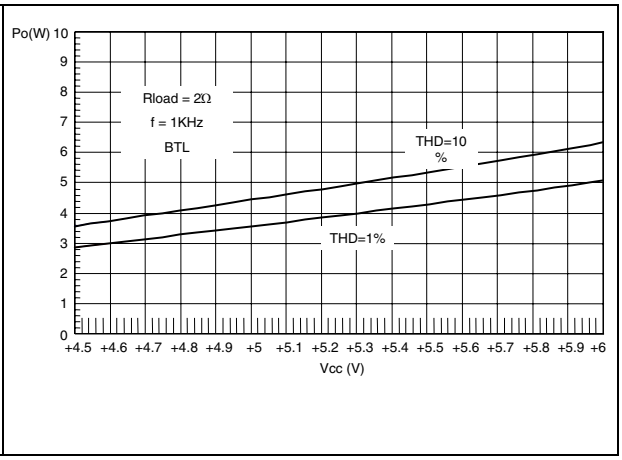


Figure 7. Output power vs. supply voltage (R_L = 4 Ω)

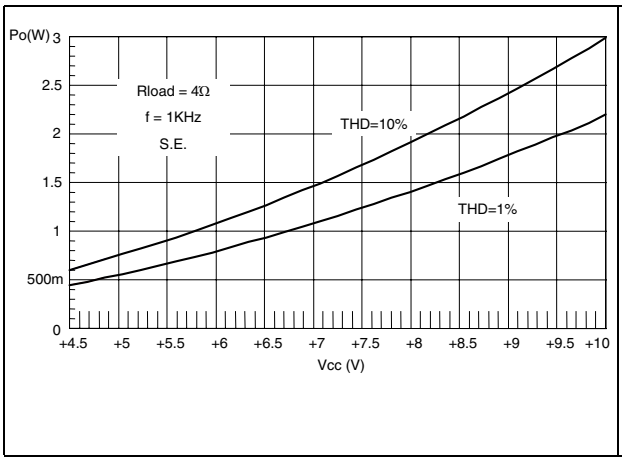


Figure 8. Output power vs. supply voltage (R_L = 4 Ω)

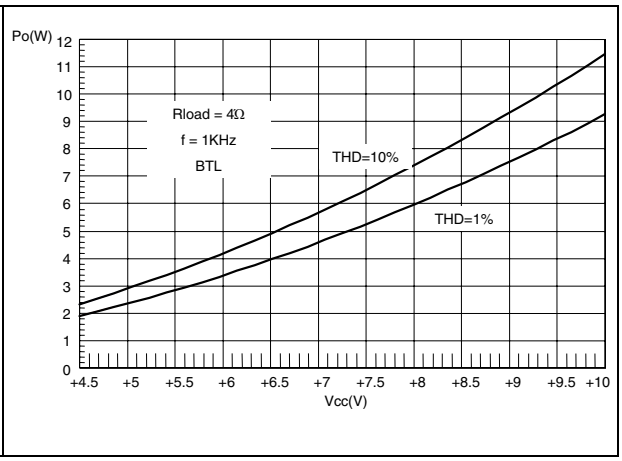


Figure 9. Output power vs. supply voltage (R_L = 6 Ω)

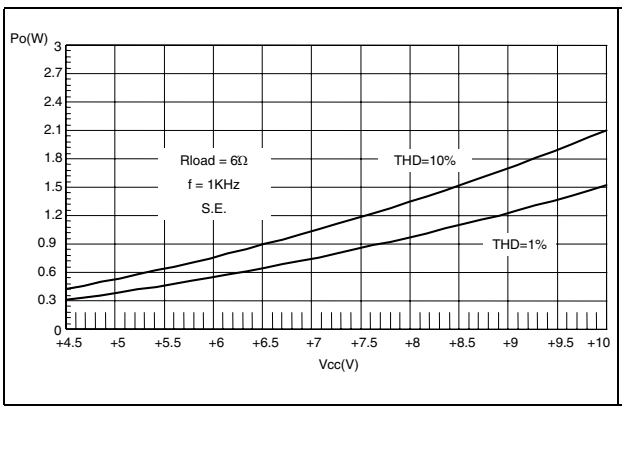


Figure 10. Output power vs. supply voltage (R_L = 6 Ω)

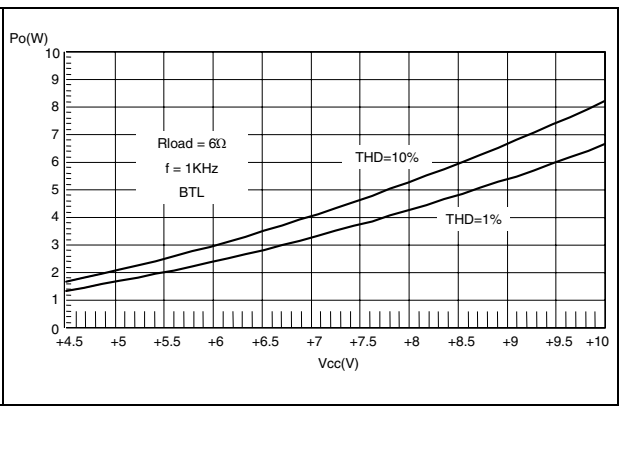


Figure 11. Output power vs. supply voltage (R_L = 8 Ω)

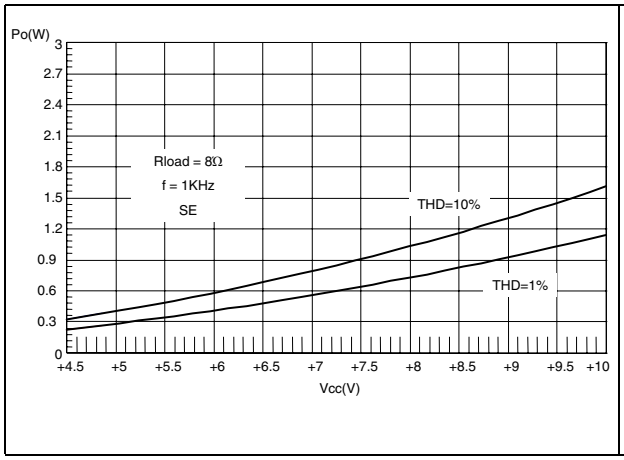


Figure 12. Output power vs. supply voltage (R_L = 8 Ω)

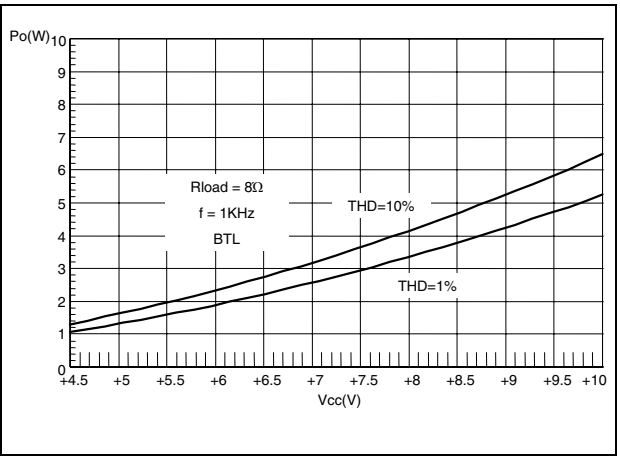


Figure 13. Efficiency vs. P_{out} (Vcc = 9 V; R_L = 8 Ω)

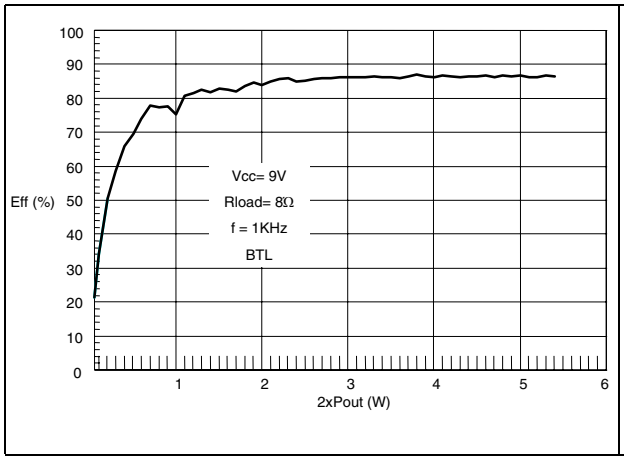


Figure 14. Efficiency vs. P_{out} (Vcc = 5 V; R_L = 4 Ω)

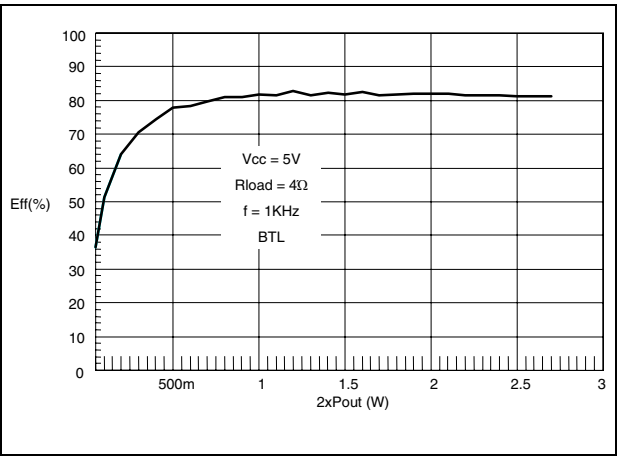


Figure 15. Efficiency vs. P_{out} (Vcc = 5 V; R_L = 2 Ω)

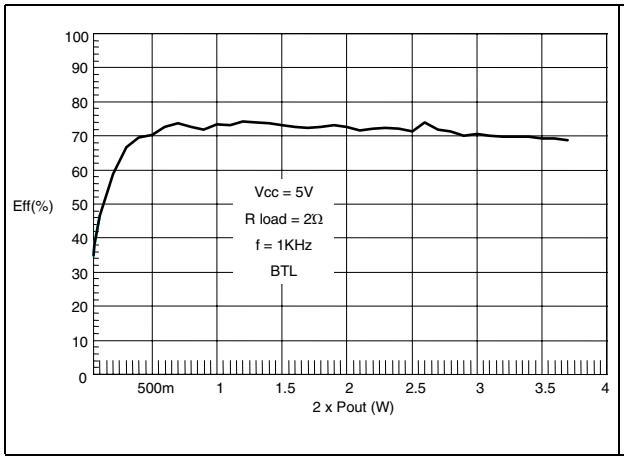


Figure 16. THD vs. frequency

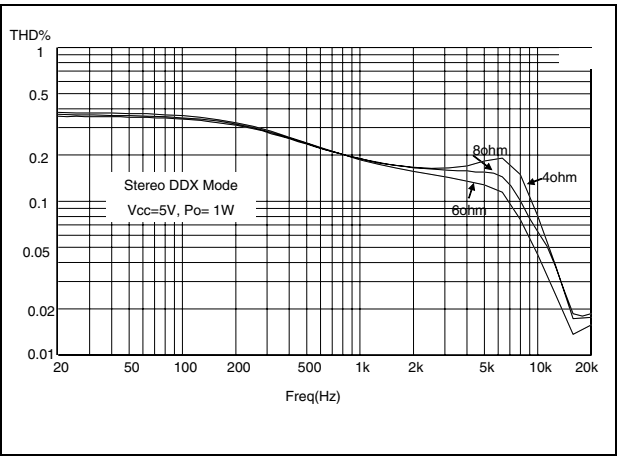


Figure 17. PSSR

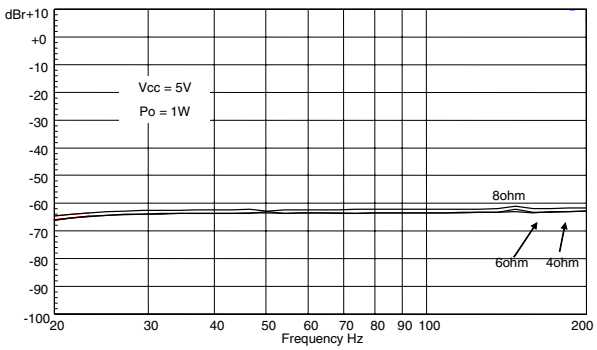


Figure 18. Channel separation stereo DDX mode (R_L = 2 Ω)

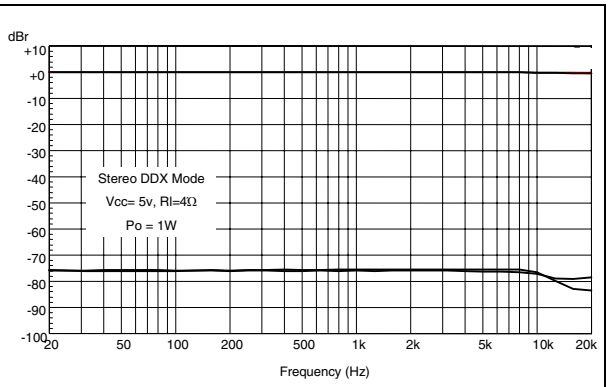


Figure 19. Channel separation stereo S.E. mode (R_L = 2 Ω)

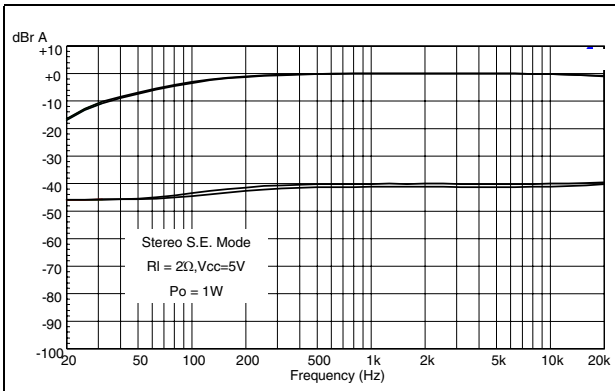


Figure 20. Channel separation stereo S.E. mode (R_L = 4 Ω)

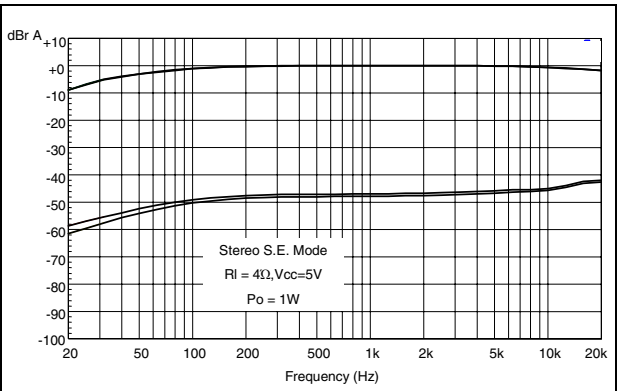


Figure 21. FFT 0 dBFS stereo DDX mode

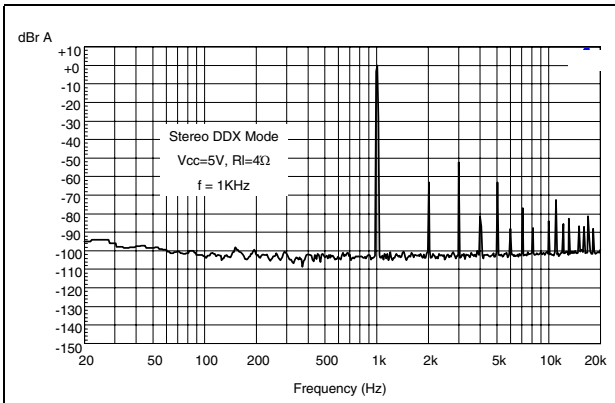


Figure 22. FFT -60 dBFS stereo DDX mode

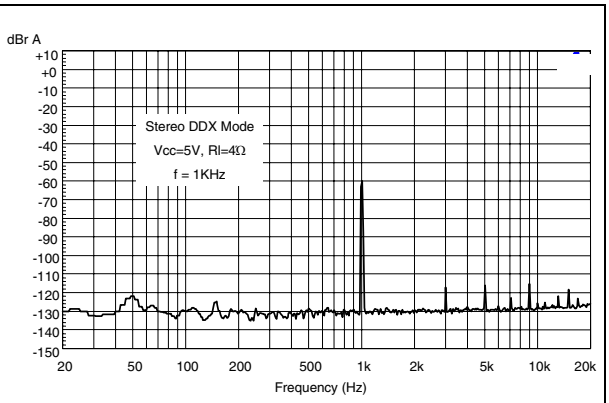


Figure 23. FFT 0 dBFS stereo S.E. mode (R_L = 4 Ω)

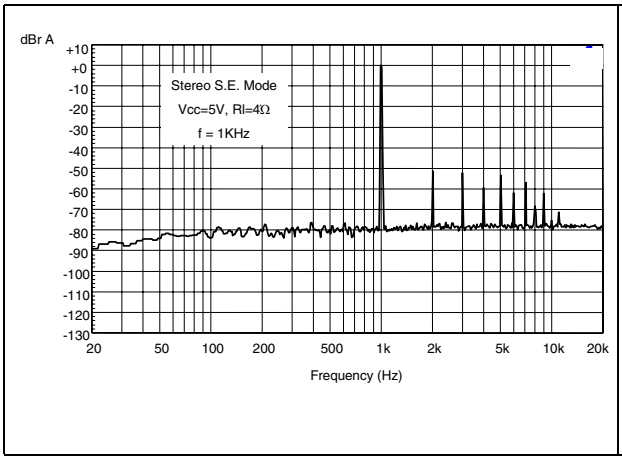


Figure 24. FFT -60 dBFS stereo S.E. mode (R_L = 4 Ω)

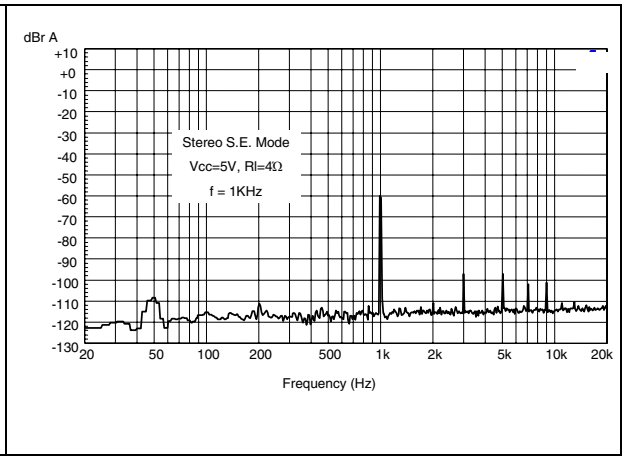


Figure 25. FFT 0 dBFS stereo S.E. mode (R_L = 2 Ω)

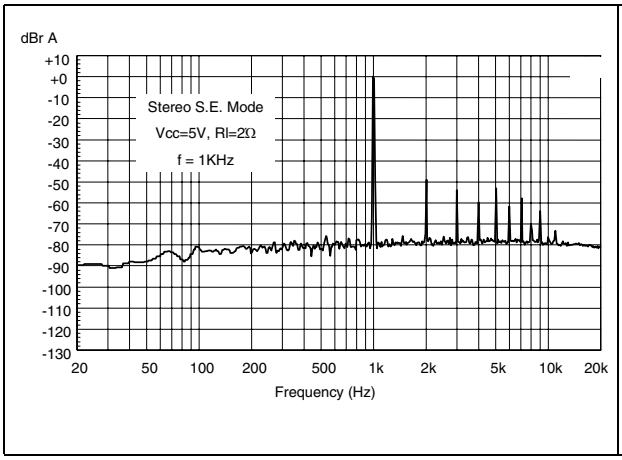
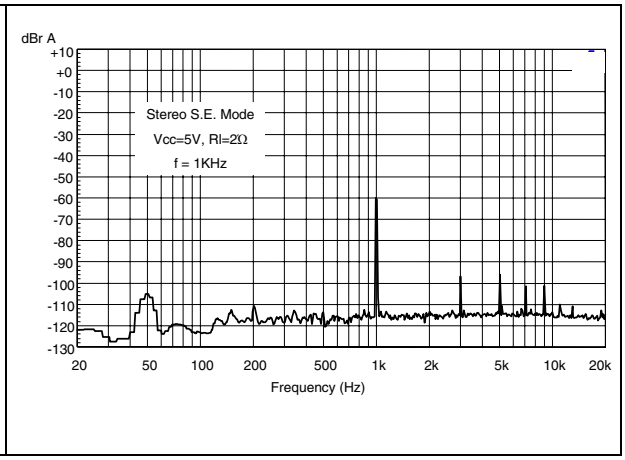


Figure 26. FFT -60 dBFS stereo S.E. mode (R_L = 2 Ω)



4 I²C bus specification

The STA559BWQS supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. STA559BWQS is always a slave device in all of its communications. It supports up to 400 kb/s rate (fast-mode bit rate). STA559BWQS I²C is a slave only interface.

4.1 Communication protocol

4.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

4.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

4.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA559BWQS and the bus master.

4.1.4 Data input

During the data input the STA559BWQS samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

4.2 Device addressing

To start communication between the master and the STA559BWQS, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA559BWQS the I²C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA559BWQS identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

4.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA559BWQS acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the STA559BWQS again responds with an acknowledgement.

4.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA559BWQS. The master then terminates the transfer by generating a STOP condition.

4.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

4.4 Read operation

4.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA559BWQS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes will be read from sequential addresses within the STA559BWQS. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

4.4.3 Random address byte read

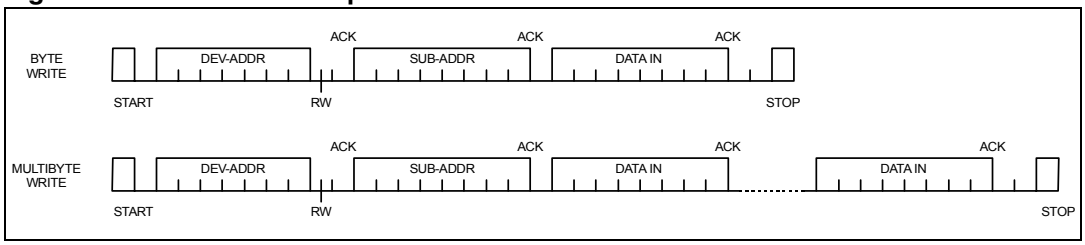
Following the START condition the master sends a device select code with the RW bit set to 0. The STA559BWQS acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA559BWQS again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA559BWQS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes will be read from sequential addresses within the STA559BWQS. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

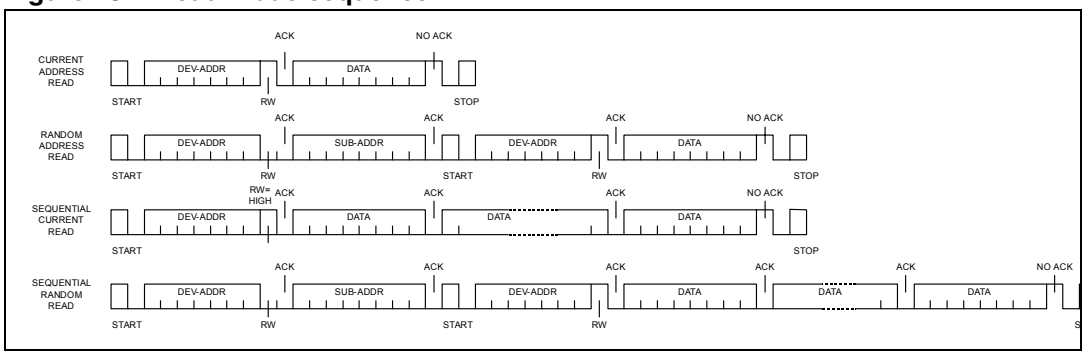
4.4.5 Write mode sequence

Figure 27. Write mode sequence



4.4.6 Read mode sequence

Figure 28. Read mode sequence



5 Register description

Table 9. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	**ConfA**	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	**ConfB**	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	**ConfC**	OCRB		CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	**ConfD**	MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	**ConfE**	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	**ConfF**	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	**Mute/LOC**	LOC1	LOC0			C3M	C2M	C1M	MMute
0x07	**Mvol**	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	**C1Vol**	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	**C2Vol**	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	**C3Vol**	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0B	**Auto1**			AMGC1	AMGC0				
0x0C	**Auto2**	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	**Auto3**								
0x0E	**C1Cfg**	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x0F	**C2Cfg**	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	**C3Cfg**	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
0x11	**Tone**	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	**L1ar**	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	**L1atrt**	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	**L2ar**	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	**L2atrt**	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	**Cfaddr**			CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x17	**B1cf1**	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x18	**B1cf2**	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x19	**B1cf3**	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x1A	**B2cf1**	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x1B	**B2cf2**	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x1C	**B2cf3**	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x1D	**A1cf1**	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x1E	**A1cf2**	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x1F	**A1cf3**	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0

Table 9. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x20	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x21	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x22	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x23	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x24	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x25	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x26	Cfud					RA	R1	WA	W1
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x2A	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	Status	PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN
0x2E	reserved			RO1BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BACT
0x2F	reserved			R01BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND
0x30	reserved				R5BBAD	R4BBAD	R3BBAD	R2BBAD	R1BBAD

5.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

5.1.1 Master clock select

Table 10. Master clock select

Bit	RW	RST	Name	Description
0	RW	1	MCS0	Master clock select: selects the ratio between the input I^2S sample frequency and the input clock.
1	RW	1	MCS1	
2	RW	0	MCS2	

The STA559BWQS will support sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock will be:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48Z kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency, f_s.

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally

Table 11. Input sample rates and clock select

Input sample rate *fs* (kHz)	IR	MCS[2:0]					
		101	100	011	010	001	000
32, 44.1, 48	00	576 fs	128 fs	256 fs	384 fs	512 fs	768 fs
88.2, 96	01	NA	64 fs	128 fs	192 fs	256 fs	384 fs
176.4, 192	1X	NA	32 fs	64fs	96 fs	128 fs	192 fs

5.1.2 Interpolation ratio select

Table 12. Interpolation ratio select

Bit	RW	RST	Name	Description
4..3	RW	00	IR [1:0]	Interpolation ratio select: selects internal interpolation ratio based on input I^2S sample frequency

The STA559BWQS has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 2-times or 1-time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 13. IR bit settings as a function of input sample rate

Input sample rate fs (kHz)	IR	1st stage interpolation ratio
32	00	2 times oversampling
44.1	00	2 times oversampling
48	00	2 times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	2 times downsampling
192	10	2 times downsampling

5.1.3 Thermal warning recovery bypass

Table 14. Thermal warning recovery bypass

Bit	RW	RST	Name	Description
5	RW	1	TWRB	Thermal-warning recovery bypass: 0: Thermal warning recovery enabled 1: Thermal warning recovery disabled

If thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery will determine if the -3 dB output limit is removed when thermal warning is negative.

If TWRB = 0 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit will be removed and the gain will be added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit will remain until TWRB is changed to zero or the device is reset.

5.1.4 Thermal warning adjustment bypass

Table 15. Thermal warning adjustment bypass

Bit	RW	RST	Name	Description
6	RW	1	TWAB	Thermal-warning adjustment bypass: 0: Thermal warning adjustment enabled 1: Thermal warning adjustment disabled

The on-chip STA559BWQS power output block provides feedback to the digital controller using inputs to the power control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period of time greater than 400 ms, the power control block will force a -3 dB output limit (determined by TWOCL in Coeff RAM) to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning output limit adjustment is applied, it remains in this state until reset, unless FDRB = 0.

5.1.5 Fault detect recovery bypass

Table 16. Fault detect recovery bypass

Bit	RW	RST	Name	Description
7	RW	0	FDRB	Fault-detect recovery bypass: 0: Fault detect recovery enabled 1: Fault detect recovery disabled

The on-chip STA559BWQS power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block will attempt a recovery from the fault by asserting the 3-state output (setting it to 0 which directs the power output block to begin recovery), hold it at 0 for period of time in the range of 0.1 ms to 1 s as defined by the fault-detect recovery constant register (FDRC registers 0x29 - 0x2A), then toggle it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

5.2 Configuration register B (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

5.2.1 Serial audio input interface format

Table 17. Serial audio input interface format

Bit	RW	RST	Name	Description
0	RW	0	SAI0	Serial audio input interface format: determines the interface format of the input serial digital audio interface.
1	RW	0	SAI1	
2	RW	0	SAI2	
3	RW	0	SAI3	

5.2.2 Serial data interface

The STA559BWQS audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. STA559BWQS always acts a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 & 2 SDI12.

The SAI register (Configuration Register B - 01h, Bits D3-D0) and the SAIFB register (configuration register B - 01h, Bit D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-First. Available formats are shown in the tables and figure that follow.

5.2.3 Serial data first bit

Table 18. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 19. Support serial audio input formats for MSB-First (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32 fs	0000	0	I^2S 15 bit data
	0001	0	Left/Right-justified 16 bit data

Table 19. Support serial audio input formats for MSB-First (SAIFB = 0) (continued)

BICKI	SAI [3:0]	SAIFB	Interface format
48 fs	0000	0	I^2S 16-23 bit data
	0001	0	Left-Justified 16-24 bit data
	0010	0	Right-Justified 24 bit data
	0110	0	Right-Justified 20 bit data
	1010	0	Right-Justified 18 bit data
	1110	0	Right-Justified 16 bit data
64 fs	0000	0	I^2S 16-24 bit data
	0001	0	Left-Justified 16-24 bit data
	0010	0	Right-Justified 24 bit data
	0110	0	Right-Justified 20 bit data
	1010	0	Right-Justified 18 bit data
	1110	0	Right-Justified 16 bit data

Table 20. Supported serial audio input formats for LSB-First (SAIFB = 1)

BICKI	SAI [3:0]	SAIFB	Interface format
32 fs	1100	1	I^2S 15 bit data
	1110	1	Left/Right-Justified 16 bit data
48 fs	0100	1	I^2S 23 bit data
	0100	1	I^2S 20 bit data
	1000	1	I^2S 18 bit data
	1100	1	LSB First I^2S 16 bit data
	0001	1	Left-Justified 24 bit data
	0101	1	Left-Justified 20 bit data
	1001	1	Left-Justified 18 bit data
	1101	1	Left-Justified 16 bit data
	0010	1	Right-Justified 24 bit data
	0110	1	Right-Justified 20 bit data
	1010	1	Right-Justified 18 bit data
	1110	1	Right-Justified 16 bit data

Table 20. Supported serial audio input formats for LSB-First (SAIFB = 1) (continued)

BICKI	SAI [3:0]	SAIFB	Interface format
64 fs	0000	1	I^2S 24 bit data
	0100	1	I^2S 20 bit data
	1000	1	I^2S 18 bit data
	1100	1	LSB first I^2S 16 bit data
	0001	1	Left-Justified 24 bit data
	0101	1	Left-Justified 20 bit data
	1001	1	Left-Justified 18 bit data
	1101	1	Left-Justified 16 bit data
	0010	1	Right-Justified 24 bit data
	0110	1	Right-Justified 20 bit data
	1010	1	Right-Justified 18 bit data
	1110	1	Right-Justified 16 bit data

5.2.4 Delay serial clock enable

Table 21. Delay serial clock enable

Bit	RW	RST	Name	Description
5	RW	0	DSCKE	Delay serial clock enable: 0: No serial clock delay 1: Serial clock delay by 1 core clock cycle to tolerate anomalies in some I²S master devices

5.2.5 Channel input mapping

Table 22. Channel input mapping

Bit	RW	RST	Name	Description
6	RW	0	C1IM	0: Processing channel 1 receives left I^2S input 1: Processing channel 1 receives right I^2S input
7	RW	1	C2IM	0: Processing channel 2 receives left I^2S input 1: Processing channel 2 receives right I^2S input

Each channel received via I^2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

5.3 Configuration register C (addr 0x02)

D7	D6	D5	D4	D3	D2	D1	D0
OCRB		CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1		0	1	0	1	1	1

5.3.1 DDX power output mode

Table 23. DXX power output mode

Bit	RW	RST	Name	Description
0	RW	1	OM0	DDX power output mode: selects configuration of DDX output.
1	RW	1	OM1	

The DDX power output mode selects how the DDX output timing is configured.

Different power devices use different output modes.

Table 24. Output modes

OM[1,0]	Output stage - Mode
00	Drop compensation
01	Discrete output stage - Tapered compensation
10	Full power mode
11	Variable drop compensation (CSZx bits)

5.3.2 DDX compensating pulse size register

Table 25. DXX compensating pulse size register

Bit	RW	RST	Name	Description
2	RW	1	CSZ0	Contra size register: when OM[1,0] = 11, this register determines the size of the DDX compensating pulse from 0 clock ticks to 15 clock periods.
3	RW	0	CSZ1	
4	RW	1	CSZ2	
5	RW	0	CSZ3	

Table 26. Compensating pulse size

CSZ[3:0]	Compensating pulse size
0000	0ns (0 tick) Compensating pulse size
0001	20ns (1 tick) Clock period compensating pulse size
…	…
1111	300 ns (15 tick) Clock period compensating pulse size

5.3.3 Over-current warning detect adjustment bypass

Table 27. Over-current warning detect adjustment bypass

Bit	RW	RST	Name	Description
7	RW	1	OCRB	Over-current warning adjustment bypass: 0: Over-current warning adjustment enabled 1: Over-current warning adjustment disabled

The OCWARN input is used to indicate an over-current warning condition. When OCWARN is asserted (set to 0), the power control block will force a adjustment to the modulation limit (default -3 dB) in an attempt to eliminate the over-current warning condition. Once the over-current warning volume adjustment is applied, it remains in this state until reset is applied. The level of adjustment can be changed via the TWOCL (Thermal Warning/Over Current Limit) setting which is address 0 x 37 of the user defined coefficient RAM.

5.4 Configuration register D (addr 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0	1	0	0	0	0	0	0

5.4.1 High-pass filter bypass

Table 28. High-pass filter bypass

Bit	RW	RST	Name	Description
0	RW	0	HPB	High-pass filter bypass bit. setting of one bypasses internal AC coupling digital high-pass filter.

The STA559BWQS features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier. DC signals can cause speaker damage. When HPB = 0, this filter is enabled.

5.4.2 De-emphasis

Table 29. De-emphasis

Bit	RW	RST	Name	Description
1	RW	0	DEMP	De-emphasis: 0: No de-emphasis 1: De-emphasis

Setting the DEMP bit enables de-emphasis on all channels

5.4.3 DSP bypass

Table 30. DSP bypass

Bit	RW	RST	Name	Description
2	RW	0	DSPB	DSP bypass bit: 0: Normal operation 1: Bypass of biquad and bass/treble functionality

Setting the DSPB bit bypasses the EQ functionality of the STA559BWQS.

5.4.4 Post-scale link

Table 31. Post-scale link

Bit	RW	RST	Name	Description
3	RW	0	PSL	Post-scale link: 0: Each channel uses individual post-scale value 1: Each channel uses channel 1 post-scale value

Post-scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

5.4.5 Biquad coefficient link

Table 32. Biquad coefficient link

Bit	RW	RST	Name	Description
4	RW	0	BQL	Biquad link: 0: Each channel uses coefficient values 1: Each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the channel 1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

5.4.6 Dynamic range compression/anti-clipping bit

Table 33. Dynamic range compression/anti-clipping bit

Bit	RW	RST	Name	Description
5	RW	0	DRC	Dynamic range compression/anti-clipping 0: Limiters act in anti-clipping mode 1: Limiters act in dynamic range compression mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

5.4.7 Zero-detect mute enable

Table 34. Zero-detect mute enable

Bit	RW	RST	Name	Description
6	RW	1	ZDE	Zero-detect mute enable: setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management) filter. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

5.4.8 MiamiMode enable

Table 35. MiamiMode enable

Bit	RW	RST	Name	Description
7	RW	0	MME	Miami-Mode enable: 0: Sub mix into left/right disabled 1: Sub mix into left/right enabled

5.5 Configuration register E (addr 0x04)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
1	1	0	0	0	0	1	0

5.5.1 Max power correction variable

Table 36. Max power correction variable

Bit	RW	RST	Name	Description
0	RW	0	MPCV	Max power correction variable: 0: Use standard MPC coefficient 1: Use MPCC bits for MPC coefficient

5.5.2 Max power correction

Table 37. Max power correction

Bit	RW	RST	Name	Description
1	RW	1	MPC	Max power correction: setting of 1 enables power bridge correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the STA50x power device at high power. This mode should lower the THD + N of a full DDX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM[1,0] = 01) and binary. When OCFG = 00, MPC will not effect channels 3 and 4, the line-out channels.

5.5.3 Noise-shaper bandwidth selection

Table 38. Noise-shaper bandwidth selection

Bit	RW	RST	Name	Description
2	RW	0	NSBW	Noise-shaper bandwidth selection: 1 - 3rd order NS 0 - 4th order NS

5.5.4 AM mode enable

Table 39. AM mode enable

Bit	RW	RST	Name	Description
3	RW	0	AME	AM mode enable: 0 - Normal DDX operation. 1 - AM reduction mode DDX operation

STA559BWQS features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to ~83 dB in this mode, which is still greater than the SNR of AM radio.

5.5.5 PWM speed mode

Table 40. PWM speed mode

Bit	RW	RST	Name	Description
4	RW	0	PWMS	PWM speed selection: 0 - Normal speed (384 kHz) all channels 1 - Odd speed (341.3k Hz) all channels

5.5.6 Distortion compensation variable enable

Table 41. Distortion compensation variable enable

Bit	RW	RST	Name	Description
5	RW	0	DCCV	Distortion compensation variable enable: 0 - Uses preset DC coefficient. 1 - Uses DCC coefficient.

5.5.7 Zero-crossing volume enable

Table 42. Zero-crossing volume enable

Bit	RW	RST	Name	Description
6	RW	1	ZCE	Zero-crossing volume enable: 1 - Volume adjustments will only occur at digital zero-crossings 0 - Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

5.5.8 Soft volume update enable

Table 43. Soft volume update enable

Bit	RW	RST	Name	Description
7	RW	1	SVE	Soft volume enable: 1: Volume adjustments ramp according to SVR settings 0: Volume adjustments will occur immediately

5.6 Configuration register F (addr 0x05)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0	1	0	1	1	1	0	0

5.6.1 Output configuration

Table 44. Output configuration

Bit	RW	RST	Name	Description
0	RW	0	OCFG0	Selects the output configuration
1	RW	0	OCFG1	

Table 45. Output configuration engine selection

OCFG[1:0]	Output configuration	Config pin
00	2 channel (full-bridge) power, 2 channel data-out: 1A/1B →1A/1B 2A/2B → 2A/2B LineOut1 → 3A/3B LineOut2 → 4A/4B Line out configuration determined by LOC register	0
01	2 (half-bridge). 1 (full-bridge) on-board power: 1A → 1A Binary 0 ° 2A → 1B Binary 90° 3A/3B → 2A/2B Binary 45° 1A/B → 3A/B Binary 0° 2A/B → 4A/B Binary 90°	0
10	2 channel (full-bridge) power, 1 channel DDX: 1A/1B → 1A/1B 2A/2B → 2A/2B 3A/3B → 3A/3B EAPDEXT and TWARNEXT active	0

Note: To the left of the arrow is the processing channel. Note that though the defaults are shown, using channel output mapping, any of the three processing channel outputs can be used for any of the three inputs

Figure 29. OCFG = 00 (default value)

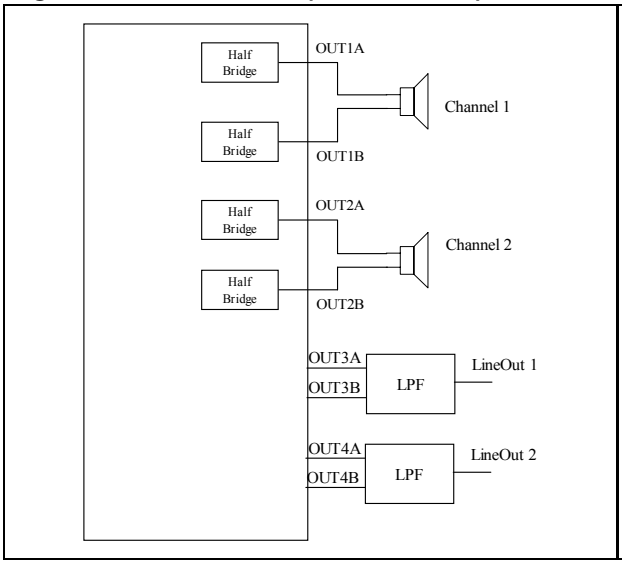


Figure 30. OCFG = 01

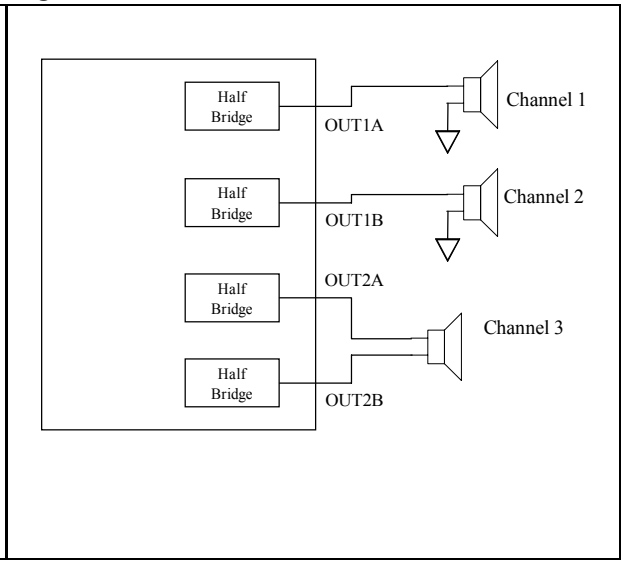
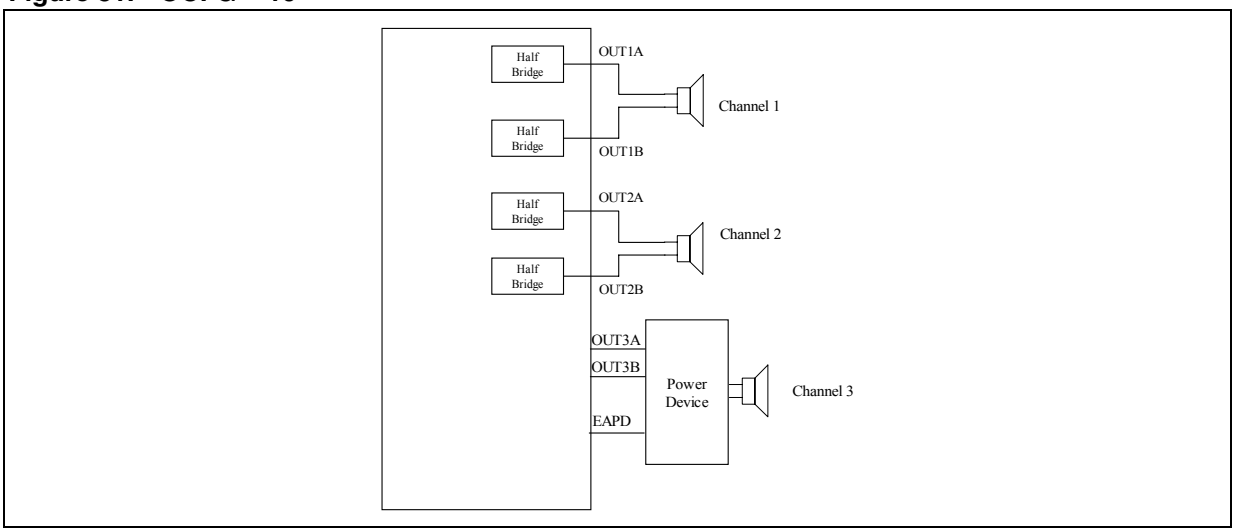


Figure 31. OCFG = 10



5.6.2 Invalid input detect mute enable

Table 46. Invalid input detect mute enable

Bit	RW	RST	Name	Description
2	RW	1	IDE	Invalid input detect mute enable: setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and will automatically mute if the signals are perceived as invalid.

5.6.3 Binary output mode clock loss detection

Table 47. Binary output mode clock loss detection

Bit	RW	RST	Name	Description
3	RW	1	BCLE	Binary output mode clock loss detection enable

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

5.6.4 LRCK double trigger protection

Table 48. LRCK double trigger protection

Bit	RW	RST	Name	Description
4	RW	1	LDTE	LRCLK double trigger protection enable

Actively prevents double trigger of LRCLK.

5.6.5 Auto EAPD on clock loss

Table 49. Auto EAPD on clock loss

Bit	RW	RST	Name	Description
5	RW	0	ECLE	Auto EAPD on clock loss

When active, will issue a power device power down signal (EAPD) on clock loss detection.

5.6.6 IC power down

Table 50. IC power down

Bit	RW	RST	Name	Description
7	RW	1	PWDN	IC power down: 0 - IC powerdown low-power condition 1 - IC normal operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output will begin a soft-mute. After the mute condition is reached, EAPD will be asserted to power down the power-stage, then the master clock to all internal hardware expect the I^2C block will be gated. This places the IC in a very low power consumption state.

5.6.7 External amplifier power down

Table 51. External amplifier power down

Bit	RW	RST	Name	Description
7	RW	0	EAPD	External amplifier power down: 0: External power stage power down active 1: Normal operation

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed on a low-power state (disabled). This register will also control the DDX4B/EAPD output pin when OCFG = 10.

5.7 Volume control registers (addr 0x06 - 0x0A)

5.7.1 Mute/line output configuration register

D7	D6	D5	D4	D3	D2	D1	D0
LOC1	LOC0			C3M	C2M	C1M	MMUTE
0	0			0	0	0	0

Table 52. Line output configuration

LOC[1:0]	Line output configuration
00	Line output fixed - no volume, no EQ
01	Line output variable - CH3 volume effects line output, no EQ
10	Line output variable with EQ - CH3 volume effects line output

Line output is only active when OCFG = 00. In this case LOC will determine the line output configuration. The source of the line output is always the channel 1 and 2 inputs.

5.7.2 Master volume register

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

5.7.3 Channel 1 volume

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

5.7.4 Channel 2 volume

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

5.7.5 Channel 3/line output volume

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

The volume structure of the STA559BWQS consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5dB steps from +48 dB to -80 dB.

As an example if C3V = 00h or +48 dB and MV = 18h or –12 dB, then the total gain for channel 3 = +36 dB.

The master mute when set to 1 will mute all channels at once, whereas the individual channel mutes (CxM) will mute only that channel. Both the master mute and the channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 96 kHz).

A “hard mute” can be obtained by commanding a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than –80 dB will be muted.

All changes in volume take place at zero-crossings when ZCE = 1 (configuration register F) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates will occur immediately.

Table 53. Master volume offset as a function of MV[7:0]

MV[7:0]	Volume offset from channel value
00000000 (0x00)	0 dB
00000001 (0x01)	-0.5 dB
00000010 (0x02)	-1 dB
…	…
01001100 (0x4C)	-38 dB
…	…
11111110 (0xFE)	-127.5 dB
11111111 (0xFF)	Hard master mute

Table 54. Channel volume as a function of CxV[7:0]

CxV[7:0]	Volume
00000000 (0x00)	+48 dB
00000001 (0x01)	+47.5 dB

Table 54. Channel volume as a function of CxV[7:0]

CxV[7:0]	Volume
00000010 (0x02)	+47 dB
…	…
01011111 (0x5F)	+0.5 dB
01100000 (0x60)	0 dB
01100001 (0x61)	-0.5 dB
…	…
11010111 (0xD7)	-59.5 dB
11011000 (0xD8)	-60 dB
11011001 (0xD9)	-61 dB
11011010 (0xDA)	-62 dB
…	…
11101100 (0xEC)	-80 dB
11101101 (0xED)	Hard channel mute
…	…
11111111 (0xFF)	Hard channel mute

5.8 Auto mode registers (addr 0x0B and 0x0C)

5.8.1 AutoMode register 1 (addr 0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
		AMGC1	AMGC2				
		0	0				

Table 55. AutoMode gain compression/limiters selection

AMGC[1:0]	Mode
00	User programmable GC
01	AC no clipping 2.1
10	AC limited clipping (10%) 2.1
11	DRC nighttime listening mode 2.1

5.8.2 AutoMode register 2 (addr 0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

5.8.3 AM interference frequency switching

Table 56. AM interference frequency switching

Bit	RW	RST	Name	Description
0	RW	0	AMAME	AutoMode AM enable 0: Switching frequency determined by PWMS setting 1: Switching frequency determined by AMAM settings

Table 57. AutoMode AM switching frequency selection

AMAM[2:0]	48 kHz/96 kHz Input Fs	44.1 kHz/88.2 kHz Input Fs
000	0.535 MHz - 0.720 MHz	0.535 MHz - 0.670 Mhz
001	0.721 MHz - 0.900 MHz	0.671 MHz - 0.800 MHz
010	0.901 MHz - 1.100 MHz	0.801 MHz - 1.000 MHz
011	1.101 MHz - 1.300 MHz	1.001 MHz - 1.180 MHz
100	1.301 MHz - 1.480 MHz	1.181 MHz - 1.340 MHz
101	1.481 MHz - 1.600 MHz	1.341 MHz - 1.500 MHz
110	1.601 MHz - 1.700 MHz	1.501 MHz - 1.700 MHz

5.8.4 Bass management crossover

Table 58. Bass management crossover

Bit	RW	RST	Name	Description
4	RW	0	XO0	Selects the bass-management crossover frequency. A 1st-order hi-pass filter (channels 1 and 2) or a 2nd-order lo-pass filter (channel 3) at the selected frequency is performed.
5	RW	0	XO1	
6	RW	0	XO2	
7	RW	0	XO3	

Table 59. Bass management crossover frequency

XO[3:0]	Crossover Frequency
0000	User-Defined
0001	80 Hz
0010	100 Hz
0011	120 Hz
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz

Table 59. Bass management crossover frequency

XO[3:0]	Crossover Frequency
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

5.9 Channel configuration registers (addr 0x0E - 0x10)

D7	D6	D5	D4	D3	D2	D1	D0
C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VPB	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VPB	C2EQBP	C2TCB
0	1	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VPB		
1	0	0	0	0	0		

5.9.1 Tone control bypass

Tone control (bass/treble) can be bypassed on a per channel basis for channels 1 and 2.

CxTCB:

0 - Perform tone control on channel X - normal operation

1 - Bypass tone control on channel X

5.9.2 EQ bypass

EQ control can be bypassed on a per channel basis for channels 1 and 2. If EQ control is bypassed on a given channel the prescale and all filters (high-pass, biquads, de-emphasis, bass, treble in any combination) are bypassed for that channel.

CxEQBP:

0 - Perform EQ on channel X - normal operation

1 - Bypass EQ on channel X

5.9.3 Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

5.9.4 Binary output enable registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is negative inverse.

CxBO:

0 - DDX tri-state output - normal operation

1 - Binary output.

5.9.5 Limiter select

Limiter selection can be made on a per-channel basis according to the channel limiter select bits.

Table 60. Channel limiter mapping as a function of CxLS bits

CxLS[1,0]	Channel limiter mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

5.9.6 Output mapping

Output mapping can be performed on a per channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

Table 61. Channel output mapping as a function of CxOM bits

CxOM[1,0]	Channel x output source from
00	Channel 1
01	Channel 2
10	Channel 3

5.10 Tone control register (addr 0x11)

5.10.1 Tone control

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

Table 62. Tone control boost/cut as a function of BTC and TTC bits

BTC[3:0]/TTC[3:0]	Boost/cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	+2 dB
1001	+4 dB
…	…
1101	+12 dB
1110	+12 dB
1111	+12 dB

5.11 Dynamics control registers (addr 0x12 - 0x15)

5.11.1 Limiter 1 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

5.11.2 Limiter 1 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

5.11.3 Limiter 2 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

5.11.4 Limiter 2 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA559BWQS includes 2 independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in configuration register F, bit 0 address 0x05. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers. It is recommended in anti-clipping mode to set this to 0dBFS, which corresponds to the maximum unclipped output power of a DDX amplifier. Since gain can be added digitally within STA559BWQS it is possible to exceed 0dBFS or any other LxAT setting, when this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the release threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the release rate register. The gain can never be increased past it's set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound "lifeless".

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 32. Basic limiter and volume flow diagram.

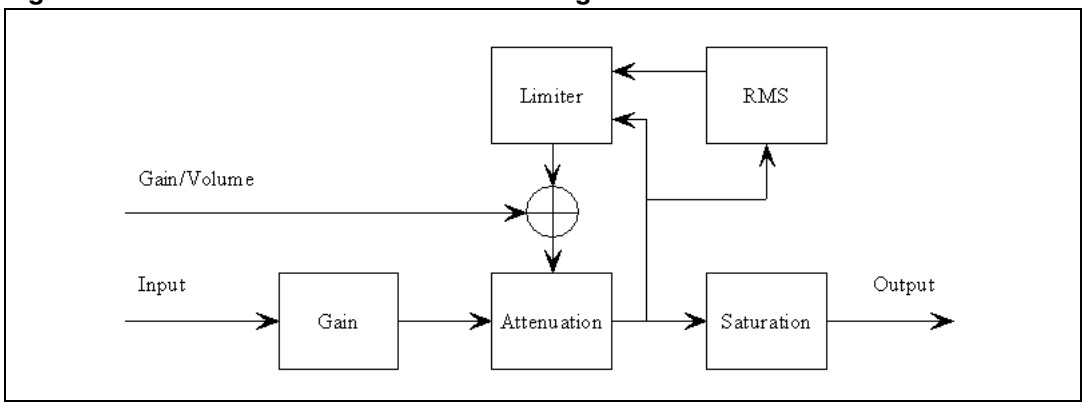


Table 63. Limiter attack rate as a function of LxA bits.

LxA[3:0]	Attack rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	Slow
1111	0.0451	

Table 64. Limiter release rate as a function of LxR bits.

LxR[3:0]	Release rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	Slow
1111	0.0104	

Anti-clipping mode

Table 65. Limiter attack threshold as a function of LxAT bits (AC-Mode)

LxAT[3:0]	AC (dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 66. Limiter release threshold as a function of LxRT bits (AC-Mode)

LxRT[3:0]	AC (dB relative to FS)
0000	-∞
0001	-29 dB
0010	-20 dB
0011	-16 dB
0100	-14 dB
0101	-12 dB
0110	-10 dB
0111	-8 dB
1000	-7 dB
1001	-6 dB
1010	-5 dB
1011	-4 dB
1100	-3 dB
1101	-2 dB
1110	-1 dB
1111	-0 dB

Dynamic range compression mode

Table 67. Limiter attack threshold as a function of LxAT bits (DRC-mode).

LxAT[3:0]	DRC (dB relative to volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 68. Limiter release threshold as a as a function of LxRT bits (DRC-mode).

LxRT [3:0]	DRC (db relative to volume + LxAT)
0000	-∞
0001	-38 dB
0010	-36 dB
0011	-33 dB
0100	-31 dB
0101	-30 dB
0110	-28 dB
0111	-26 dB
1000	-24 dB
1001	-22 dB
1010	-20 dB
1011	-18 dB
1100	-15 dB
1101	-12 dB
1110	-9 dB
1111	-6 dB

5.12 User-defined coefficient control registers (addr 0x16 - 0x26)

5.12.1 Coefficient address register

D7	D6	D5	D4	D3	D2	D1	D0
		CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
		0	0	0	0	0	0

5.12.2 Coefficient b1data register bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

5.12.3 Coefficient b1data register bits 15..8 address

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

5.12.4 Coefficient b1data register bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

5.12.5 Coefficient b2 data register bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

5.12.6 Coefficient b2 data register bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

5.12.7 Coefficient b2 data register bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

5.12.8 Coefficient a1 data register bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

5.12.9 Coefficient a1 data register bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

5.12.10 Coefficient a1 data register bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

5.12.11 Coefficient a2 data register bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

5.12.12 Coefficient a2 data register bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

5.12.13 Coefficient a2 data register bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

5.12.14 Coefficient b0 data register bits 23..16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

5.12.15 Coefficient b0 data register bits 15..8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

5.12.16 Coefficient b0 Data Register Bits 7..0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

5.12.17 Coefficient write/read control register

D7	D6	D5	D4	D3	D2	D1	D0
				RA	R1	WA	W1
				0	0	0	0

Coefficients for user-defined EQ, mixing, scaling, and bass management are handled internally in the STA559BWQS via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I²C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write/read of the coefficient(s) to/from RAM. The following are instructions for reading and writing coefficients.

Reading a coefficient from RAM

- write 6-bits of address to I^2C register 0x16
- write 1 to R1 bit in I^2C address 0x26
- read top 8-bits of coefficient in I^2C address 0x17
- read middle 8-bits of coefficient in I^2C address 0x18
- read bottom 8-bits of coefficient in I^2C address 0x19.

Reading a set of coefficients from RAM

- write 6-bits of address to I^2C register 0x16
- write 1 to RA bit in I^2C address 0x26
- read top 8-bits of coefficient in I^2C address 0x17
- read middle 8-bits of coefficient in I^2C address 0x18
- read bottom 8-bits of coefficient in I^2C address 0x19
- read top 8-bits of coefficient b2 in I^2C address 0x1A
- read middle 8-bits of coefficient b2 in I^2C address 0x1B
- read bottom 8-bits of coefficient b2 in I^2C address 0x1C
- read top 8-bits of coefficient a1 in I^2C address 0x1D
- read middle 8-bits of coefficient a1 in I^2C address 0x1E
- read bottom 8-bits of coefficient a1 in I^2C address 0x1F
- read top 8-bits of coefficient a2 in I^2C address 0x20
- read middle 8-bits of coefficient a2 in I^2C address 0x21
- read bottom 8-bits of coefficient a2 in I^2C address 0x22
- read top 8-bits of coefficient b0 in I^2C address 0x23
- read middle 8-bits of coefficient b0 in I^2C address 0x24
- read bottom 8-bits of coefficient b0 in I^2C address 0x25.

Writing a single coefficient to RAM

- write 6-bits of address to I^2C register 0x16
- write top 8-bits of coefficient in I^2C address 0x17
- write middle 8-bits of coefficient in I^2C address 0x18
- write bottom 8-bits of coefficient in I^2C address 0x19
- write 1 to W1 bit in I^2C address 0x26.

Writing a set of coefficients to RAM

- write 6-bits of starting address to I^2C register 0x16
- write top 8-bits of coefficient b1 in I^2C address 0x17
- write middle 8-bits of coefficient b1 in I^2C address 0x18
- write bottom 8-bits of coefficient b1 in I^2C address 0x19
- write top 8-bits of coefficient b2 in I^2C address 0x1A
- write middle 8-bits of coefficient b2 in I^2C address 0x1B
- write bottom 8-bits of coefficient b2 in I^2C address 0x1C
- write top 8-bits of coefficient a1 in I^2C address 0x1D
- write middle 8-bits of coefficient a1 in I^2C address 0x1E
- write bottom 8-bits of coefficient a1 in I^2C address 0x1F
- write top 8-bits of coefficient a2 in I^2C address 0x20
- write middle 8-bits of coefficient a2 in I^2C address 0x21
- write bottom 8-bits of coefficient a2 in I^2C address 0x22
- write top 8-bits of coefficient b0 in I^2C address 0x23
- write middle 8-bits of coefficient b0 in I^2C address 0x24
- write bottom 8-bits of coefficient b0 in I^2C address 0x25
- write 1 to WA bit in I^2C address 0x26.

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 6-bit address would specify the address of the biquad b1 coefficient (for example, 0, 5, 10, 20, 35 decimal), and the STA559BWQS will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

5.12.18 User-defined EQ

The STA559BWQS provides the ability to specify four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$$Y[n] = 2(b_0/2)X[n] + 2(b_1/2)X[n-1] + b_2X[n-2] - 2(a_1/2)Y[n-1] - a_2Y[n-2]$$
$$= b_0X[n] + b_1X[n-1] + b_2X[n-2] - a_1Y[n-1] - a_2Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999998808).

Coefficients stored in the user defined coefficient RAM are referenced in the following manner:

CxHy0 = $b_1/2$
CxHy1 = b_2
CxHy2 = $-a_1/2$
CxHy3 = $-a_2$
CxHy4 = $b_0/2$

where x represents the channel and the y the biquad number. For example C2H41 is the b_2 coefficient in the fourth biquad for channel 2.

Additionally, the STA559BWQS allows specification of a high-pass filter (processing channels 1 and 2) and a lo-pass filter (processing channel 3) to be used for bass-management crossover when the XO setting is 000 (user-defined). Both of these filters when defined by the user (rather than using the preset crossover filters) are 2^{nd} order filters that use the biquad equation noted above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in the table below.

By default, all user-defined filters are pass-thru where all coefficients are set to 0, except the $b_0/2$ coefficient which is set to 0x400000 (representing 0.5)

5.12.19 Pre-scale

The STA559BWQS provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiply is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass-management. All channels can use the channel 1 pre-scale factor by setting the Biquad link bit. By default, all pre-scale factors are set to 0x7FFFFF.

5.12.20 Post-scale

The STA559BWQS provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This post-scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiply is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass-management. This post-scale factor can be used in conjunction with an ADC equipped micro-controller to perform power-supply error correction. All channels can use the channel 1 post-scale factor by setting the post-scale link bit. By default, all post-scale factors are set to 0x7FFFFF. When Line output is being utilized, channel 3 post-scale will affect both channels 3 and 4.

5.12.21 Over-current post-scale

The STA559BWQS provides a simple mechanism for reacting to over-current detection in the power-block. When the ocwarn input is asserted, the over-current post-scale value is used in place of the normal post-scale value to provide output attenuation on all channels. The default setting provides 3 dB of output attenuation when ocwarn is asserted.
The amount of attenuation to be applied in this situation can be adjusted by modifying the Over-current Post-scale value. As with the normal post-scale, this scaling value is a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. By default, the over-current post-scale factor is set to 0x5A9DF7. Once the over-current attenuation is applied, it remains until the device is reset.

Table 69. RAM block for biquads, mixing, scaling, and bass management

Index (Decimal)	Index (Hex)		Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10(b1/2)	0x000000
1	0x01		C1H11(b2)	0x000000
2	0x02		C1H12(a1/2)	0x000000
3	0x03		C1H13(a2)	0x000000
4	0x04		C1H14(b0/2)	0x400000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
…	…	…	…	…
19	0x13	Channel 1 - Biquad 4	C1H44	0x400000
20	0x14	Channel 2 - Biquad 1	C2H10	0x000000
21	0x15		C2H11	0x000000
…	…	…	…	…
39	0x27	Channel 2 - Biquad 4	C2H44	0x400000
40	0x28	High-pass 2nd order filter for XO = 000	C12H0(b1/2)	0x000000
41	0x29		C12H1(b2)	0x000000
42	0x2A		C12H2(a1/2)	0x000000
43	0x2B		C12H3(a2)	0x000000
44	0x2C		C12H4(b0/2)	0x400000
45	0x2D	Low-pass 2nd order filter for XO = 000	C3H0(b1/2)	0x000000
46	0x2E		C3H1(b2)	0x000000
47	0x2F		C3H2(a1/2)	0x000000
48	0x30		C3H3(a2)	0x000000
49	0x31		C3H4(b0/2)	0x400000
50	0x32	Channel 1 - Pre-scale	C1PreS	0x7FFFFF
51	0x33	Channel 2 - Pre-scale	C2PreS	0x7FFFFF
52	0x34	Channel 1 - Post-scale	C1PstS	0x7FFFFF
53	0x35	Channel 2 - Post-scale	C2PstS	0x7FFFFF
54	0x36	Channel 3 - Post-scale	C3PstS	0x7FFFFF
55	0x37	TWARN/OC– Limit	TWOCL	0x5A9DF7
56	0x38	Channel 1 - Mix 1	C1MX1	0x7FFFFF
57	0x39	Channel 1 - Mix 2	C1MX2	0x000000
58	0x3A	Channel 2 - Mix 1	C2MX1	0x000000
59	0x3B	Channel 2 - Mix 2	C2MX2	0x7FFFFF
60	0x3C	Channel 3 - Mix 1	C3MX1	0x400000
61	0x3D	Channel 3 - Mix 2	C3MX2	0x400000
62	0x3E	UNUSED		
63	0x3F	UNUSED		

5.13 Variable max power correction registers (addr 0x27 - 0x28)

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	0	1	1	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

5.14 Variable distortion compensation registers (addr 0x29-0x2A)

DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

5.15 Fault detect recovery constant registers (addr 0x2B - 0x2C)

FDRC bits specify the 16-bit Fault Detect Recovery time delay. When FAULT is asserted, the TRISTATE output will be immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x000C specifies approximately 0.1 ms.

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

5.16 Device status register (addr 0x2D)

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN

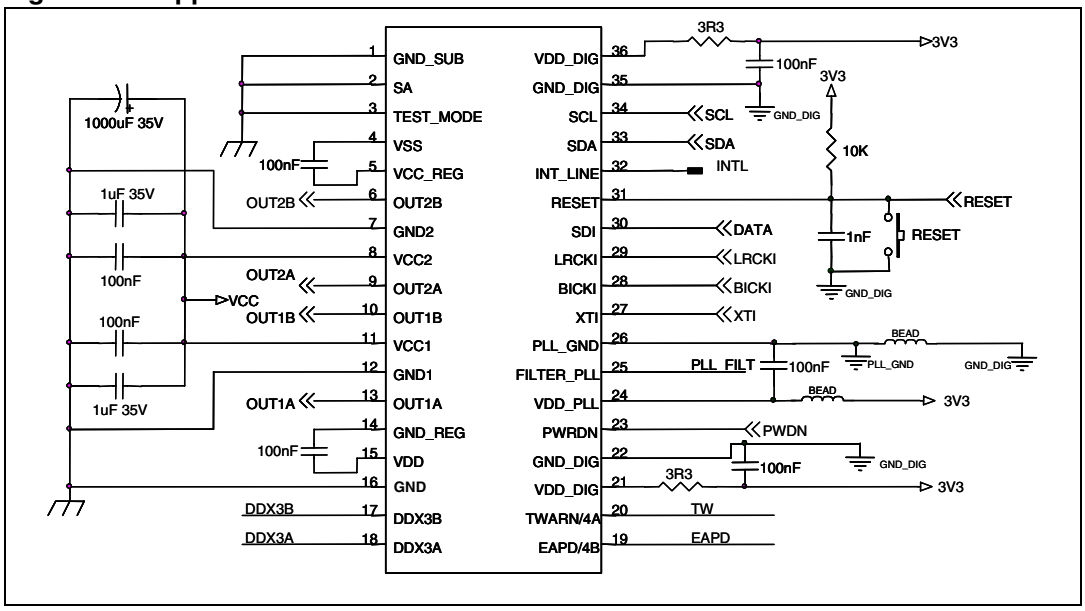
This read-only register provides fault and thermal-warning status information from the power control block.

6 Application

6.1 Application scheme for power supplies

Figure 33 below shows a circuit diagram of a typical application for STA559BWQS.Particular care has to be given to the layout of the PCB, especially the power supplies. The 3.3-Ω resistors on the digital supplies (VDD_DIG) have to be placed as close as possible to the device. This helps to prevent unwanted oscillation on the digital portion of the device due to inductive tracks of the PCB. This same rule also applies to all the decoupling capacitors in order to limit any kind of spikes on the supplies.

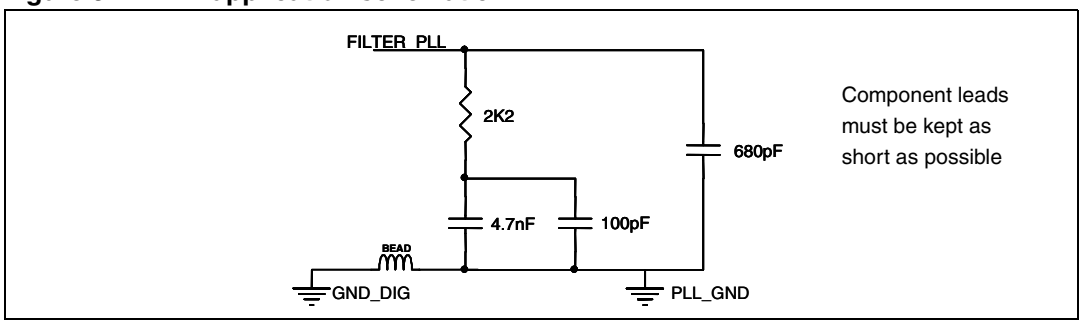
Figure 33. Application schematic



6.2 PLL filter schematic

It is recommended to use the below schematic and values in *Figure 34* below for the PLL loop filter. In order to achieve the best performance from the device in general applications the filter ground (PLL_GND) must be connected as close as possible to the device pin PLL_GND. Concerning the component values, please take into account that the greater is the filter bandwidth, the less is the lock time but the higher is the PLL output jitter.

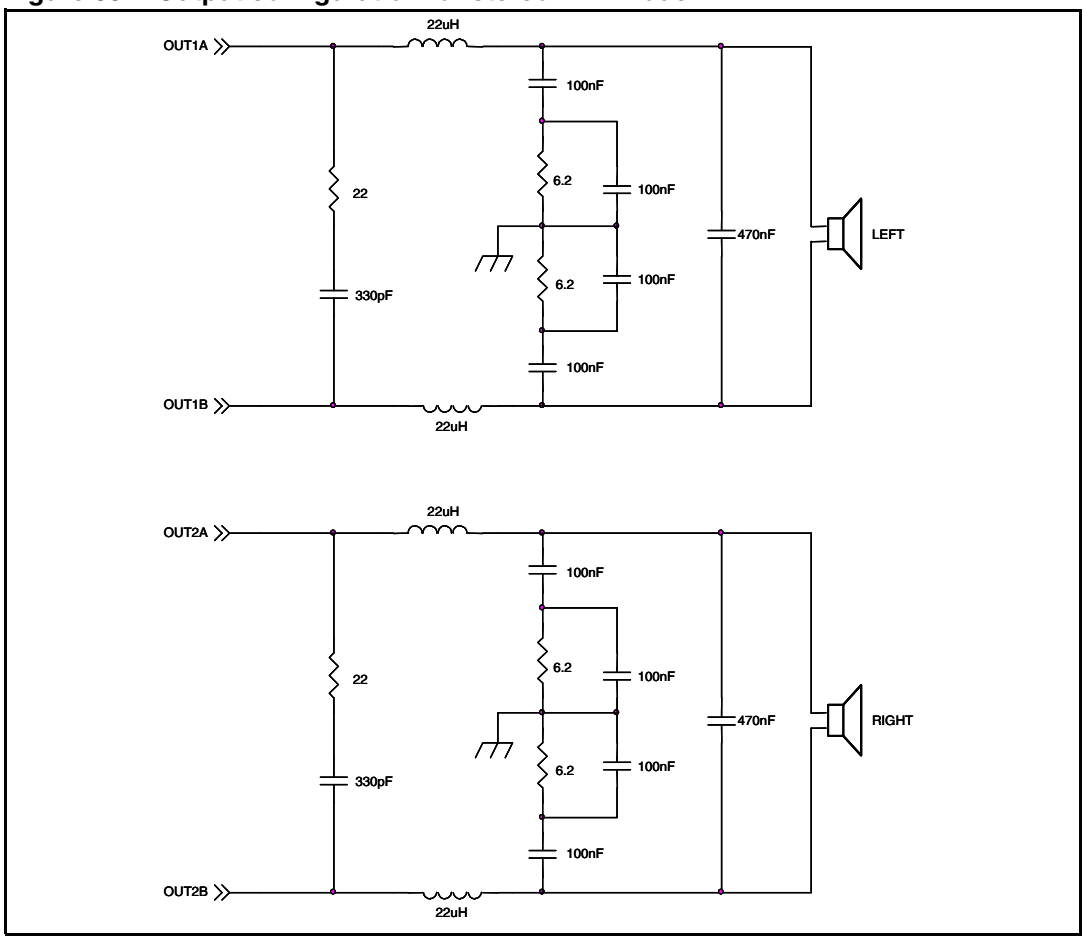
Figure 34. PLL application schematic



6.3 Typical output configuration

Figure 35 shows the typical output configuration used for BTL stereo mode. Please refer to the application note for other recommended output configuration schematics.

Figure 35. Output configuration for stereo BTL mode



7 Package thermal characteristics

Due to the high efficiency of the system the dissipated power is negligible, allowing the use of the STA559BWQS without heat sink but using only a small copper area on the PCB.

Using a double layer PCB the thermal resistance junction to ambient with two copper ground areas of 3 x 3 cm^2 and with 16 via holes (see *Figure 36*) is 24° C/W in natural air convection.

The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level.

The max estimated dissipated power for the STA559BWQS is:

2 x 3 W into 4 Ω at 5 V	Pd max ~ 600mW
2 x 0.7 W + 1 x 3 W into 4 Ω at 5 V	Pd max < 500mW
2 x 1.4 W + 1 x 6 W into 2 Ω at 5 V	Pd max ~ 800mW

This gives, with the suggested board copper area, a max ΔTj of only approximately 20° C for the worst case of the above mentioned applications. The safety margin before the thermal protection intervention (Tj=150°C) is thus ensured, also in severe environments where the ambient temperature exceeds 50° C.

Figure 36. Double layer PCB with copper ground area and with 16 via holes

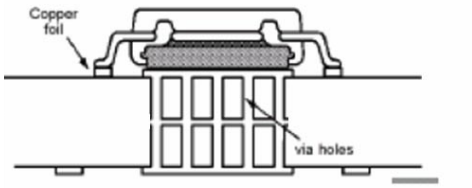
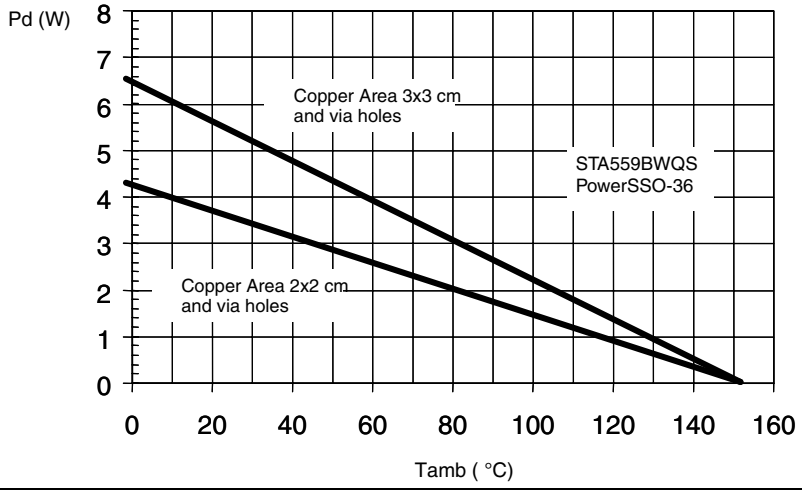


Figure 37 shows the power derating curves for the PowerSSO-36 package on a board with two different sizes of copper layers.

Figure 37. PowerSSO-36 power derating curve



8 Package information

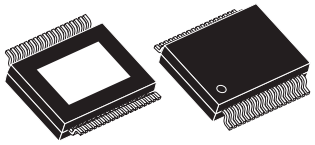
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 38. PowerSSO-36 (slug-up) mechanical data and package dimensions

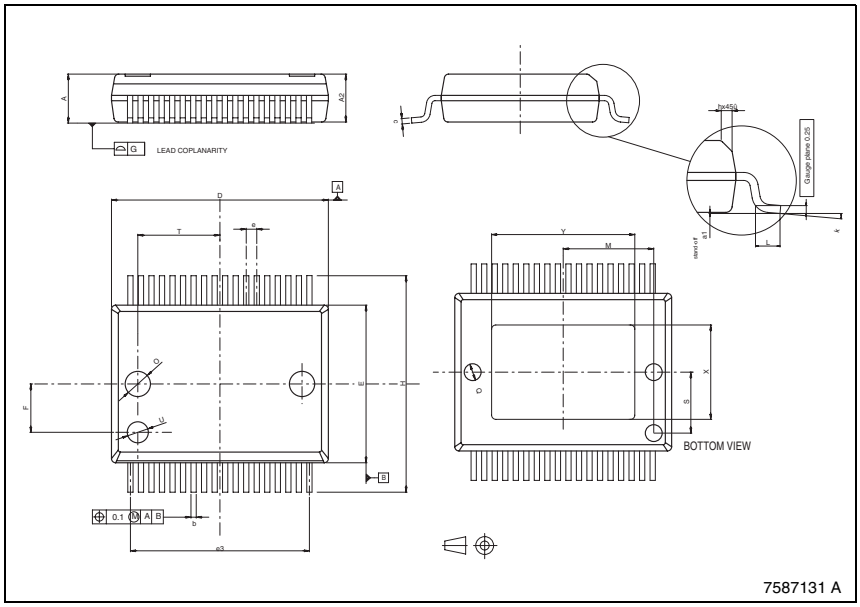
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.5			0.019	
e3		8.5			0.335	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
k		5°			5°	
L	0.55		0.90	0.022		0.035
M		4.3			0.169	
N			10°			10°
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.1		4.7	0.161		0.185
Y	6.5		7.3	0.256		0.287

(1) "D" and "E" do not include mold flash or protrusions Mold flash or protrusions shall not exceed 0.15 mm per side(0.006")

OUTLINE AND MECHANICAL DATA



PowerSSO-36 (slug-down)



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11 Revision history

Table 70. Document revision history

Date	Revision	Changes
28-Mar-2008	1	Initial release.

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