

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe TSOP-6 saves board space.
- Fast switching speed.
- High performance trench technology.

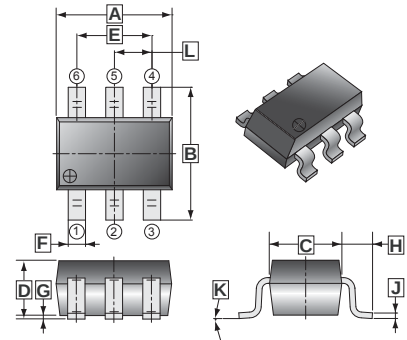
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

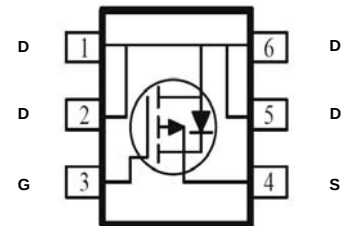
PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7' inch

TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	MAX.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_A = 25^\circ\text{C}$	I_D	2.0	A
	$T_A = 70^\circ\text{C}$		1.6	
Pulsed Drain Current ²		I_{DM}	-8	A
Continuous Source Current (Diode Conduction) ¹		I_S	-2.1	A
Power Dissipation ¹	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating				
Maximum Junction to Ambient ¹	$t \leq 5 \text{ sec}$	$R_{\theta JA}$	62.5	$^\circ\text{C} / \text{W}$
			110	

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS}=0$, $V_{GS} = \pm 20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -80\text{V}$, $V_{GS}=0$
		-	-	-10		$V_{DS} = -80\text{V}$, $V_{GS}=0$, $T_J = 55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-20	-	-	A	$V_{DS} = -5\text{V}$, $V_{GS} = -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	350	m Ω	$V_{GS} = -10\text{V}$, $I_D = -1.4\text{A}$
		-	-	450		$V_{GS} = -4.5\text{V}$, $I_D = -1.2\text{A}$
Forward Transconductance ¹	g_{fs}	-	2.8	-	S	$V_{DS} = -15\text{V}$, $I_D = -1.4\text{A}$
Diode Forward Voltage	V_{SD}	-	-	-1	V	$I_S = -1.4\text{A}$, $V_{GS}=0$
Dynamic ²						
Total Gate Charge	Q_g	-	6	-	nC	$V_{DS} = -30\text{V}$, $V_{GS} = -4.5\text{V}$, $I_D = -1.4\text{A}$
Gate-Source Charge	Q_{gs}	-	10	-		
Gate-Drain Charge	Q_{gd}	-	3	-		
Turn-on Delay Time	$T_{d(on)}$	-	3	-	nS	$V_{DD} = -30\text{V}$, $V_{GEN} = -10\text{V}$, $R_L = 30\Omega$, $I_D = -1\text{A}$, $R_G = 6\Omega$
Rise Time	T_r	-	3	-		
Turn-off Delay Time	$T_{d(off)}$	-	13	-		
Fall Time	T_f	-	7	-		

Notes:

1. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.