Die on Carrier, Silicon Digital Attenuator, 2 dB LSB, 4-Bit, 10 MHz to 60 GHz

FEATURES

- Ultrawideband frequency range: 10 MHz to 60 GHz
- Attenuation range: 22 dB with 2 dB steps
- Bond pads for wire bond and ribbon bond
- Low insertion loss
  - 1.3 dB typical up to 20 GHz
  - 2.0 dB typical up to 44 GHz
  - 2.7 dB typical up to 55 GHz
- Attenuation accuracy
  - ±(0.3 + 1.0% of attenuation state) typical up to 20 GHz
  - ±(0.4 + 4.0% of attenuation state) typical up to 44 GHz
  - ±(0.4 + 6.0% of attenuation state) typical up to 55 GHz
- Typical step error
  - ±0.30 dB typical up to 20 GHz
  - ±0.65 dB typical up to 44 GHz
  - ±1.10 dB typical up to 55 GHz
- High input linearity
  - P0.1dB: 25.5 dBm typical
  - IP3: 45 dBm typical
- High RF power handling
  - 23 dBm steady state and hot switching, average
  - 24 dBm steady state and hot switching, peak
- Tight distribution in relative phase
- No low frequency spurious signals
- Parallel mode control, CMOS/LVTTL compatible
- RF amplitude settling time (0.1 dB of final RF output): 175 ns
- 16-pad, 2.770 mm × 1.620 mm, die on carrier [CHIP]

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeterwave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

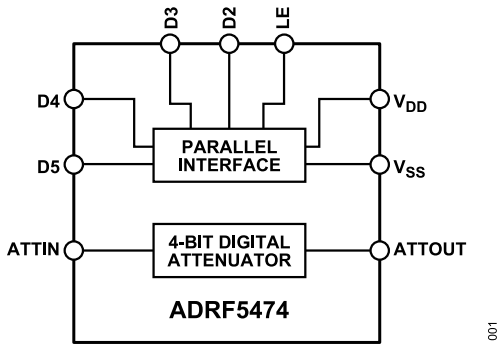

Figure 1.

GENERAL DESCRIPTION

The ADRF5474 is a 4-bit digital attenuator with 22 dB attenuation control range in 2 dB steps manufactured in a silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly, and the bottom of the device is metalized and connected to ground.

This device operates from 10 MHz to 60 GHz with better than 2.7 dB of insertion loss and excellent attenuation accuracy at 55 GHz. The ADRF5474 has a RF input power handling capability of 23 dBm average and 24 dBm peak for all states.

The ADRF5474 requires a dual-supply voltage of +3.3 V and −3.3 V. The device features parallel mode control, and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5474 is designed to match a characteristic impedance of 50 Ω.

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REVISION HISTORY

5/2022—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, die temperature (T_{DIE}) = 25°C, and 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembeded. See the Applications Information section for assembly details.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		10		60,000	MHz
INSERTION LOSS	10 MHz to 20 GHz		1.3		dB
	20 GHz to 44 GHz		2.0		dB
	44 GHz to 55 GHz		2.7		dB
	55 GHz to 60 GHz		4.0		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	10 MHz to 20 GHz		13		dB
	20 GHz to 44 GHz		11		dB
	44 GHz to 55 GHz		9		dB
	55 GHz to 60 GHz		6		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		22		dB
Step Size	Between any successive attenuation states		2		dB
Accuracy	Referenced to insertion loss				
	10 MHz to 20 GHz		±(0.3 + 1.0% of state)		dB
	20 GHz to 44 GHz		±(0.4 + 4.0% of state)		dB
	44 GHz to 55 GHz		±(0.4 + 6.0% of state)		dB
	55 GHz to 60 GHz		±(0.4 + 12.0% of state)		dB
Step Error	Between any successive state				
	10 MHz to 20 GHz		±0.30		dB
	20 GHz to 44 GHz		±0.65		dB
	44 GHz to 55 GHz		±1.10		dB
	55 GHz to 60 GHz		±1.30		dB
RELATIVE PHASE	Referenced to insertion loss				
	10 MHz to 20 GHz		25		Degrees
	20 GHz to 44 GHz		60		Degrees
	44 GHz to 55 GHz		75		Degrees
	55 GHz to 60 GHz		85		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power (P_{IN}) = 10 dBm				
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		50		ns
On and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF output		100		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF output		175		ns
0.05 dB	50% triggered control to 0.05 dB of final RF output		225		ns
Overshoot			2		dB
Undershoot			0.75		dB
RF Phase Settling Time	Frequency = 40 GHz				
5°	50% triggered control to 5° of final RF output		105		ns
1°	50% triggered control to 1° of final RF output		120		ns
INPUT LINEARITY[1]	100 MHz to 50 GHz				
0.1 dB Power Compression (P0.1dB)			25.5		dbm

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Third-Order Intercept (IP3)	Two-tone P_{IN} = 12 dBm per tone, Δf = 1 MHz, all attenuation states		45		dBm
DIGITAL CONTROL INPUTS	LE, D2, D3, D4, and D5				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			−10		μA
High (I_{INH})			<1		μA
SUPPLY CURRENT					
Positive Supply Current					
Bias Low	LE, D2, D3, D4, and D5 = 0 V		52		μA
Bias High	LE, D2, D3, D4, and D5 = 3.3 V		2		μA
Negative Supply Current			−110		μA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
Positive (V_{DD})		3.15		3.45	V
Negative (V_{SS})		−3.45		−3.15	V
Digital Control Voltage		0		V_{DD}	V
RF Power Handling [2]	Frequency = 100 MHz to 50 GHz, T_{DIE}[3] = 85°C,[4] all attenuation states				
Input at ATTIN	Steady state, average			23	dBm
	Steady state, peak			24	dBm
	Hot switching, average			23	dBm
	Hot switching, peak			24	dBm
Input at ATTOUT	Steady state, average			15	dBm
	Steady state, peak			16	dBm
	Hot switching, average			15	dBm
	Hot switching, peak			16	dBm
T_{DIE}[3]		−40		+105	°C

[1] Input linearity performance degrades over frequency, see Figure 19 and Figure 22.

[2] For power derating over frequency, see Figure 2 to Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[3] T_{DIE} refers to the bottom of the die on carrier.

[4] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

TIMING SPECIFICATIONS

See Figure 24 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width, see Figure 24		10		ns
t_{PH}	Hold time, see Figure 24		10		ns
t_{PS}	Setup time, see Figure 24		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Inputs	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Power[1] (Frequency = 100 MHz to 50 GHz, T_{DIE} = 85°C[2])	
Input at ATTIN	
Steady State, Average	24 dBm
Steady State, Peak	25 dBm
Hot Switching, Average	24 dBm
Hot Switching, Peak	25 dBm
Input at ATTOUT	
Steady State, Average	16 dBm
Steady State, Peak	17 dBm
Hot Switching, Average	16 dBm
Hot Switching, Peak	17 dBm
RF Power Under Unbiased Condition (V_{DD} and V_{SS} = 0 V)	
Input at ATTIN	17 dBm
Input at ATTOUT	9 dBm
Temperature	
Junction (T_J)	135°C
Storage	−55°C to +150°C
Processing	170°C
Continuous Power Dissipation (P_{DISS})	0.20 W

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[2] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
C-16-5	250	°C/W

POWER DERATING CURVES

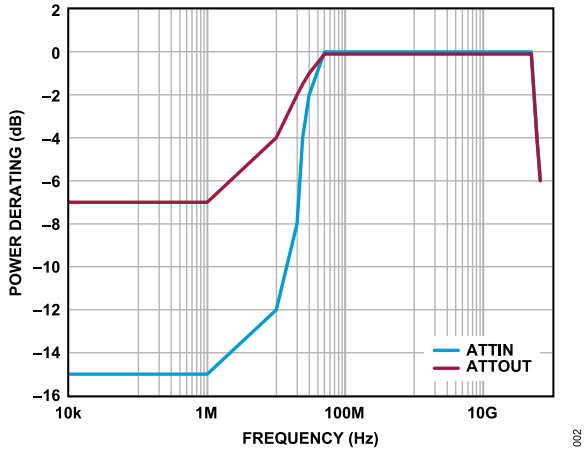

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{DIE} = 85°C

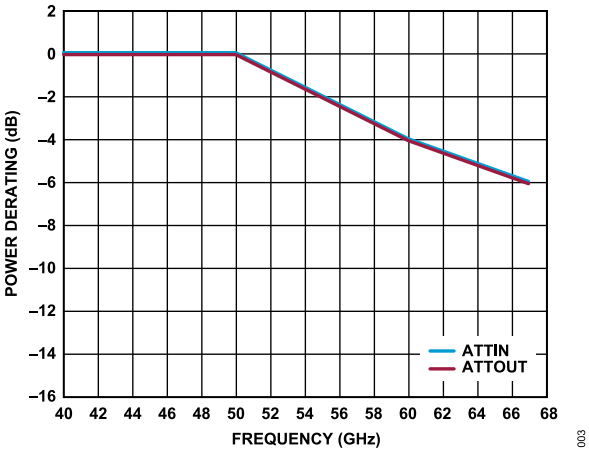

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{DIE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ABSOLUTE MAXIMUM RATINGS

ESD Ratings for ADRF5474

Table 5. ADRF5474, 16-Pad Die on Carrier [CHIP]

ESD Model	Withstand Threshold (V)
Human Body Model (HBM)	±250 ±250 for ATTIN and ATTOUT Pads ±2000 for Supply and Control Pads

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

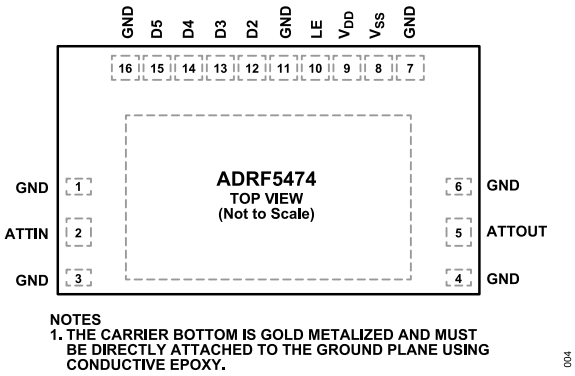

Figure 4. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 7, 11, 16	GND	Ground. Bonding of these ground pads are optional. See the Applications Information section.
2	ATTIN	Attenuator Input. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
5	ATTOUT	Attenuator Output. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
8	V_{SS}	Negative Supply Input. See Figure 8 for the interface schematic.
9	V_{DD}	Positive Supply Input. See Figure 7 for the interface schematic.
10	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
12	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
13	D3	Parallel Control Input for 4 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
14	D4	Parallel Control Input for 8 dB Attenuator Bit.See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
15	D5	Parallel Control Input for 8 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
	Carrier Bottom	The carrier bottom is gold metalized and must be directly attached to the ground plane using conductive epoxy.

INTERFACE SCHEMATICS

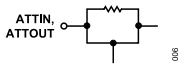

Figure 5. ATTIN and ATTOUT Interface Schematic

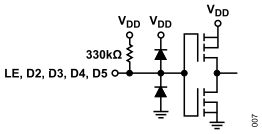

Figure 6. Digital Input Interface Schematic (LE, D2, D3, D4, and D5)

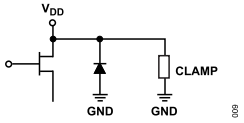

Figure 7. V_{DD} Input Interface Schematic

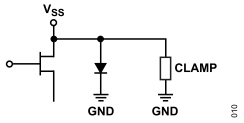

Figure 8. V_{SS} Input Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using GSG probes. The launchers are deembedded. See the Applications Information section for assembly details.

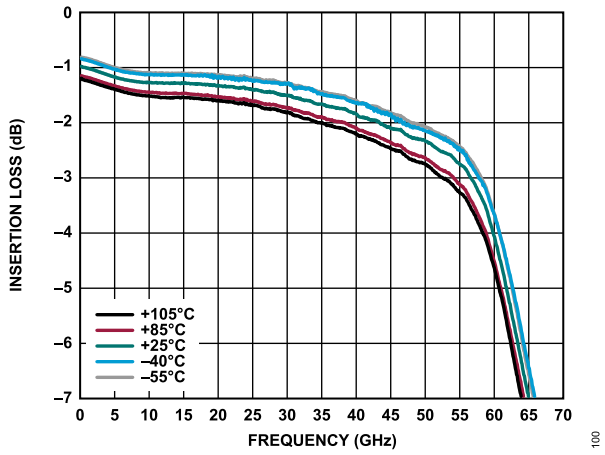

Figure 9. Insertion Loss vs. Frequency over Temperature

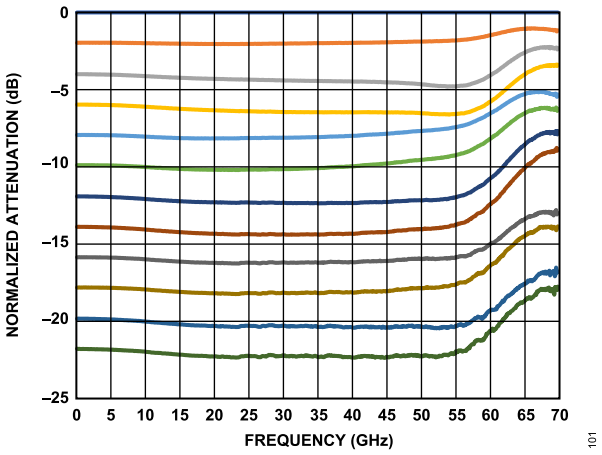

Figure 11. Normalized Attenuation vs. Frequency for All States

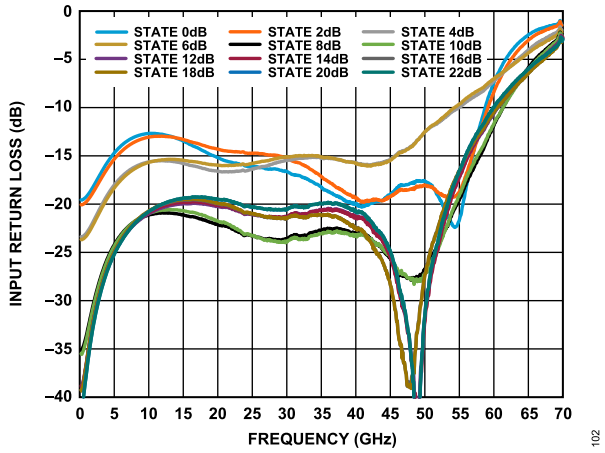

Figure 10. Input Return Loss vs. Frequency

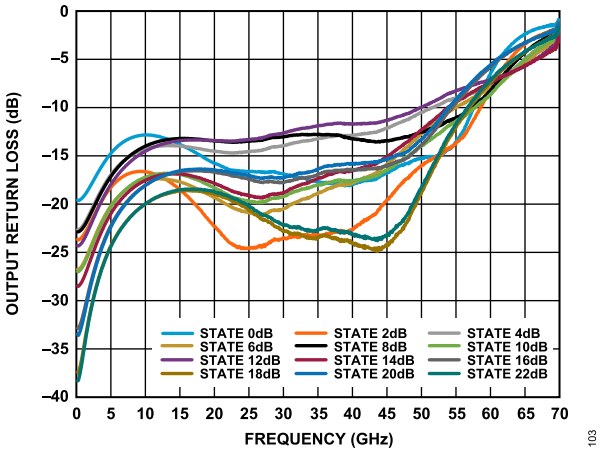

Figure 12. Output Return Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

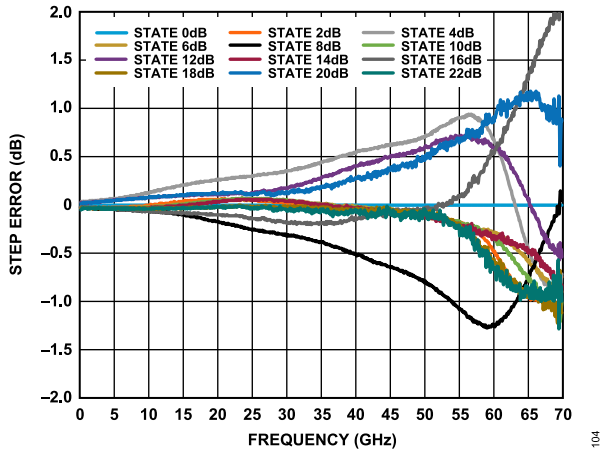

Figure 13. Step Error vs. Frequency

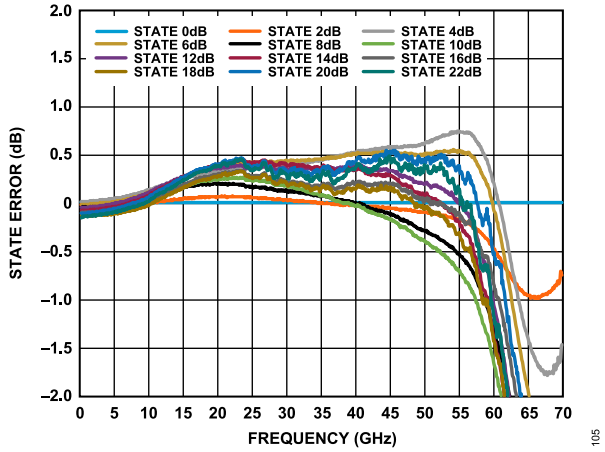

Figure 14. State Error vs. Frequency

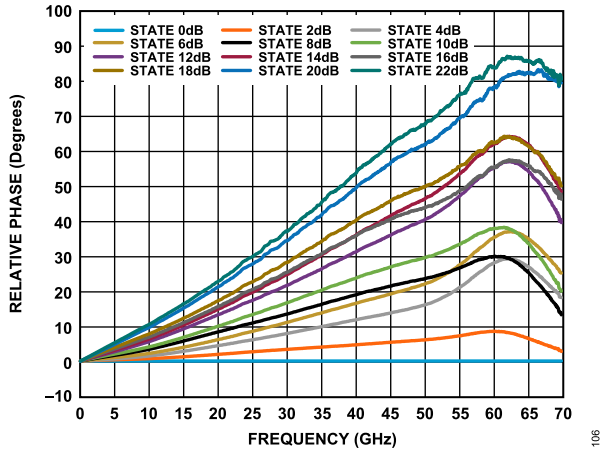

Figure 15. Relative Phase vs. Frequency

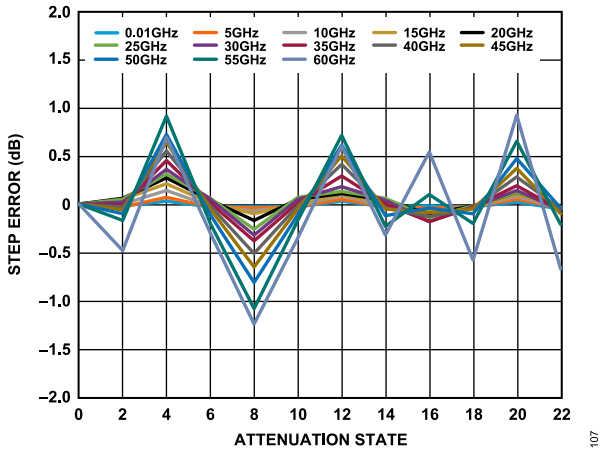

Figure 16. Step Error vs. Attenuation State over Frequency

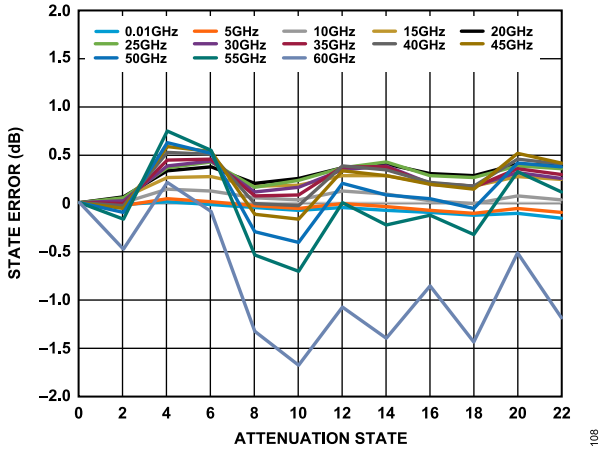

Figure 17. State Error vs. Attenuation State over Frequency

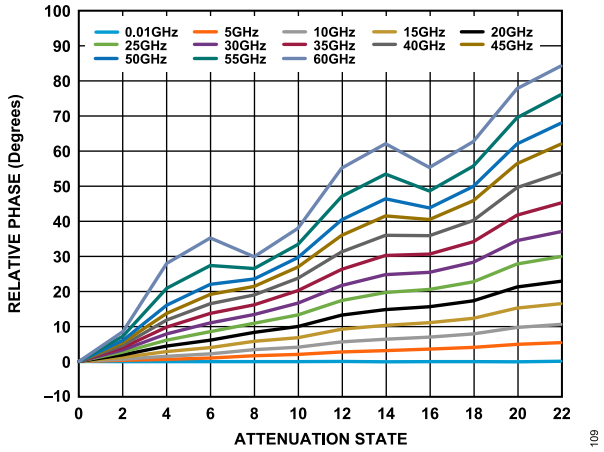

Figure 18. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

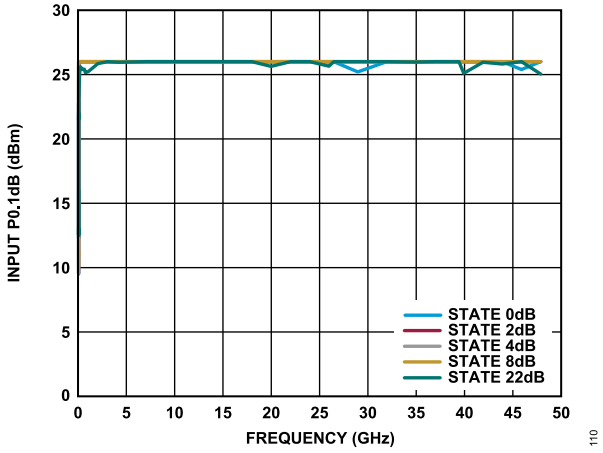

Figure 19. Input P0.1dB vs. Frequency

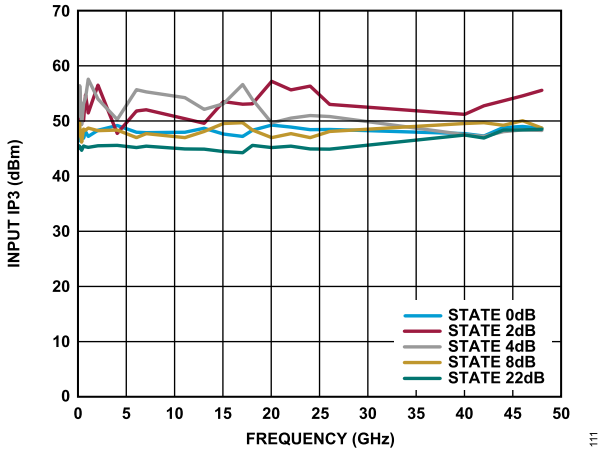

Figure 20. Input IP3 vs. Frequency

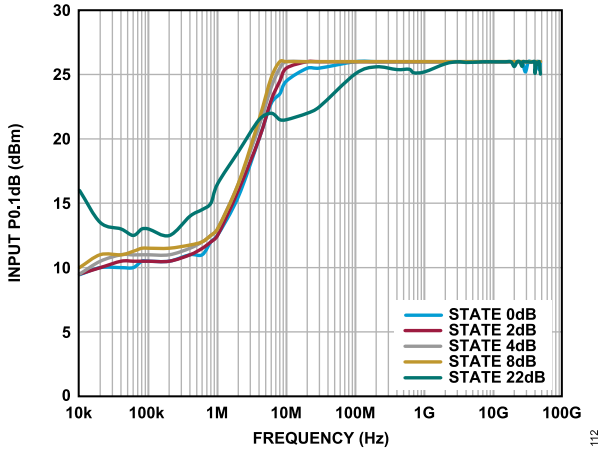

Figure 21. Input P0.1dB vs. Frequency, Low Frequency Detail

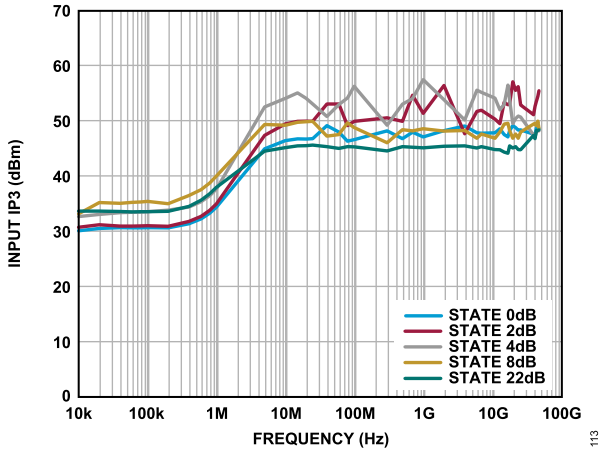

Figure 22. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5474 incorporates a 4-bit fixed attenuator array that offers an attenuation range of 22 dB in 2 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5474 has four digital control inputs, D2 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Figure 23. Internally, there are two 8 dB stages, and these stages can be controlled by the D4 and D5 pins.

POWER SUPPLY

The ADRF5474 requires a positive supply voltage applied to the V_{DD} pad and a negative supply voltage applied to the V_{SS} pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5474 has an internal pull-up resistor (see Figure 6). The internal pull-up resistor sets the attenuator to the maximum attenuation state (22 dB) when the V_{DD} and V_{SS} voltages are applied.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. No dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The ADRF5474 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

Table 7. Truth Table

Digital Control Input[1]				
D5[2]	D4[2]	D3	D2	Attenuation State (dB)
Low	Low	Low	Low	0 (reference)
Low	Low	Low	High	2.0
Low	Low	High	Low	4.0
Low	Low	High	High	6.0
Low	High	Low	Low	8.0
Low	High	Low	High	10.0
Low	High	High	Low	12.0
Low	High	High	High	14.0
High	High	Low	Low	16.0
High	High	Low	High	18.0
High	High	High	Low	20.0
High	High	High	High	22.0

[1] Any combination of the control voltage input states shown in this table provides an attenuation equal to the sum of the bits selected.

[2] D4 and D5 both correspond to the 8 dB state. D4 has slightly better state accuracy at higher frequencies.

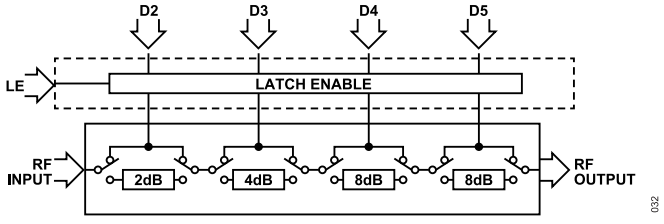

Figure 23. Simplified Circuit Diagram

THEORY OF OPERATION

PARALLEL MODE INTERFACE

The ADRF5474 has four digital control inputs, D2 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 7.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pad high. To change the attenuation state, use the control voltage inputs (D2 to D5) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pad must be kept low when changing the control voltage inputs (D2 to D5) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 4-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 24 and Table 2 for additional information).

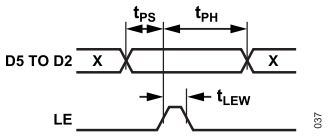

Figure 24. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5474 is shown in Figure 25.

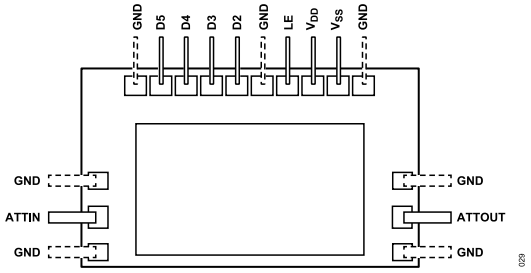

Figure 25. Die Assembly Diagram

The ADRF5474 is designed to have the optimum RF input and output impedance match with 3 mil × 0.5 mil gold ribbon wire and 3 mil loop height typical. The bonding diagrams are shown in Figure 26 and Figure 27. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally to the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The dc pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The device is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

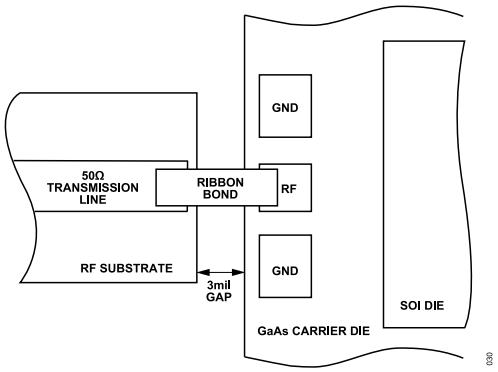

Figure 26. Bonding Diagram Top View

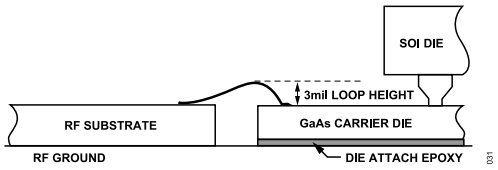

Figure 27. Bonding Diagram Side View

HANDLING, MOUNTING AND EPOXY DIE ATTACH

Keep devices in ESD protective sealed bags for shipment, and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in clean environment.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Because both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS

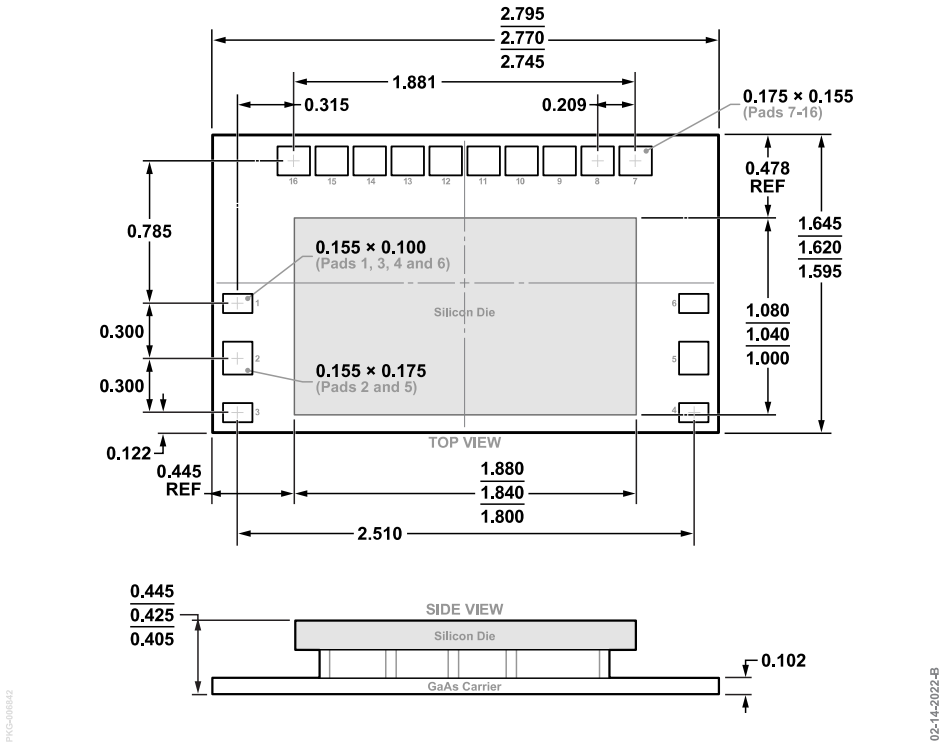

Figure 28. 16-Pad Die on Carrier [CHIP]
(C-16-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Information	Package Option
ADRF5474BCZ	–40°C to +105°C	16-Pad Die on Carrier [CHIP]	Waffle Pack, 50	C-16-5
ADRF5474BCZ-GP	–40°C to +105°C	16-Pad Die on Carrier [CHIP]	Gel Pack, 50	C-16-5
ADRF5474BCZ-SX	–40°C to +105°C	16-Pad Die on Carrier [CHIP]	Waffle Pack, 2	C-16-5

[1] Z = RoHS Compliant Part.