



TPS22962 5.5V, 10A, 4.4mΩ 导通电阻负载开关

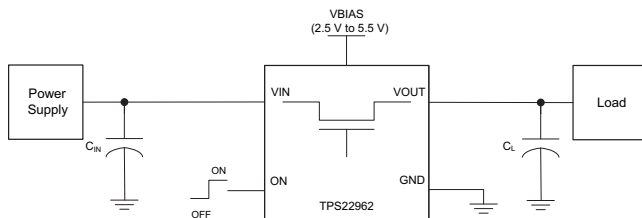
1 特性

- 集成单通道负载开关
- V_{BIAS} 电压范围: 2.5V 至 5.5V
- V_{IN} 电压范围: 0.8V 至 5.5V
- 超低 R_{ON} 电阻
 - $V_{IN} = 5V$ ($V_{BIAS} = 5V$) 时, $R_{ON} = 4.4m\Omega$
- 10A 最大持续开关电流
- 低静态电流 ($V_{BIAS} = 5V$ 时为 $20\mu A$)
- 低关断电流 ($V_{BIAS} = 5V$ 时为 $1\mu A$)
- 低控制输入阈值允许使用 1.2V 或更高电压的通用输入输出 (GPIO) 接口
- V_{BIAS} 和 V_{IN} 范围内的受控和固定转换率
 - $V_{IN} = 5V$ ($V_{BIAS} = 5V$) 时, $t_R = 2663\mu s$
- 快速输出放电 (QOD)
- 带有散热焊盘的小外形尺寸无引线 (SON) 8 端子封装
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
 - 2kV 人体模式 (HBM)
 - 1kV 充电器件模型 (CDM)

2 应用范围

- 服务器
- 医疗
- 电信系统
- 计算
- 工业系统
- 高电流电压轨

4 简化电路原理图



3 说明

TPS22962 是一款小型, 超低 R_{ON} , 单通道负载开关, 此开关具有受控接通功能。此器件包含一个可在 0.8V 至 5.5V 输入电压范围内运行的 N 通道金属氧化物半导体场效应晶体管 (MOSFET), 并且支持最大 10A 的持续电流。

器件的超低 R_{ON} 和高电流处理能力的组合使得此器件非常适合于驱动具有非常严格压降耐受的处理电源轨。器件的受控上升时间大大减少了由大容量负载电容导致的涌入电流, 从而减少或消除了电源损耗。此开关可由 ON 端子单独控制, 此端子能够与微控制器或低压离散逻辑电路生成的低压控制信号直接对接。通过集成一个在开关关闭时实现快速输出放电 (QOD) 的 224Ω 下拉电阻器, 此器件进一步减少总体解决方案尺寸。

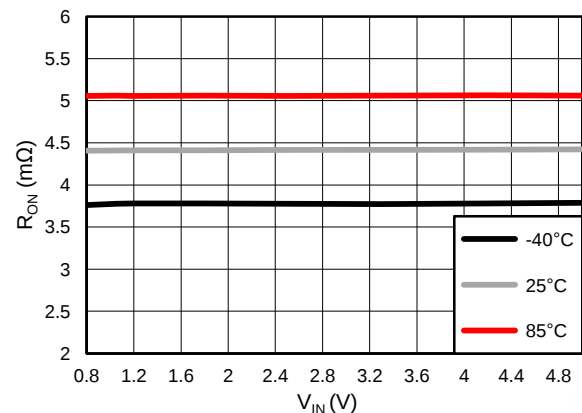
TPS22962 采用小型 3mm x 3mm 超薄小外形尺寸无引线 (WSO8)-8 封装 (DNY)。DNY 封装集成有一个散热焊盘, 此散热焊盘可在高电流和高温应用中实现高功率耗散。器件在自然通风环境下的额定运行温度范围为 $-40^{\circ}C$ 至 $85^{\circ}C$ 。

器件信息⁽¹⁾

产品型号	封装	封装尺寸 (标称值)
TPS22962	WSO8 (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

R_{ON} 与 V_{IN} 之间的关系 ($V_{BIAS} = 5V$, $I_{OUT} = -200mA$)



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5 修订历史记录

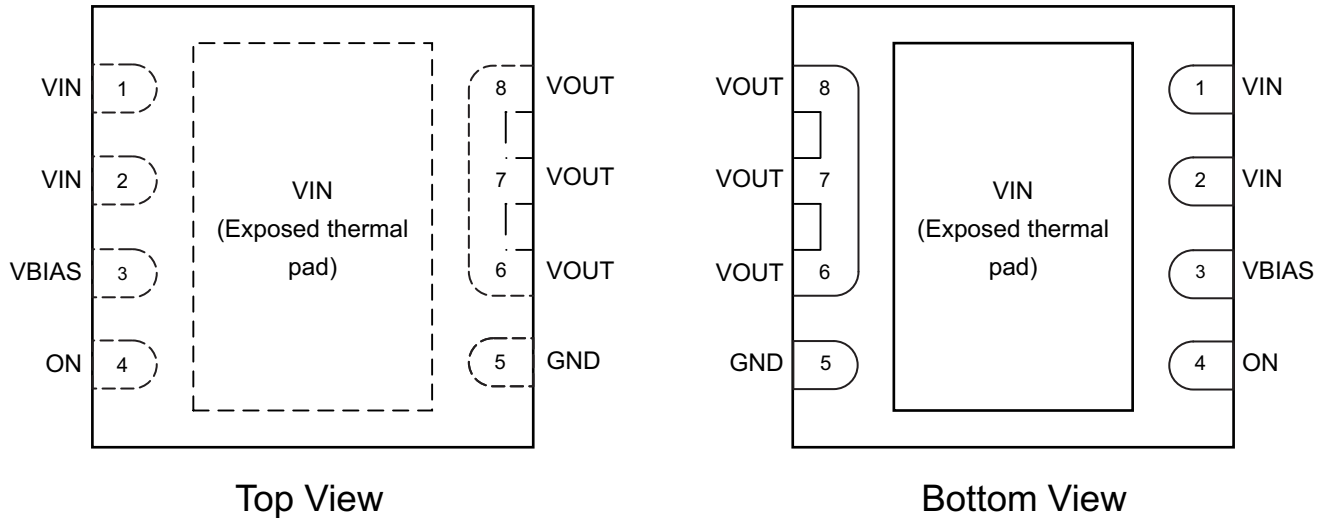
Changes from Original (June 2014) to Revision A

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• 完整版的最初发布版本。	1
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6 Pin Configuration and Functions

**WSO (DNY) PACKAGE
8 PIN**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	–0.3	6	V
V _{BIAS}	Bias voltage range	–0.3	6	V
V _{OUT}	Output voltage range	–0.3	6	V
V _{ON}	ON pin voltage range	–0.3	6	V
I _{MAX}	Maximum Continuous Switch Current, T _A = 70°C		10	A
I _{PLS}	Maximum Pulsed Switch Current, pulse < 300 μs, 2% duty cycle		12	A
T _J	Maximum junction temperature		125	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		–65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage range		0.8	V _{BIAS}	V
V _{BIAS}	Bias voltage range		2.5	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range			V _{IN}	V
V _{IH, ON}	High-level voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V _{IL, ON}	Low-level voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	0	0.5	V
T _A	Operating free-air temperature range		–40	85	°C
C _{IN}	Input Capacitor		1 ⁽¹⁾		μF

(1) Refer to [Detailed Description](#) section.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22962	UNIT
		DNY 8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	44.6	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	44.4	
R _{θJB}	Junction-to-board thermal resistance	17.6	
ψ _{JT}	Junction-to-top characterization parameter	0.4	
ψ _{JB}	Junction-to-board characterization parameter	17.4	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics, $V_{BIAS} = 5.0\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full) and $V_{BIAS} = 5.0\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS							
I_Q , V_{BIAS}	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{BIAS}$, $V_{ON} = 5.0\text{ V}$	Full		20.4	26.0	μA
I_{SD} , V_{BIAS}	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full		1.1	1.5	μA
I_{SD} , V_{IN}	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full			0.1	μA
						0.1	
						0.1	
						0.1	
						0.1	
I_{ON}	ON pin leakage current	$V_{ON} = 5.5\text{ V}$	Full			0.1	μA
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C		113		mV
RESISTANCE CHARACTERISTICS							
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$	$V_{IN} = 5.0\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
			$V_{IN} = 3.3\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
			$V_{IN} = 2.5\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
			$V_{IN} = 1.8\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
			$V_{IN} = 1.05\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
			$V_{IN} = 0.8\text{ V}$	25°C	4.4	5.0	$\text{m}\Omega$
				Full		5.6	
R_{PD}	Output pulldown resistance	$V_{IN} = 5.0\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	Full		224	233	Ω

7.6 Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full) and $V_{BIAS} = 2.5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS							
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{BIAS}$, $V_{ON} = 5.0\text{ V}$	Full		9.9	12.5	μA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full		0.5	0.65	μA
$I_{SD, VIN}$	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full			0.1	μA
						0.1	
						0.1	
						0.1	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	Full			0.1	μA
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C		83		mV
RESISTANCE CHARACTERISTICS							
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	25°C	4.7	5.3	m Ω
				Full		6.0	
			$V_{IN} = 1.8\text{ V}$	25°C	4.6	5.2	m Ω
				Full		5.8	
			$V_{IN} = 1.05\text{ V}$	25°C	4.5	5.1	m Ω
				Full		5.7	
			$V_{IN} = 0.8\text{ V}$	25°C	4.5	5.1	m Ω
				Full		5.7	
R_{PD}	Output pulldown resistance	$V_{IN} = 2.5\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	Full		224	233	Ω

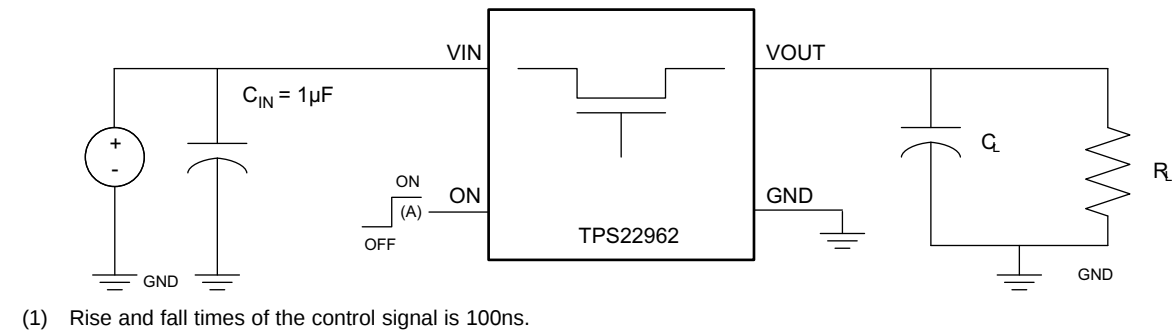
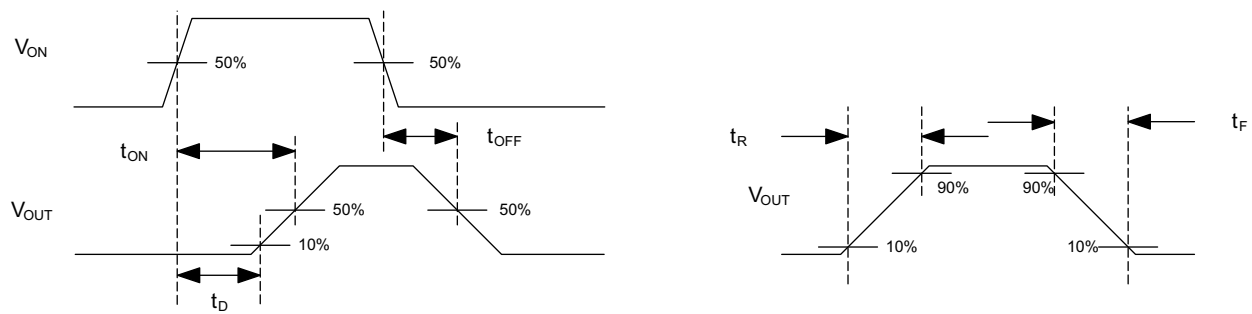
7.7 Switching Characteristics

Refer to the timing test circuit in [Figure 1](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN} = 5 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		2397		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			2663		
t _F	V _{OUT} fall time			2		
t _D	Delay time			1009		
V _{IN} = 3.3 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		1811		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			1756		
t _F	V _{OUT} fall time			2		
t _D	Delay time			897		
V _{IN} = 0.8 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		981		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			500		
t _F	V _{OUT} fall time			2		
t _D	Delay time			714		
V _{IN} = 2.5 V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10Ω, C _L = 0.1 μF		1576		μs
t _{OFF}	Turn-off time			8		
t _R	V _{OUT} rise time			1372		
t _F	V _{OUT} fall time			2		
t _D	Delay time			865		
V _{IN} = 1.8V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		1343		μs
t _{OFF}	Turn-off time			7		
t _R	V _{OUT} rise time			1006		
t _F	V _{OUT} fall time			2		
t _D	Delay time			815		
V _{IN} = 0.8 V, V _{ON} = 5V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		994		μs
t _{OFF}	Turn-off time			8		
t _R	V _{OUT} rise time			502		
t _F	V _{OUT} fall time			2		
t _D	Delay time			723		

TPS22962

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Figure 1. Test Circuit

Figure 2. Timing Waveforms

7.8 Typical Characteristics

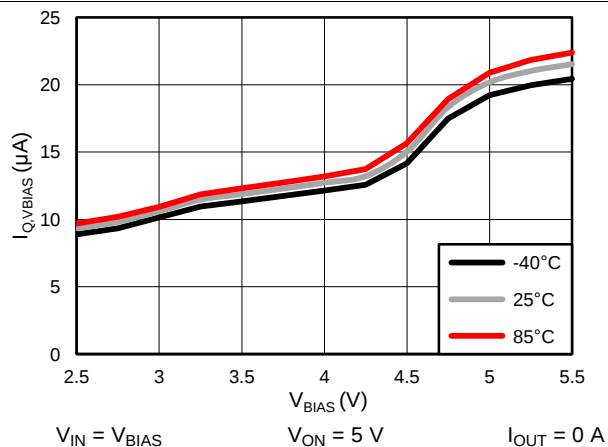


Figure 3. $I_{Q,VBIAS}$ vs V_{BIAS}

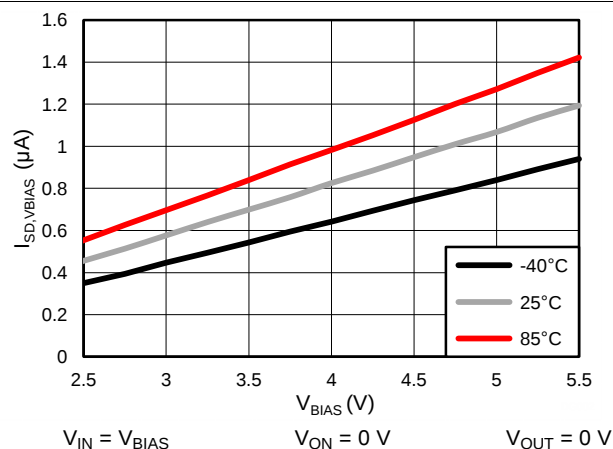


Figure 4. $I_{SD,VBIAS}$ vs V_{BIAS}

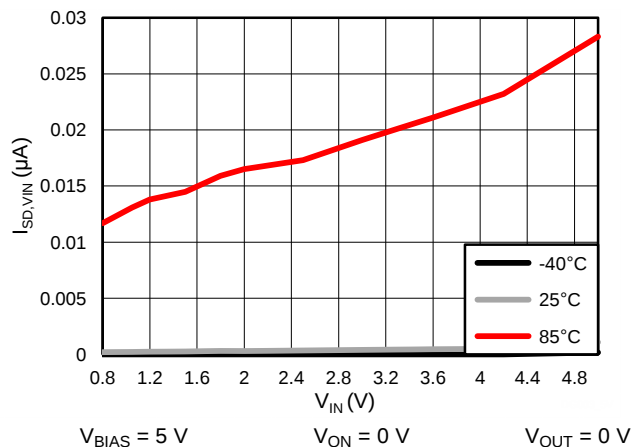


Figure 5. $I_{SD,VIN}$ vs V_{IN}

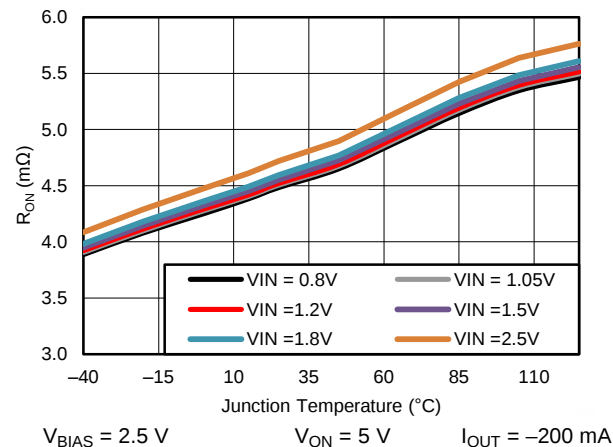


Figure 6. R_{ON} vs Junction Temperature

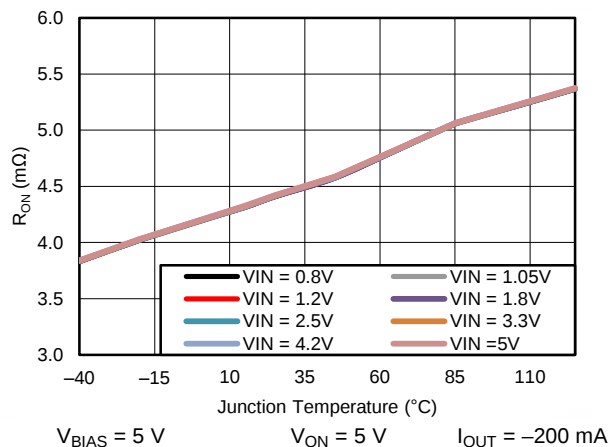


Figure 7. R_{ON} vs Junction Temperature

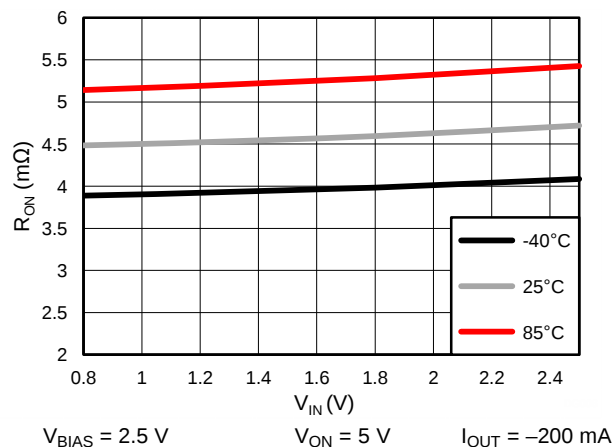


Figure 8. R_{ON} vs V_{IN}

Typical Characteristics (continued)

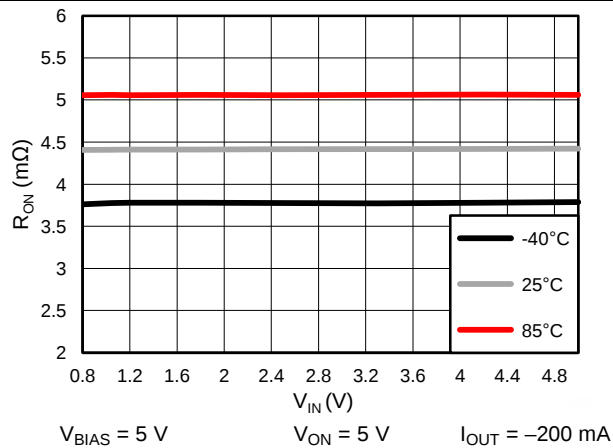


Figure 9. R_{ON} vs V_{IN}

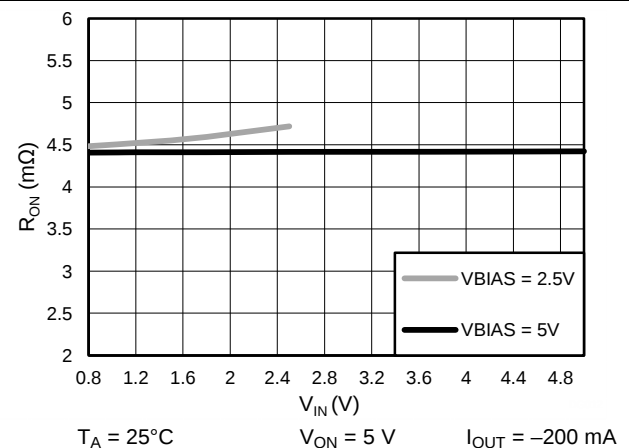


Figure 10. R_{ON} vs V_{IN}

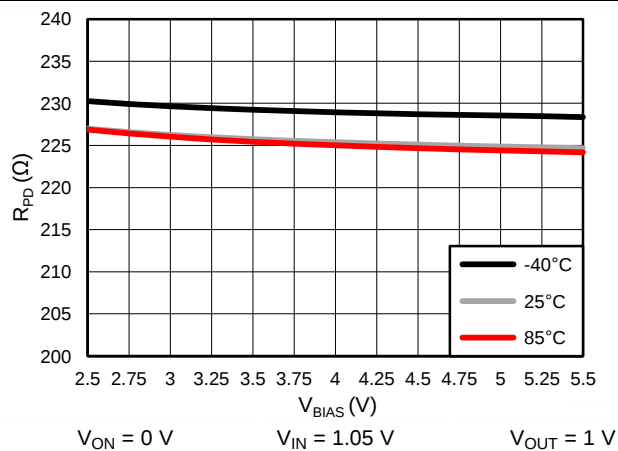


Figure 11. R_{PD} vs V_{BIAS}

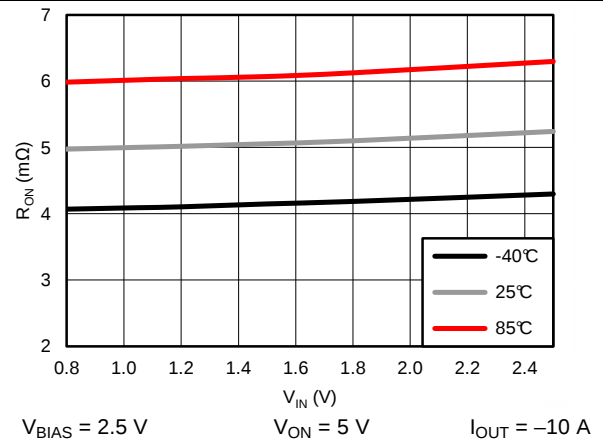


Figure 12. R_{ON} vs V_{IN} at 10A load

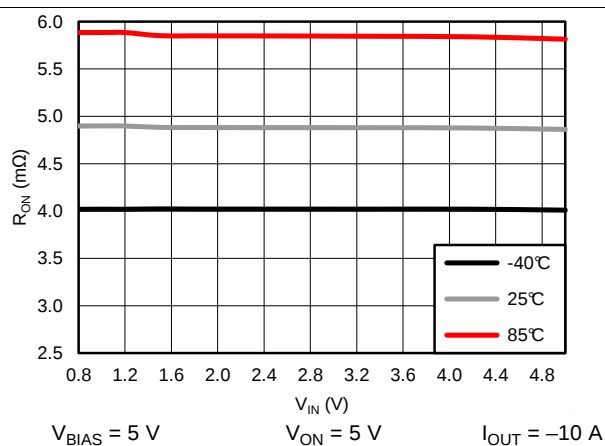


Figure 13. R_{ON} vs V_{IN} at 10A load

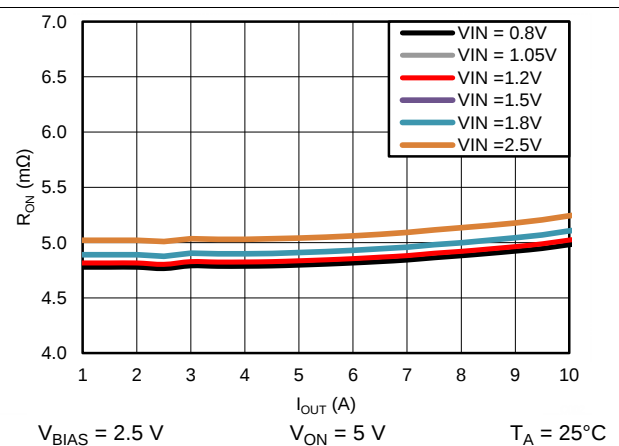


Figure 14. R_{ON} vs I_{OUT}

Typical Characteristics (continued)

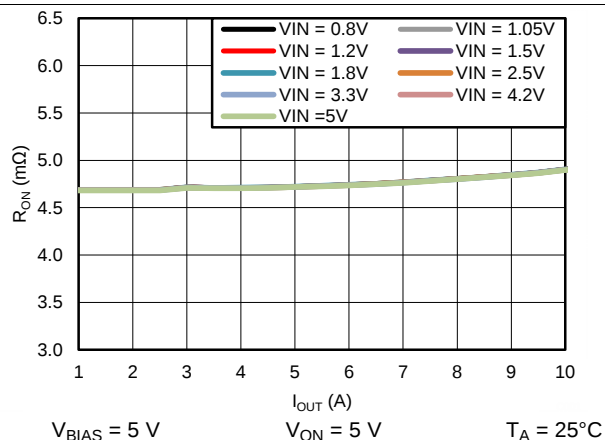


Figure 15. R_{ON} vs I_{OUT}

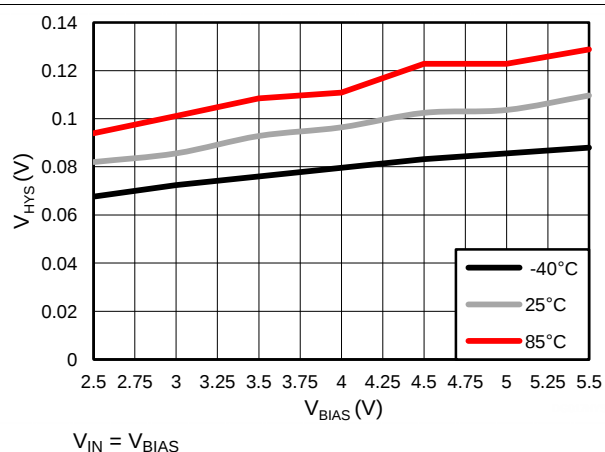


Figure 16. V_{HYS} vs V_{BIAS}

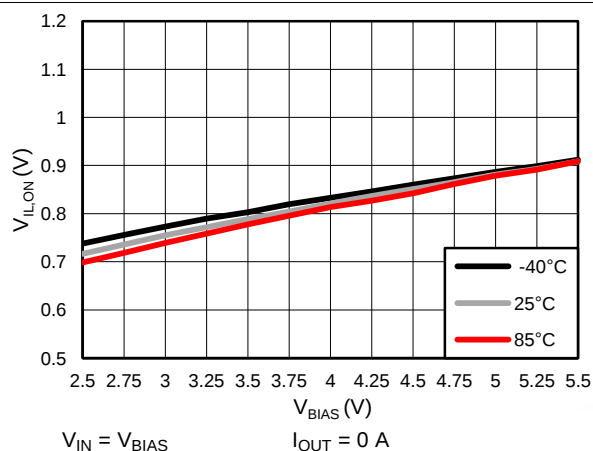


Figure 17. $V_{IL,ON}$ vs V_{BIAS}

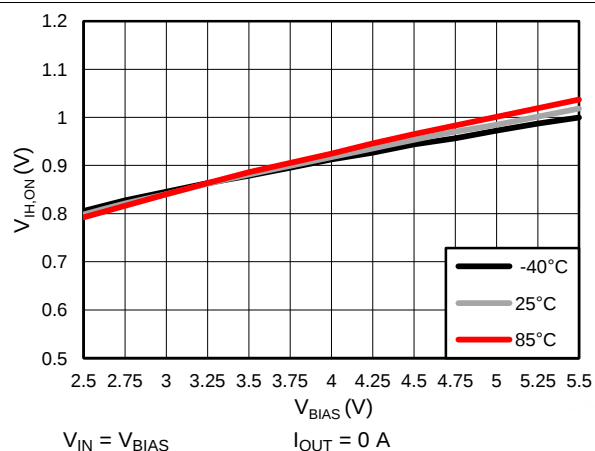


Figure 18. $V_{IH,ON}$ vs V_{BIAS}

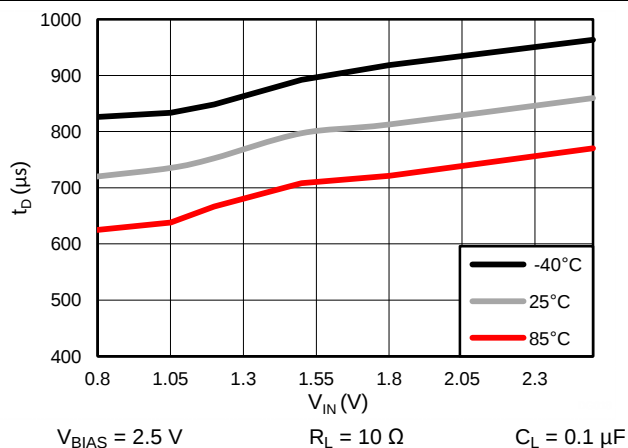


Figure 19. t_D vs V_{IN}

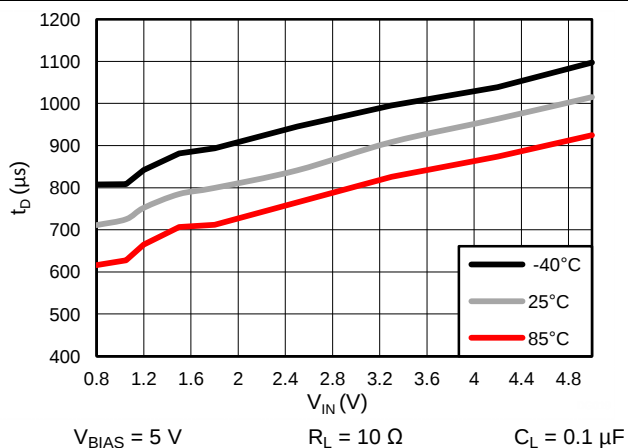
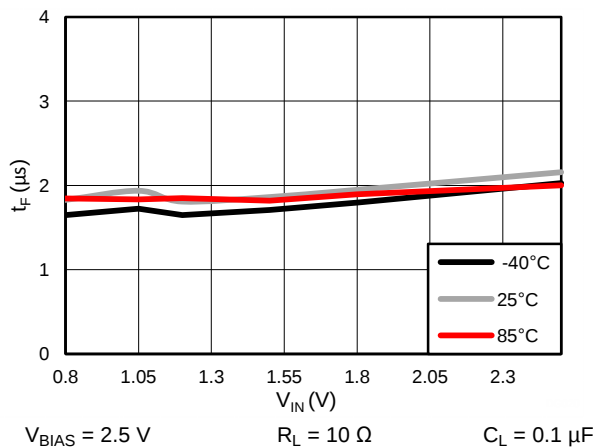
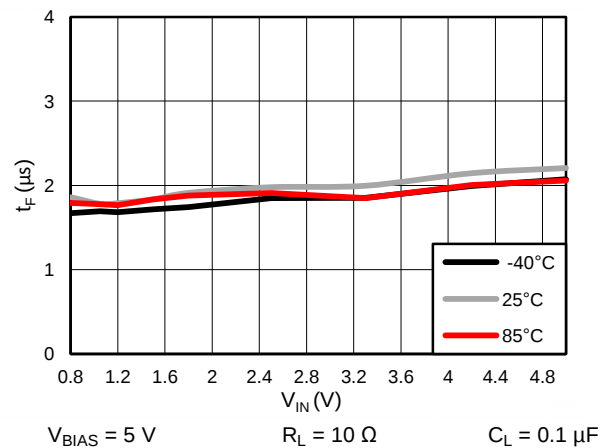
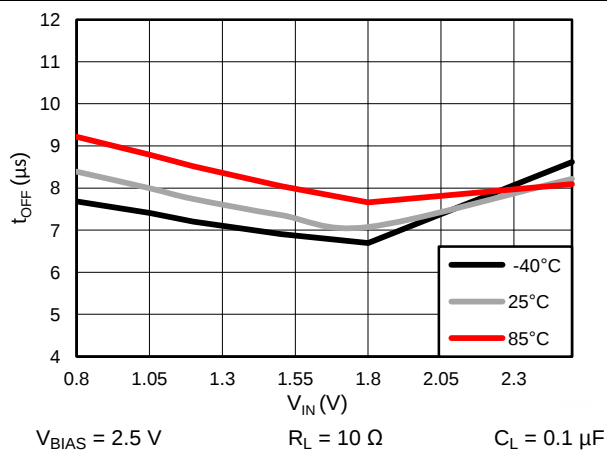
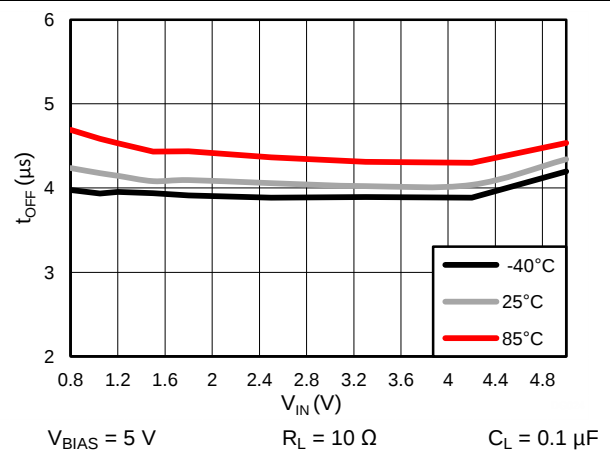
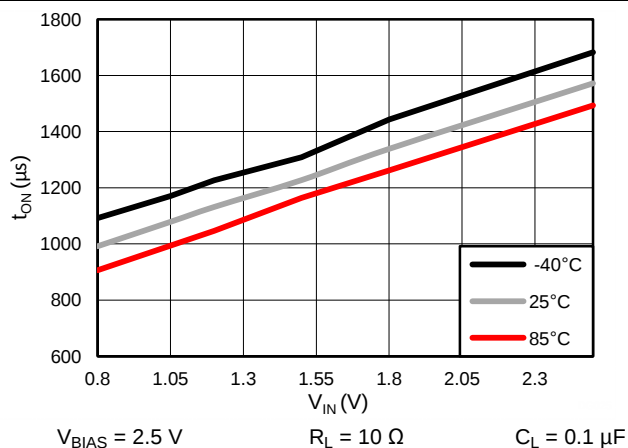
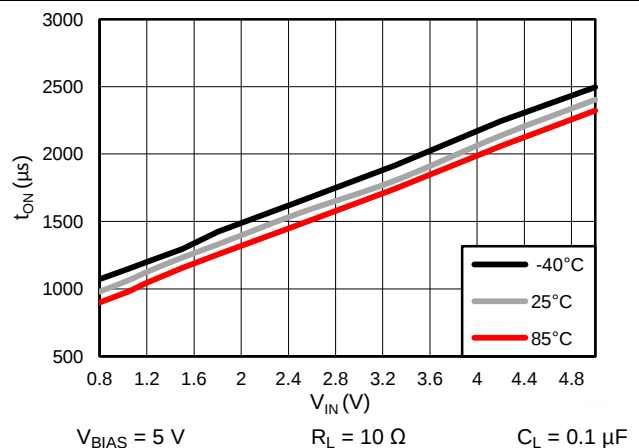


Figure 20. t_D vs V_{IN}

Typical Characteristics (continued)

Figure 21. t_F vs V_{IN}

Figure 22. t_F vs V_{IN}

Figure 23. t_{OFF} vs V_{IN}

Figure 24. t_{OFF} vs V_{IN}

Figure 25. t_{ON} vs V_{IN}

Figure 26. t_{ON} vs V_{IN}

Typical Characteristics (continued)

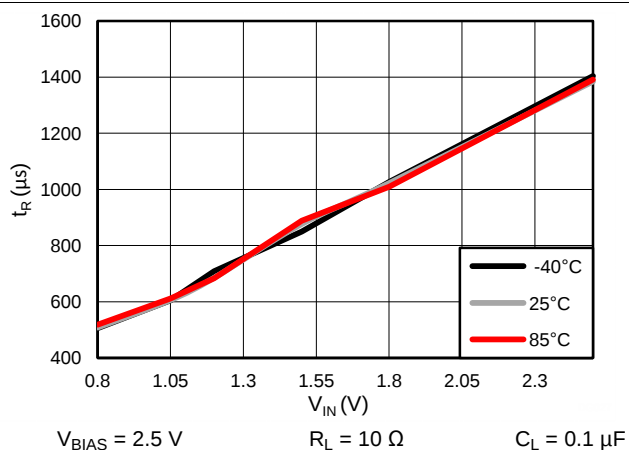


Figure 27. t_R vs V_{IN}

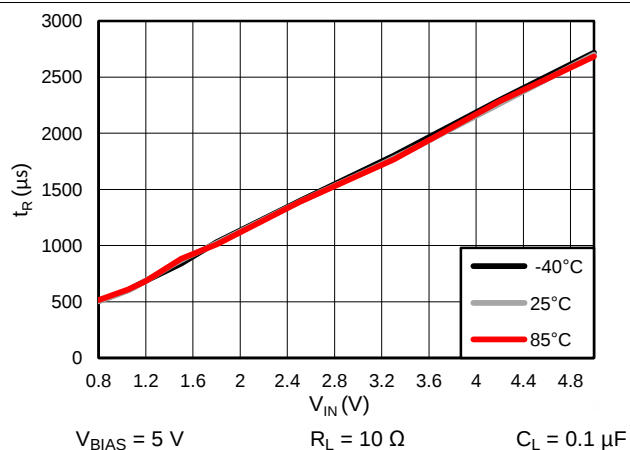


Figure 28. t_R vs V_{IN}

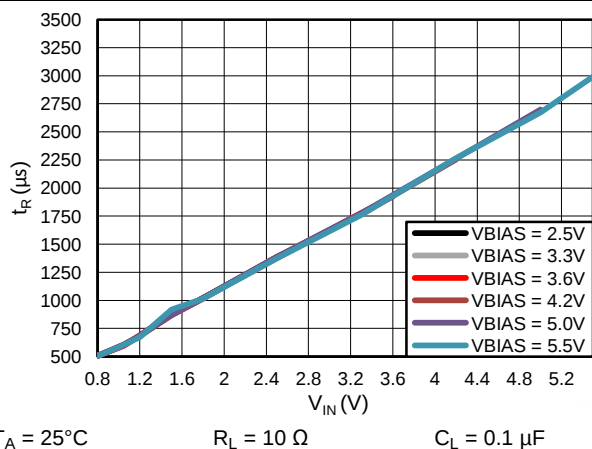


Figure 29. t_R vs V_{IN} for Various V_{BIAS}

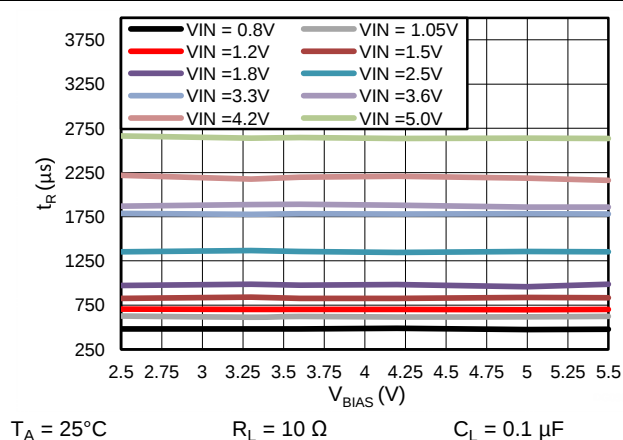


Figure 30. t_R vs V_{BIAS} for Various V_{IN}

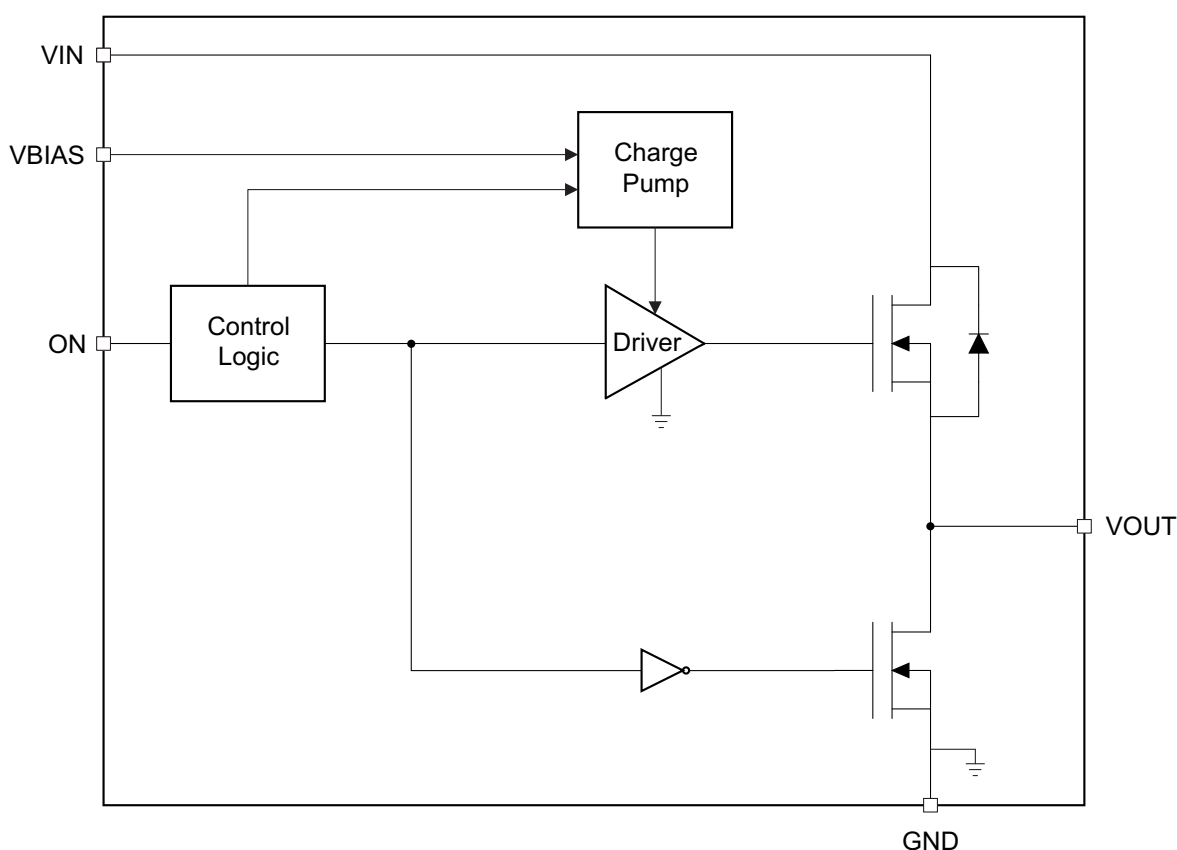
8 Detailed Description

8.1 Overview

The device is a 5.5 V, 10 A load switch in a 8-pin SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On/off Control

The ON pin controls the state of the load switch, and asserting the pin high (active high) enables the switch. The ON pin is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

Feature Description (continued)

8.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device, but a ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

8.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the N-channel MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

8.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device may still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the Electrical Characteristics table. See Figure 31 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} . Performance of the device is not guaranteed for $V_{IN} > V_{BIAS}$.

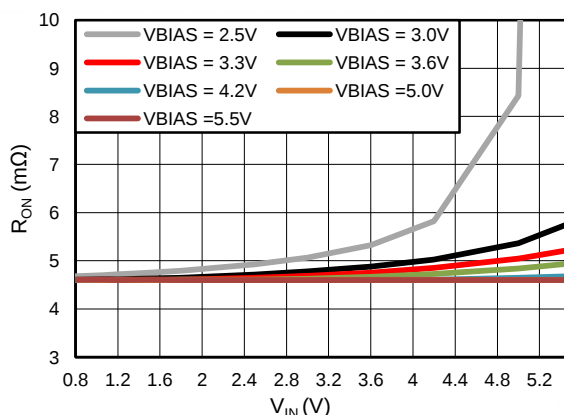


Figure 31. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

8.4 Device Functional Modes

Table 1 shows the connection of V_{OUT} depending on the state of the ON pin.

Table 1. V_{OUT} Connection

ON	V_{OUT}
L	GND
H	V_{IN}

9 Applications and Implementation

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

9.2 Typical Application

This application demonstrates how the TPS22962 can be used to power downstream modules with large capacitances. The example below is powering a 100-μF capacitive output load.

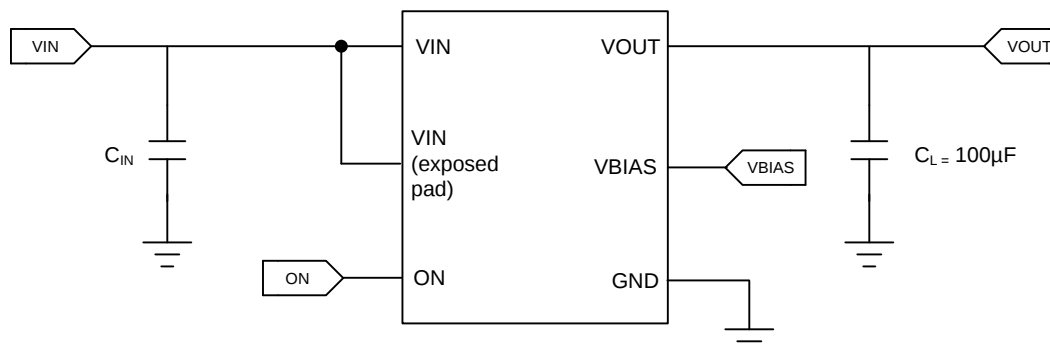


Figure 32. Typical Application Schematic for Powering a Downstream Module

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5.0 V
V_{BIAS}	5.0 V
Load current	10 A

9.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current

9.2.2.1 V_{IN} to V_{OUT} Voltage Drop

The V_{IN} to V_{OUT} voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 1 to calculate the V_{IN} to V_{OUT} voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = voltage drop from V_{IN} to V_{OUT}
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt} \quad (2)$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

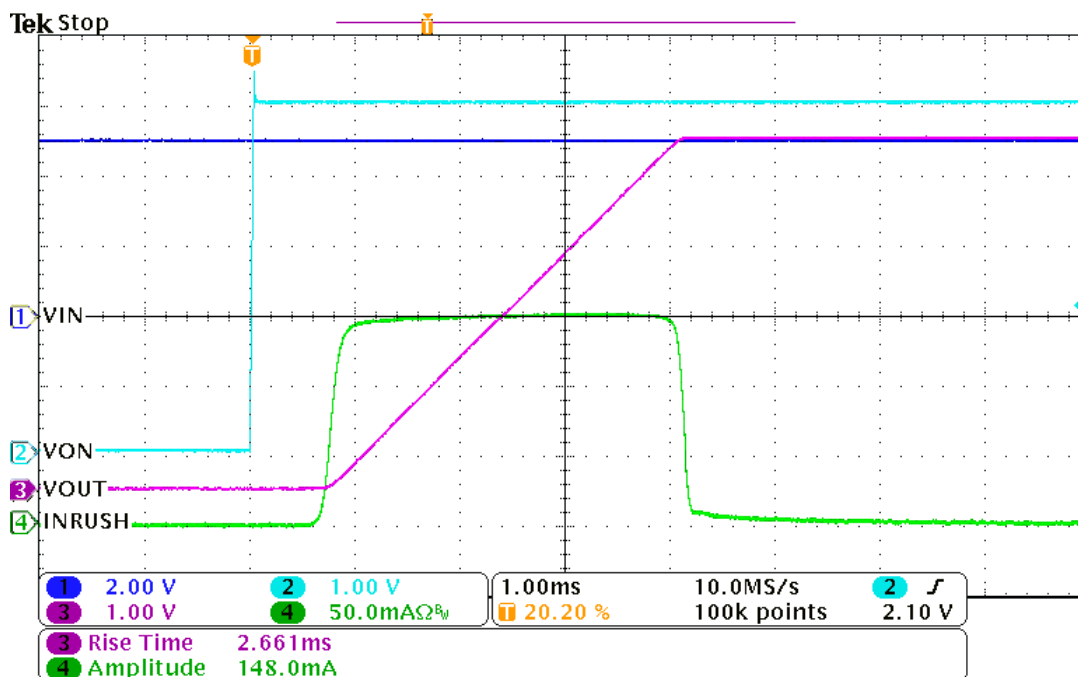


Figure 33. Inrush Current ($V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 5 \text{ V}$, $C_L = 100 \mu\text{F}$)

9.2.2.3 Thermal Considerations

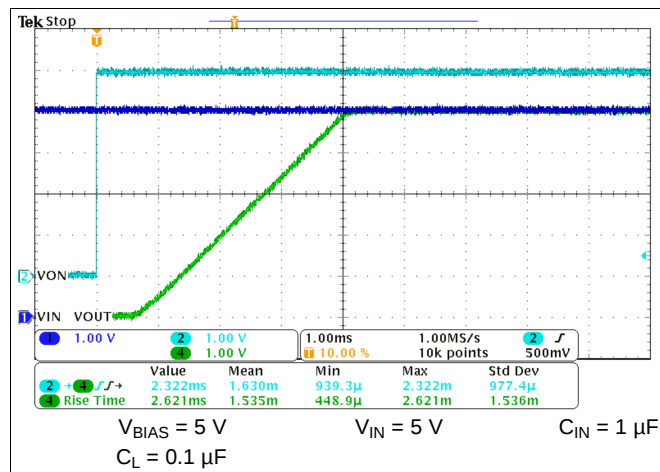
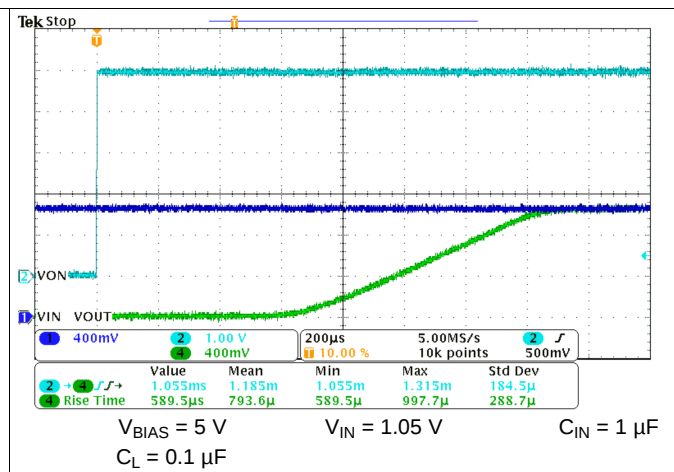
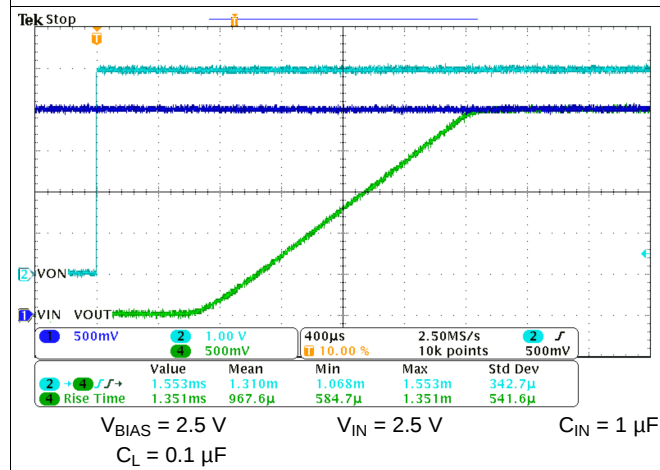
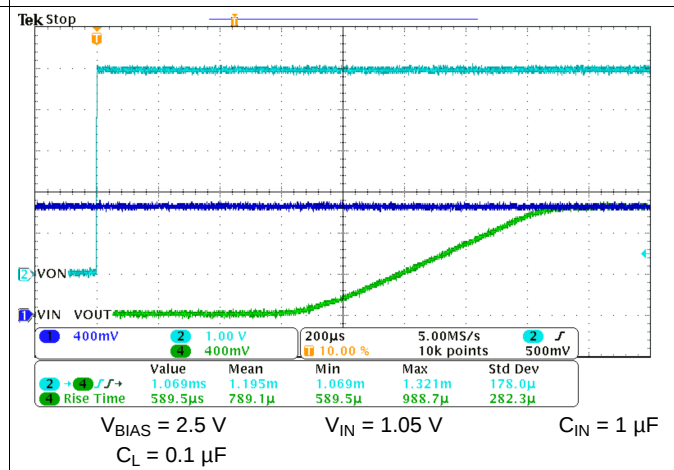
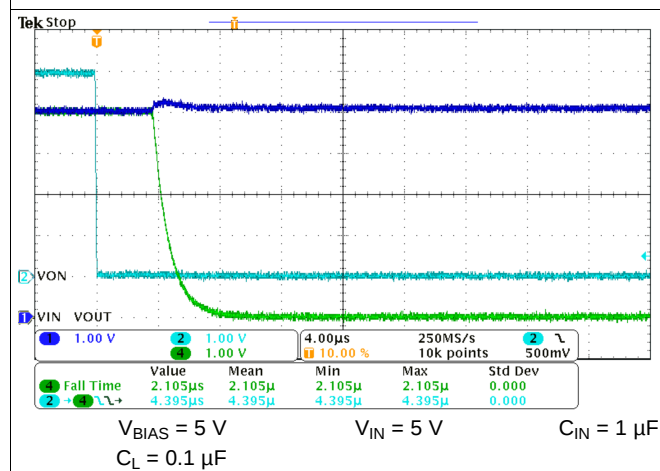
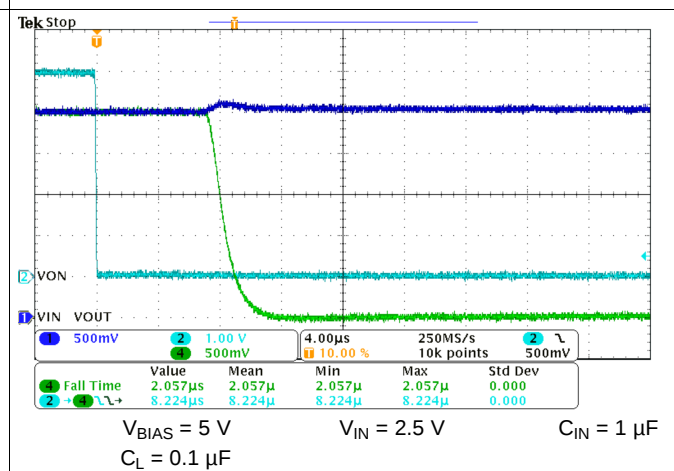
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{\text{D(max)}}$ for a given output current and ambient temperature, use Equation 3.

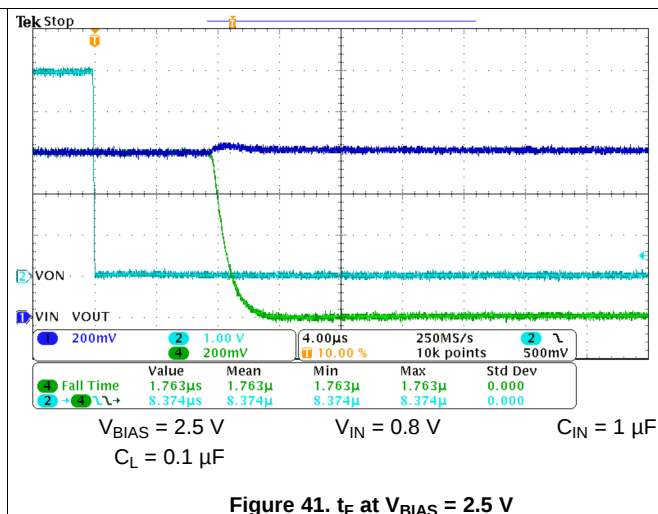
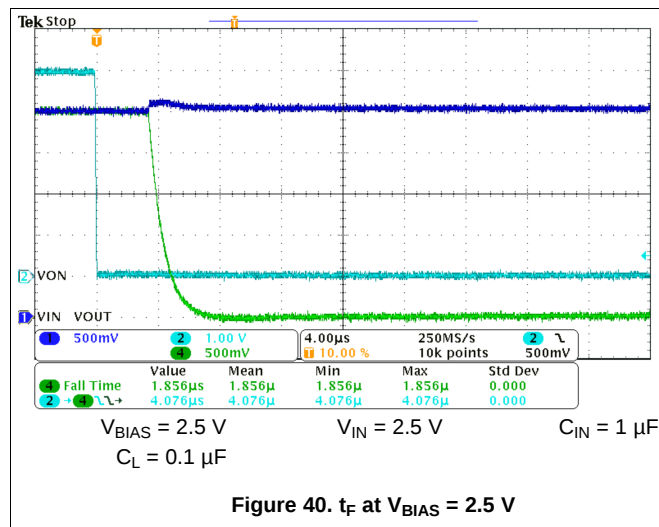
$$P_{\text{D(MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{\theta_{\text{JA}}} \quad (3)$$

where

- $P_{\text{D(max)}}$ = maximum allowable power dissipation
- $T_{\text{J(max)}}$ = maximum allowable junction temperature (125°C for the TPS22962)
- T_{A} = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

9.2.3 Application Curves


Figure 34. t_R at $V_{BIAS} = 5\text{ V}$

Figure 35. t_R at $V_{BIAS} = 5\text{ V}$

Figure 36. t_R at $V_{BIAS} = 2.5\text{ V}$

Figure 37. t_R at $V_{BIAS} = 2.5\text{ V}$

Figure 38. t_F at $V_{BIAS} = 5\text{ V}$

Figure 39. t_F at $V_{BIAS} = 5\text{ V}$



10 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.5 V and V_{IN} range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1 μF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

11 Layout

11.1 Layout Guidelines

- V_{IN} and V_{OUT} traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The V_{IN} pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The V_{OUT} pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{IN} bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The V_{BIAS} pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-μF ceramic with X5R or X7R dielectric.

11.2 Layout Example

○ VIA to Power Ground Plane

⌋ VIA to VIN Plane

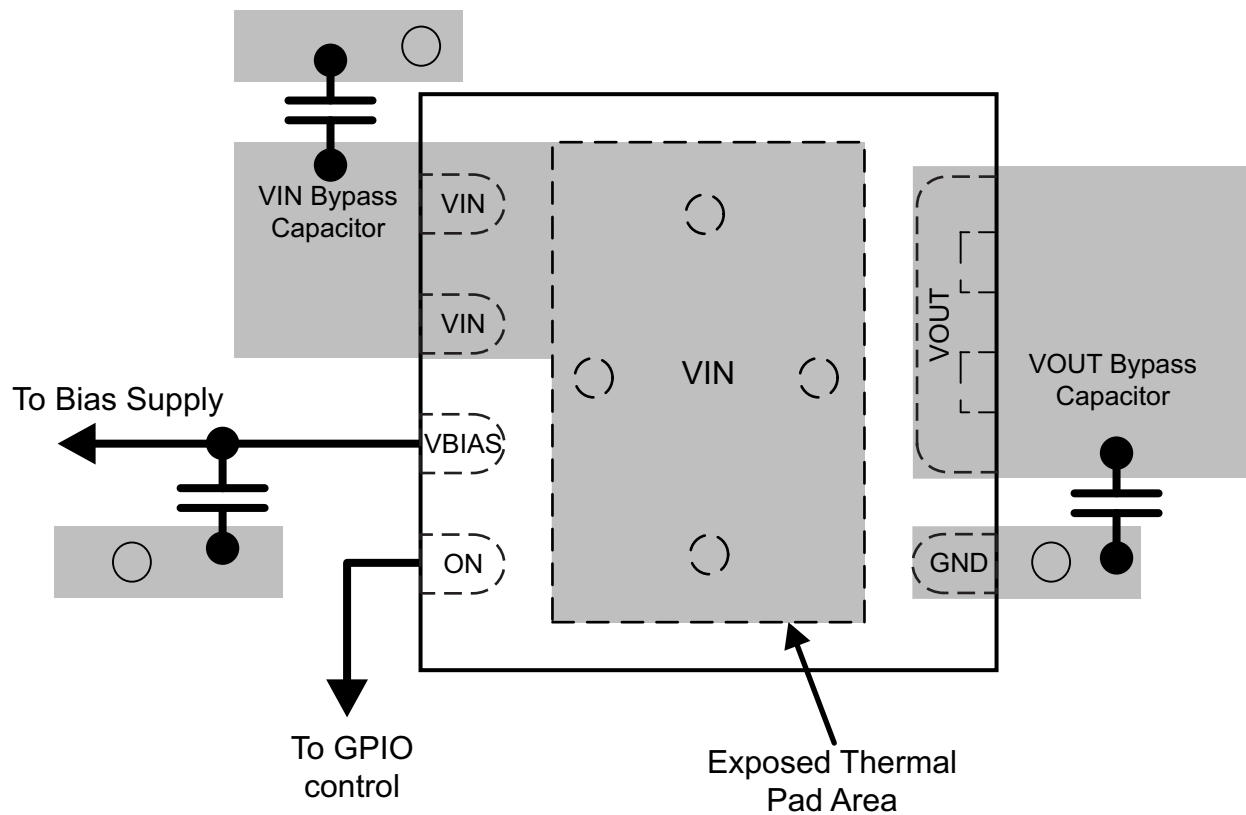


Figure 42. Recommended Board Layout

12 器件和文档支持

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22962DNYR	ACTIVE	WSO	DNY	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	962A0	Samples
TPS22962DNYT	ACTIVE	WSO	DNY	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	962A0	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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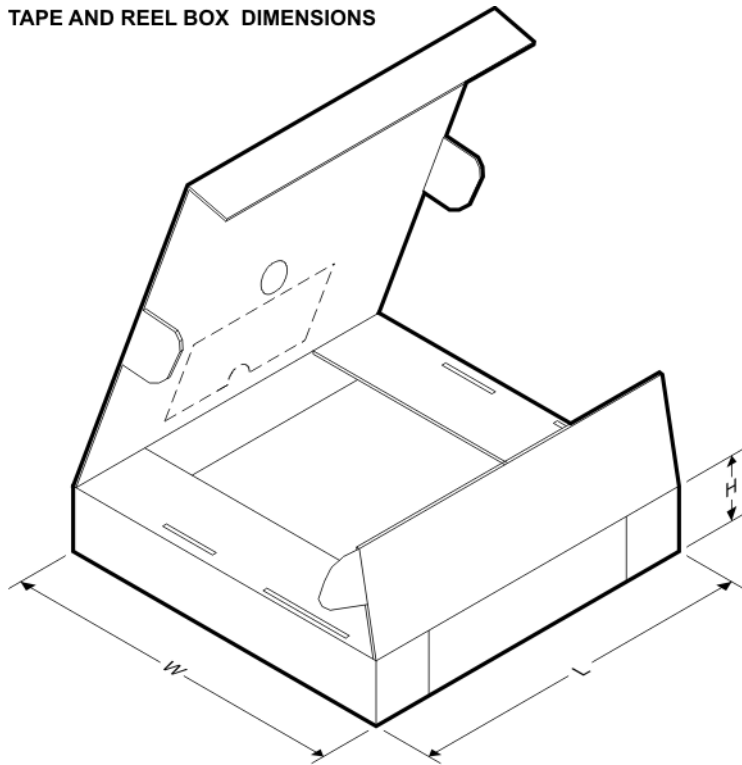
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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22962DNYR	WSO	DNY	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS22962DNYT	WSO	DNY	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

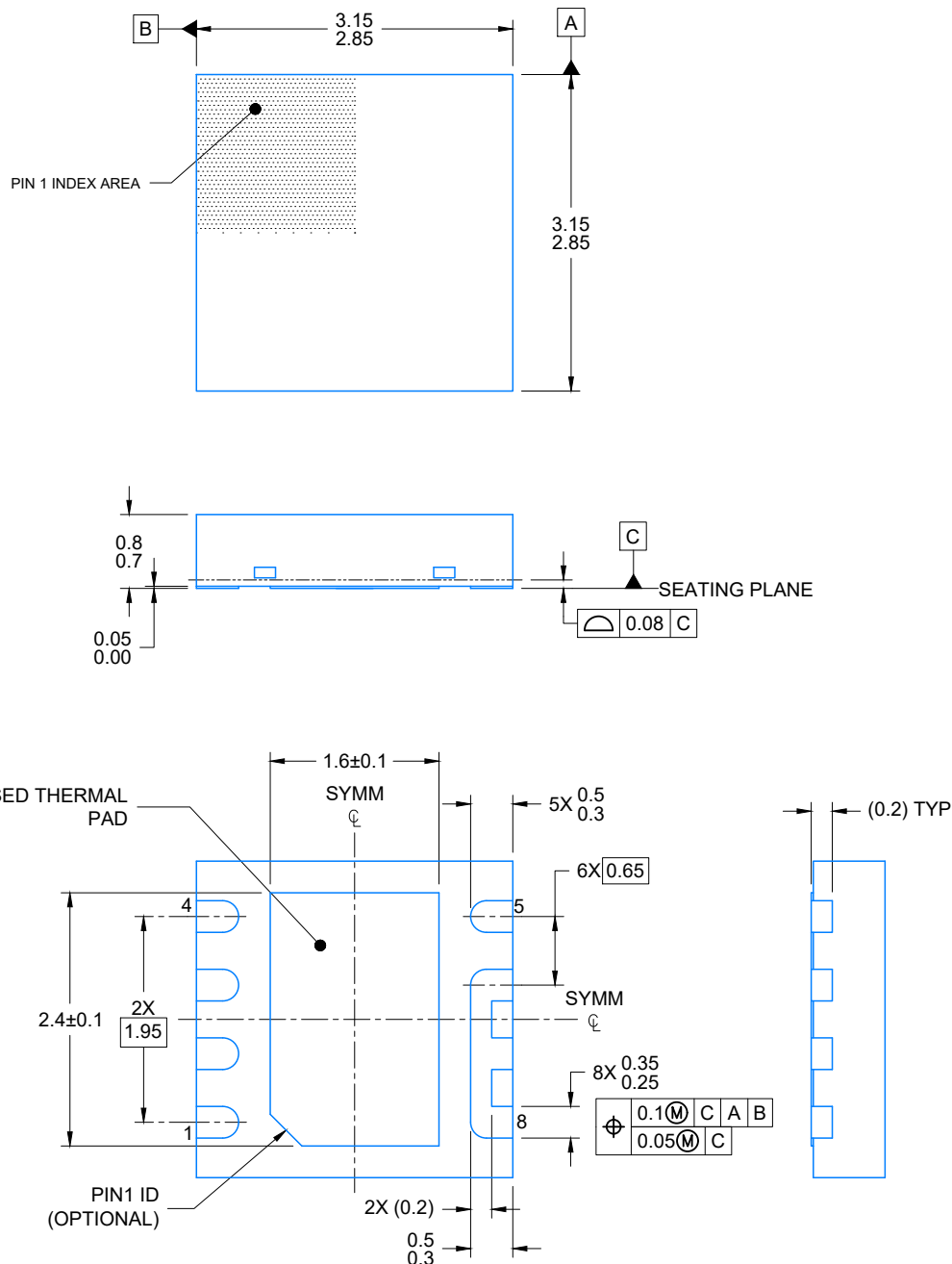
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22962DNYR	WSO	DNY	8	3000	367.0	367.0	38.0
TPS22962DNYT	WSO	DNY	8	250	213.0	191.0	35.0

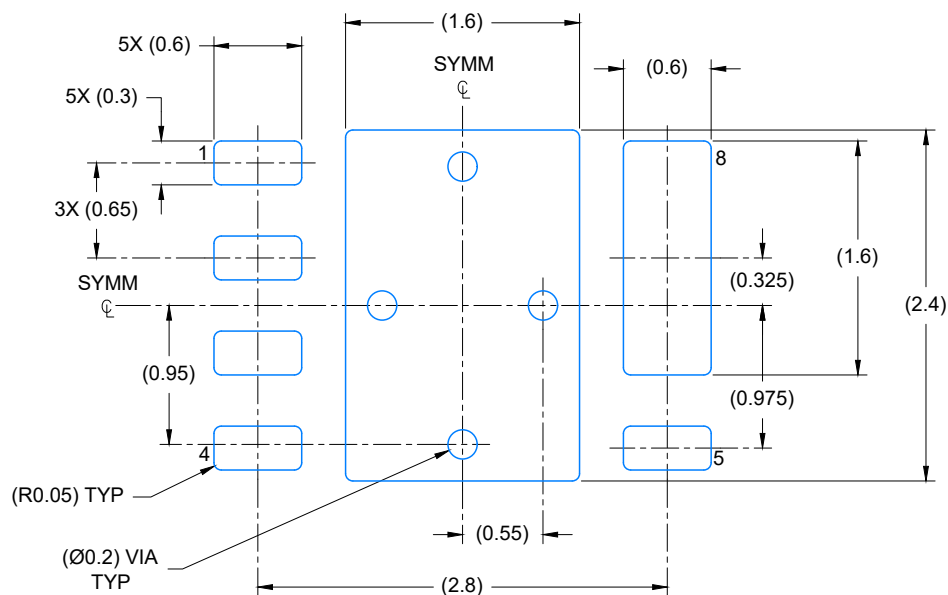
PLASTIC QUAD FLATPACK- NO LEAD



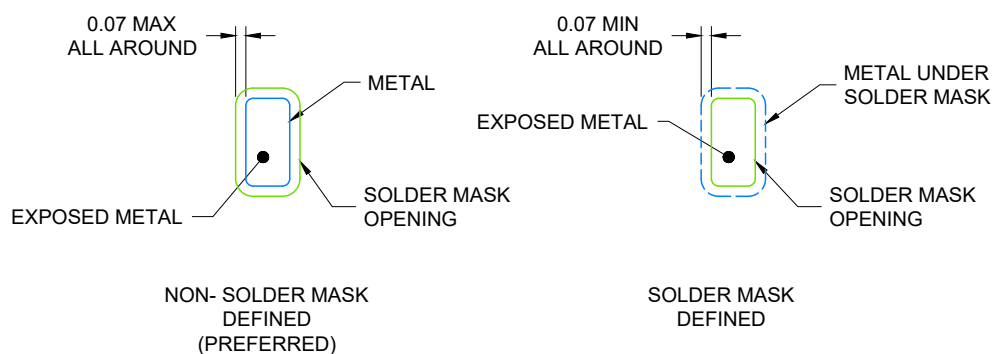
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

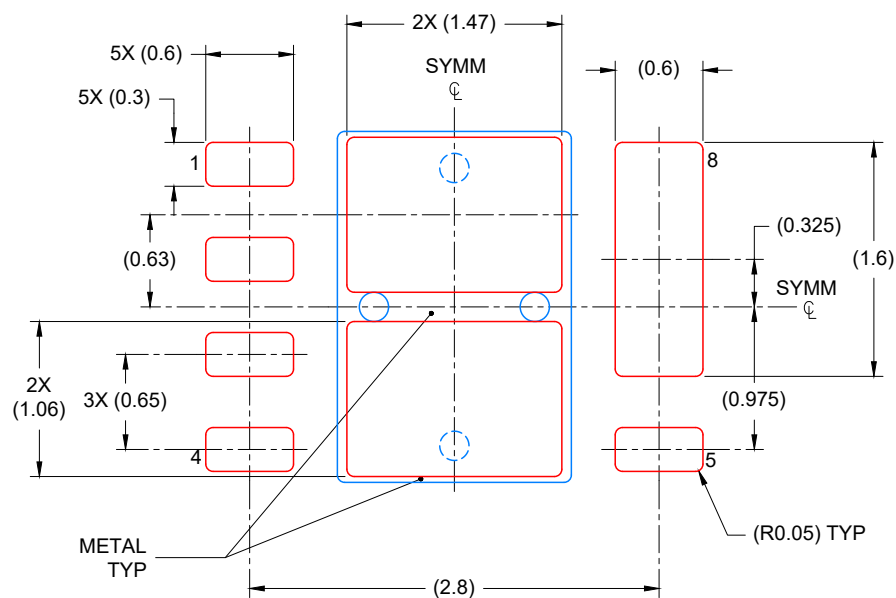


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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