SmartMX2 family P60D080 and P60D144

Secure high-performance dual interface smart card controller

Rev. 1 — 1 September 2010 Objective short data sheet
197210 PUBLIC

1. Introduction

The new NXP Semiconductors SmartMX2 P60 family was created in order to cover all important market requests for state-of-the-art security chip controllers:

- Innovative and unique security measures, Common Criteria certified
- Superior transaction and personalization time
- Broadest portfolio of memory configurations with contact, dual-interface and contactless on a single platform
- Proven SmartMX reliability, interoperability and RF excellence for shortest time-to-market
- Market benchmark in view of cost-performance ratio

Further feature improvements in comparison to the existing approved SmartMX P5 family:

- Significant increases in controller and crypto performance
- Further extended CPU instructions for Java and C code
- Comprehensive hardware support for efficient and secure OS implementation
- Highest transaction and personalization speed
- Excellent power efficiency
- New-generation Fame2 crypto coprocessor for RSA/ECC
- New-generation Symmetric Block Cipher (SBC) crypto coprocessor for DES/AES
- Advanced 90 nm CMOS technology

Other important SmartMX2 P60 differentiators in the market are:

- Optional implementation of MIFARE Plus and MIFARE DESFire EV1 functionality to enable easy coverage of application convergence
- New development tool suite, totally revised and based on an optimized close-to-product true bond-out chip emulation approach
- Broadest portfolio of certified package variations

2. General description

The P60D080 and P60D144 devices are members of the new SmartMX2 Family and offer with their two different EEPROM size variations a common set of functional blocks and interfaces, supporting high-performance, high-security contact, dual-interface and contactless applications. Figure 1 shows the block diagram of the modular controller architecture consisting of the following blocks and features:

- SmartMX2 CPU with enhanced application instruction set supporting 32-/24-/16-/8-bit move, logical and arithmetic functions
- Fame2 coprocessor based on innovative power-efficient and fast architecture for optimized RSA/ECC cryptography
- SBC coprocessor interface with multiple data/key register sets now supporting both AES and Triple-DES
- ISO/IEC 7816 data transfer improved with enhanced protocol support for T=0 and T=1 protocols
- ISO/IEC 14443 Type A contactless interface unit optimized also for small antenna dimensions
- Fully concurrent operation of contact and contactless communication
- New Copy Machines supporting direct memory access (DMA) to memories and all SFRs
- Cyclic Redundancy Check (CRC) coprocessors 16-bit/32-bit
- Memory Management Unit (MMU) with 16 cache segments
- New security features especially targeting combined laser light attacks and integrity of code execution and data fetch
- Development tool suite based on approved suppliers Keil and Ashling
  - μVision4 user interface
  - New and high-performance emulation hardware “SmartICE series”
- High-memory SoftMasking DIF device for code development purposes
- Common Criteria security certified high-performance crypto library supporting various algorithms
- Consequent family concept with regard to all future platforms of the P60 family

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3. Features and benefits

3.1 Product specific features

- EEPROM: choice of 80 KB or 144 KB
  - Data retention time: 25 years minimum
  - Endurance: 500000 cycles
  - Versatile EEPROM programming: 1 B to 256 B at a time
- ROM: 384 KB
- RAM: 8.125 KB (8320 B)
  - 5632 B CXRAM (including 256 B IRAM) usable for CPU
  - 2688 B FXRAM usable for Fame2 or CPU
- SmartMX2 CPU
  - orthogonal instruction set offering 32-/24-/16-/8-bit instructions optimized for secured and low power smart card applications
- Enhanced high-performance secured Public Key Infrastructure (PKI) coprocessor (RSA, ECC) Fame2
- Enhanced high-performance secured hardware support for symmetric block cipher (SBC) algorithms
  - Secured dual/triple-DES coprocessor
  - Secured AES coprocessor
  - Multiple key and data register sets supporting parallel data/key loading and calculation
- True Random Number Generator (compliant to AIS-31)
- 16-bit and 32-bit CRC coprocessor supporting fast memory verify functionality
- Memory Management Unit (MMU)
  - 16 segment cache entries and performance improvements
  - supporting integral concept for secure code fetch and execution
- Copy Machines offering data transfer between all Special Function Registers and all memory instances without CPU interaction
- Watchdog Timer supporting secure code execution
- Time Stamp Counter, Real Time Clock
- ISO/IEC 7816 contact interface (UART) and ISO/IEC 14443A Contactless Interface Unit (CIU)
  - ISO/IEC 7816 contact interface (UART) offering hardware support for ISO/IEC 7816 T=0 and T=1 protocol stack implementation
  - ISO/IEC 14443A Contactless Interface Unit (CIU) supporting data rates of 106 kbit/s, 212 kbit/s, 424 kbit/s, 848 kbit/s and offering hardware support for ISO/IEC 14443 T=CL protocol stack implementation
  - Hardware support for automatic WTX generation for both ISO/IEC 7816 UART and ISO/IEC 14443 CIU
  - support of concurrent operation of both ISO/IEC 7816 and ISO/IEC 14443 interface
  - continuos operation from 1.62 V up to 5.5 V supported
- –25 °C to +85 °C ambient temperature

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3.2 Security features

- Outstanding Glue Logic chip layout approach:
  - Most efficient and proven protection against reverse engineering
  - Based on avoidance of any logical layout block recognition
- Secure Fetch (Code and Data)
- Active and dynamic shielding
- Enhanced security sensors:
  - Low and high clock frequency sensor
  - Low and high temperature sensor
  - Low and high supply voltage sensor
  - Single Fault Injection (SFI) attack detection
  - Light sensors (included integrated memory light sensor functionality)
- Electronic fuses for safeguarded mode control
- Clock input filter for protection against spikes
- Power-up and power-down reset
- Memory security (encryption and physical measures) for RAM, EEPROM and ROM
- Memory Management Unit (MMU) including memory protection:
  - Secure multi application operating systems via two different operation modes: System mode and User mode
  - OS controlled access restriction mechanism to peripherals in User mode
  - Memory mapping up to 8-MB code memory
  - Memory mapping up to 8-MB data memory
- Built-in integral concept for secure code execution covering code fetch, MMU and CPU
- Optional disabling of ROM read instructions by code executed in EEPROM
- Optional disabling of any code execution out of RAM
- Optional Unique ID for each die
- Optional programmable card disable feature
- EEPROM programming:
  - Hardware sequencer controlled
  - Enhanced error correction mechanism
- 128-B or 264-B EEPROM for customer-defined Security FabKey:
  - Featuring batch, wafer or die-individual security data
  - Encrypted diversification features available on request
- 14 B user write protected security area in EEPROM (byte access, inhibit functionality per byte)
- 32 B write once protected security area in EEPROM (bit access)
- 32 B user read only protected security area in EEPROM (byte access)
- Total useable EEPROM for customer OS (including optional FabKey areas) and excluding the MIFARE Plus and DESFire EV1 implementations
  - P60D080: 81408 bytes + above 78 bytes within protected security area
  - P60D144: 146944 bytes + above 78 bytes within protected security area
- Customer specific EEPROM initialization available

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4. Applications

- E-passports
- ID cards
- Health cards
- Electronic driving licences
- Contact and contactless banking
- Digital Signature
- Conditional Access (Pay TV)
- High-security access management
- Authentication
- Trusted platform modules
- Multi-application cards

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions [1]		Min	Typ	Max	Unit
V_{DD}	supply voltage	Class A: 5 V range		4.5	5.0	5.5	V
		Class B: 3 V range		2.7	3.0	3.3	V
		Class C: 1.8 V range		1.62	1.8	1.98	V

[1] **Remark:** continuos operation from 1.62 V up to 5.5 V supported

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6. Ordering information

Table 2. Feature table (EEPROM and RAM sizes without applied implementation of MIFARE Plus and/or DESFire EV1)

Product type	EEPROM [KB]	user ROM [KB]	total RAM [KB]	CXRAM [KB]	FXRAM [KB]	Coprocessor			MMU	Copy machines	ISO/ IEC 7816 IO pads	interface option
						Fame2	DES	AES				
P60D080	80	384	8.125	5.5	2.625	yes	yes	yes	yes	2	3	ISO/IEC 7816 + ISO/IEC 14443
P60D144	144	384	8.125	5.5	2.625	yes	yes	yes	yes	2	3	ISO/IEC 7816 + ISO/IEC 14443

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
P60D080PU15	FFC	12 inch wafer (sawn; 150 μm thickness; on film frame carrier; electronic fail die marking according to SECSII format)	NAU000
P60D144PU15			
P60D080PU75	FFC	12 inch wafer (sawn; 75 μm thickness; on film frame carrier; electronic fail die marking according to SECSII format)	NAU000
P60D144PU75			
P60D080PA4	MOB4	contactless chip card module (super 35 mm tape format, module thickness 320 μm)	SOT500-2
P60D144PA4			
P60D080PA6	MOB6	contactless chip card module (super 35 mm tape format, module thickness 250 μm)	SOT500-3
P60D144PA6			
P60D080PX1	PDM1.1	dual interface chip card module (Plug-in type; super 35 mm tape format, 8-contact)	SOT658-3
P60D144PX1			
P60D080PX0	PDM1.1	dual interface chip card module (super 35 mm tape format, 8-contact)	SOT658-3
P60D144PX0			
P60D080PX30	Pd-PDM1.1	palladium plated dual interface chip card module (super 35 mm tape format, 8-contact)	SOT658-3
P60D144PX30			

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7. Functional diagram

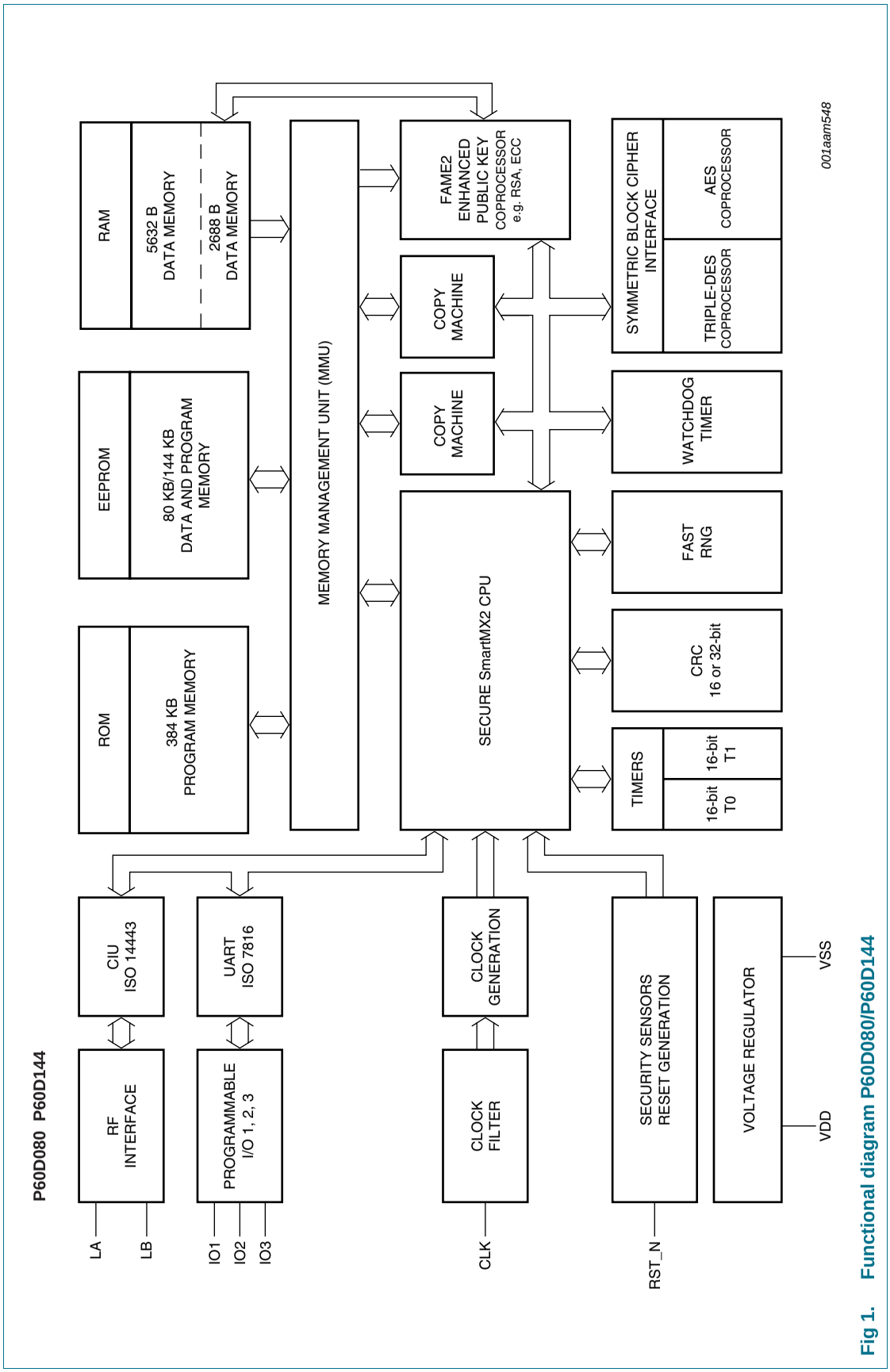


Fig 1. Functional diagram P60D080/P60D144

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8. Abbreviations

Table 4. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
DES	Digital Encryption Standard
DIF	Dual InterFace
ECC	Elliptic Curve Cryptography
ICE	Integrated Circuit Emulator
RSA	Rivest, Shamir and Adleman
SFR	Special Function Register

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9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SMX2_FAM_P60D080_D144_SDS v.1	20100901	Objective short data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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