ISL21007

Precision, Low Noise FGA Voltage References

FN6326
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The ISL21007 FGA™ voltage references are extremely low power, high precision, and low noise voltage references fabricated on Intersil's proprietary Floating Gate Analog (FGA) technology. The ISL21007 features very low noise (4.5µV_{P-P} for 0.1Hz to 10Hz) and very low operating current (150µA, Max). In addition, the ISL21007 family features guaranteed initial accuracy as low as ±0.5mV.

This combination of high initial accuracy, low drift, and low output noise performance of the ISL21007 enables versatile high performance control and data acquisition applications with low power consumption.

Applications

- High Resolution A/Ds and D/As
- Digital Meters
- Bar Code Scanners
- Base Stations
- Battery Management/Monitoring
- Industrial/Instrumentation Equipment

Features

- Reference Output Voltage 1.250V, 2.048V, 2.500V, 3.000V
- Input Voltage Range
  ISL21007-12, 20, 25. . . . . 2.7V to 5.5V
  ISL21007-30. . . . . 3.2V to 5.5V
- Low Output Voltage Noise. . . . . 4.5µV_{P-P} (0.1Hz to 10Hz)
- Supply Current . . . . . 150µA (Max)
- Temperature Coefficient . . . . . .3ppm/°C (B grade)
- Operating Temperature Range. . . . . .-40°C to +125°C
- Package . . . . . 8 Ld SOIC
- Pb-Free (RoHS Compliant)

Related Literature

- For a full list of related documents, visit our website
  - ISL21007 product pages

TABLE 1. AVAILABLE OPTIONS

PART NUMBER	V_{OUT} OPTION (V)	INITIAL ACCURACY (mV)	TEMPCO. (ppm/°C)
ISL21007BFB812Z **(Obsolete. Recommended replacement part ISL21007CFB812Z)**	1.250	±0.5	3
ISL21007CFB812Z	1.250	±1.0	5
ISL21007DFB812Z	1.250	±2.0	10
ISL21007BFB820Z **(Obsolete. Recommended replacement part ISL21007CFB820Z)**	2.048	±0.5	3
ISL21007CFB820Z	2.048	±1.0	5
ISL21007DFB820Z **(Obsolete. Recommended replacement ISL21007CFB820Z)**	2.048	±2.0	10
ISL21007BFB825Z **(Obsolete. Recommended replacement part ISL21007CFB825Z)**	2.500	±0.5	3
ISL21007CFB825Z	2.500	±1.0	5
ISL21007DFB825Z	2.500	±2.0	10
ISL21007BFB830Z **(Obsolete. Recommended replacement ISL21007CFB825Z-TK)**	3.000	±0.5	3
ISL21007CFB830Z **(Obsolete. Recommended replacement ISL21007CFB825Z-TK)**	3.000	±1.0	5
ISL21007DFB830Z **(Obsolete. Recommended replacement ISL21007CFB825Z-TK)**	3.000	±2.0	10

Ordering Information

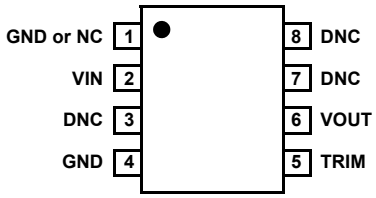
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} OPTION (V)	GRADE	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL21007CFB812Z	21007CF Z12	1.250	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB812Z	21007DF Z12	1.250	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007CFB820Z	21007CF Z20	2.048	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB820Z **(Obsolete recommended replacement ISL21007CFB820Z)**	21007DF Z20	2.048	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007CFB825Z	21007CF Z25	2.500	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB825Z	21007DF Z25	2.500	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007CFB830Z **(Obsolete, recommended replacement ISL21007CFB825Z-TK)**	21007CF Z30	3.000	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB830Z **(Obsolete, recommended replacement ISL21007CFB825Z-TK)**	21007DF Z30	3.000	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1k unit tape and reel option. Refer to TB347 for details on reel specifications.
3. For Moisture Sensitivity Level (MSL), see device information pages for ISL21007CFB812, ISL21007CFB820, ISL21007CFB825, ISL21007CFB830, ISL21007DFB812, ISL21007DFB820, ISL21007DFB825, ISL21007DFB830. For more information on MSL, see techbrief TB363.

Pin Configuration

ISL21007
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND or NC	Ground or No Connection
2	VIN	Power Supply Input Connection
4	GND	Ground
5	TRIM	Allows User Trim V_{OUT} ±2.5%
6	VOUT	Voltage Reference Output Connection
3, 7, 8	DNC	Do Not Connect; Internal Connection - Must Be Left Floating

Typical Application Circuit

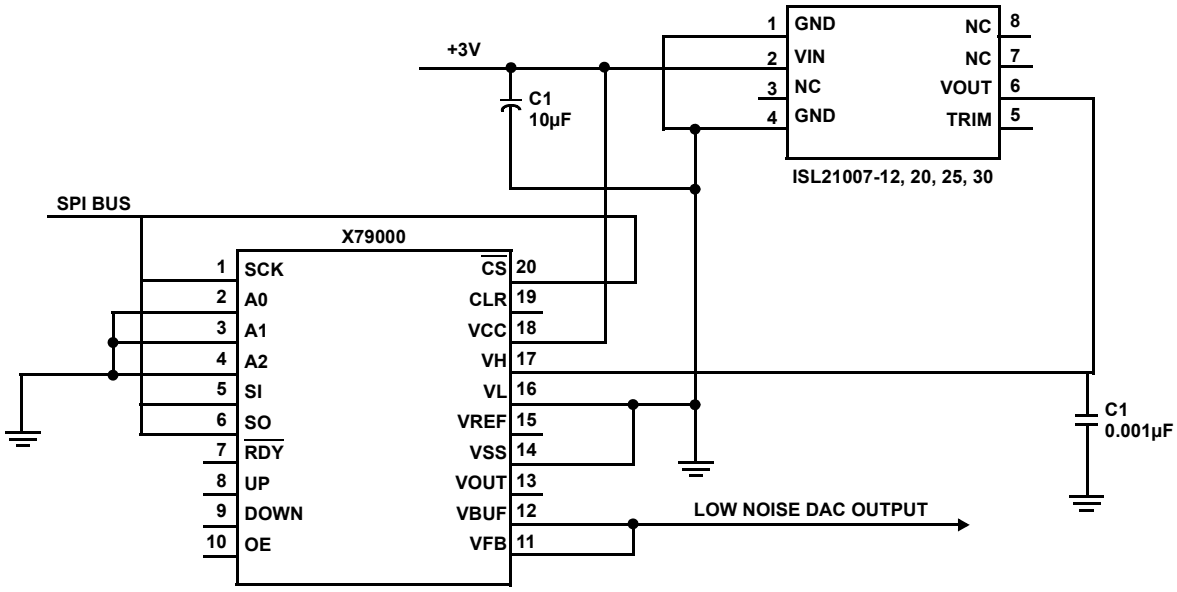


FIGURE 1. TYPICAL APPLICATION PRECISION 12-BIT SUBRANGING DAC

Absolute Voltage Ratings

Storage Temperature Range . . . . . -65°C to +150°C
Max Voltage VIN to GND . . . . . -0.5V to +6.5V
Max Voltage VOUT to GND (10s) . . . . . -0.5V to V_{OUT} + 1
Voltage on "DNC" pins . . . . . No connections permitted to these pins.
ESD Rating
Human Body Model (HBM) 6kV
Machine Model (MM) 600V
Charged Device Model (CDM) 2kV

Environmental Operating Conditions

X-Ray Exposure (Note 4) 10mRem

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
8 Ld SOIC 113.12
Continuous Power Dissipation (Note 5) . . . . . T_A = +70°C
8 Ld SOIC Derate 5.88mW/°C above +70°C 471mW
Pb-Free Reflow Profile (Note 6) . . . . . see TB493

Recommended Operating Conditions

Temperature Range (Full Range Industrial) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

4. Measured with no filtering, distance of 10" from source, intensity set to 55kV and 70mA current, 30s duration. Other exposure levels should be analyzed for Output Voltage drift effects. See "Applications Information" on page 16.
5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See tech brief TB379 for details.
6. Post-reflow drift for the ISL21007 devices will range from 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The design engineer must take this into account when considering the reference voltage after assembly.

Common Electrical Specifications (ISL21007-12, -20, -25, -30)

T_A = -40°C to +125°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
V_{OUT} Accuracy at T_A = +25°C	V_{OA}	ISL21007B	-0.5		+0.5	mV
		ISL21007C	-1.0		+1.0	mV
		ISL21007D	-2.0		+2.0	mV
Output Voltage Temperature Coefficient (Note 7)	TC V_{OUT}	ISL21007B			**3**	ppm/°C
		ISL21007C			**5**	ppm/°C
		ISL21007D			**10**	ppm/°C
Supply Current	I_{IN}			75	**150**	µA
Trim Range			**±2.0**	±2.5		%
Turn-On Settling Time	t_R	V_{OUT} = ±0.1%		120		µs
Ripple Rejection		f = 10kHz		60		dB
Output Voltage Noise	e_N	0.1Hz ≤ f ≤ 10Hz		4.5		μV_{P-P}
Broadband Voltage Noise	V_N	10Hz ≤ f ≤ 1kHz		2.2		μV_{RMS}
Noise Density		f = 1kHz		60		$nV/\sqrt{Hz}$

Electrical Specifications (ISL21007-12, V_{OUT} = 1.250V)

V_{IN} = 3.0V, T_A = -40°C to +125°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Input Voltage Range	V_{IN}		**2.7**		**5.5**	V
Output Voltage	V_{OUT}			1.250		V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	2.7V ≤ V_{IN} ≤ 5.5V		100	**700**	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 7mA		10	**100**	µV/mA
		Sinking: -7mA ≤ I_{OUT} ≤ 0mA		20	**150**	µV/mA
Short-Circuit Current	I_{SC}	T_A = +25°C, V_{OUT} tied to GND		40		mA
Thermal Hysteresis (Note 8)	$\Delta V_{OUT}/\Delta T_A$	ΔT_A = +165°C		50		ppm
Long Term Stability (Note 9)	$\Delta V_{OUT}/\Delta t$	T_A = +25°C		100		ppm

Electrical Specifications (ISL21007-20, V_{OUT} = 2.048V)

V_{IN} = 3.0V, T_A = -40°C to +125°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Input Voltage Range	V_{IN}		**2.7**		**5.5**	V
Output Voltage	V_{OUT}			2.048		V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	2.7V ≤ V_{IN} ≤ 5.5V		50	**200**	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 7mA		10	**100**	µV/mA
		Sinking: -7mA ≤ I_{OUT} ≤ 0mA		20	**150**	µV/mA
Short-Circuit Current	I_{SC}	T_A = +25°C, V_{OUT} tied to GND		50		mA
Thermal Hysteresis (Note 8)	$\Delta V_{OUT}/\Delta T_A$	ΔT_A = +165°C		50		ppm
Long Term Stability (Note 9)	$\Delta V_{OUT}/\Delta t$	T_A = +25°C		75		ppm

Electrical Specifications (ISL21007-25, V_{OUT} = 2.500V)

V_{IN} = 3.0V, T_A = -40°C to +125°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Input Voltage Range	V_{IN}		**2.7**		**5.5**	V
Output Voltage	V_{OUT}			2.500		V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	2.7V ≤ V_{IN} ≤ 5.5V		50	**200**	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 5mA		10	**100**	µV/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA		20	**150**	µV/mA
Short-Circuit Current	I_{SC}	T_A = +25°C, V_{OUT} tied to GND		50		mA
Thermal Hysteresis (Note 8)	$\Delta V_{OUT}/\Delta T_A$	ΔT_A = +165°C		50		ppm
Long Term Stability (Note 9)	$\Delta V_{OUT}/\Delta t$	T_A = +25°C		50		ppm

Electrical Specifications (ISL21007-30, V_{OUT} = 3.000V)

V_{IN} = 5.0V, T_A = -40°C to +125°C, unless otherwise specified.
Boldface limits apply over the operating temperature range, -40°C to +125°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Input Voltage Range	V_{IN}		**3.2**		**5.5**	V
Output Voltage	V_{OUT}			3.000		V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3.2V ≤ V_{IN} ≤ 5.5V		50	**200**	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 7mA		10	**100**	µV/mA
		Sinking: -7mA ≤ I_{OUT} ≤ 0mA		20	**150**	µV/mA
Short-Circuit Current	I_{SC}	T_A = +25°C, V_{OUT} tied to GND		50		mA
Thermal Hysteresis (Note 8)	$\Delta V_{OUT}/\Delta T_A$	ΔT_A = +165°C		50		ppm
Long Term Stability (Note 9)	$\Delta V_{OUT}/\Delta t$	T_A = +25°C		50		ppm

NOTES:

7. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -40°C to +125°C = +165°C.
8. Thermal Hysteresis is the change of V_{OUT} measured at T_A = +25°C after temperature cycling over a specified range, ΔT_A. V_{OUT} is read initially at T_A = +25°C for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at +25°C. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For ΔT_A = +165°C, the device under test is cycled from +25°C to +125°C to -40°C to +25°C.
9. Long term drift is logarithmic in nature and diminishes over time. Drift after the first 1000 hours will be approximately 10ppm/√(1kHrs).
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Curves (ISL21007-12)

(R_{EXT} = 100kΩ)

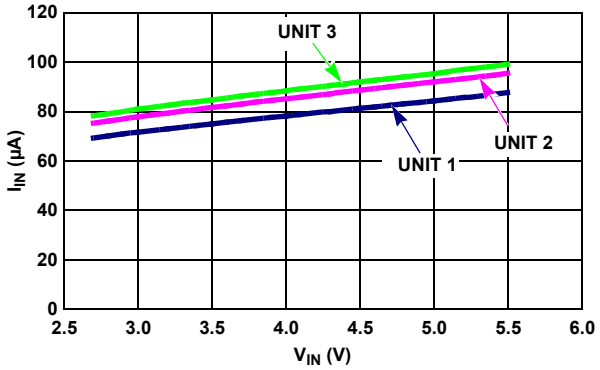


FIGURE 2. I_{IN} vs V_{IN} (3 UNITS)

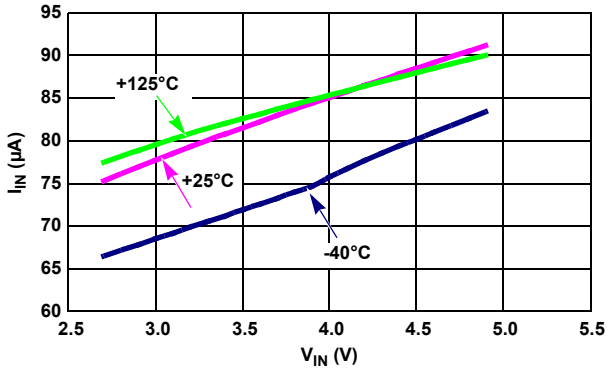


FIGURE 3. I_{IN} vs V_{IN} OVER TEMPERATURE

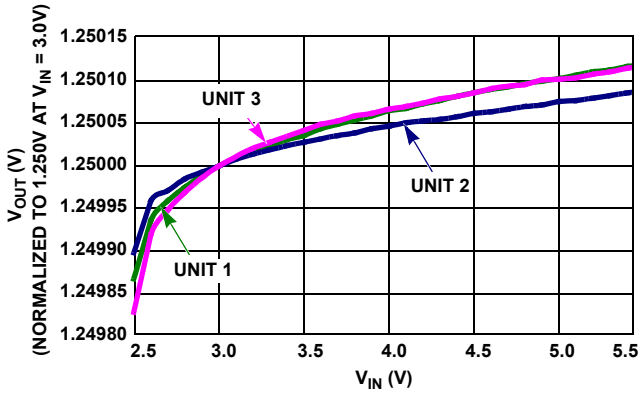


FIGURE 4. LINE REGULATION (3 UNITS)

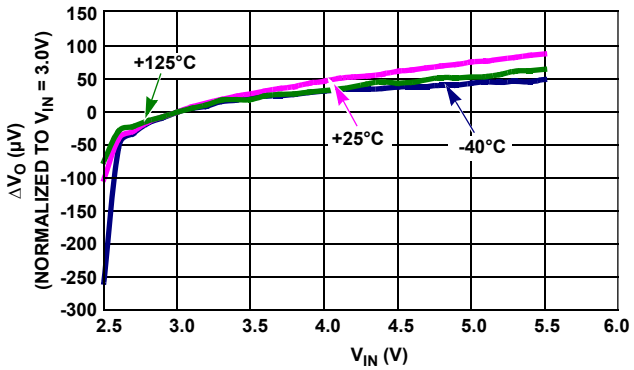


FIGURE 5. LINE REGULATION OVER TEMPERATURE

Typical Performance Curves (ISL21007-12) (R_{EXT} = 100kΩ) (Continued)

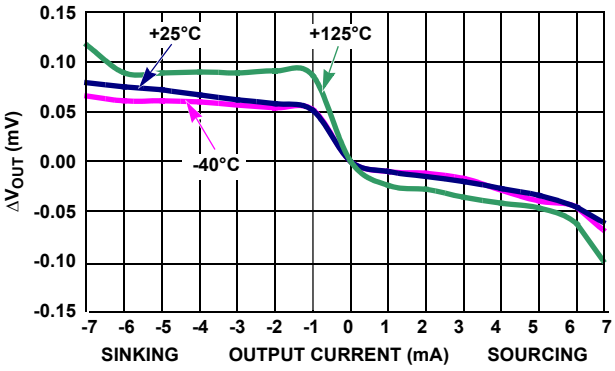


FIGURE 6. LOAD REGULATION OVER TEMPERATURE

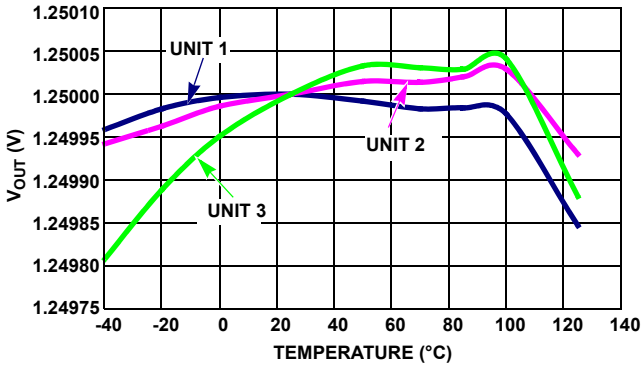


FIGURE 7. V_{OUT} vs TEMPERATURE (3 UNITS)

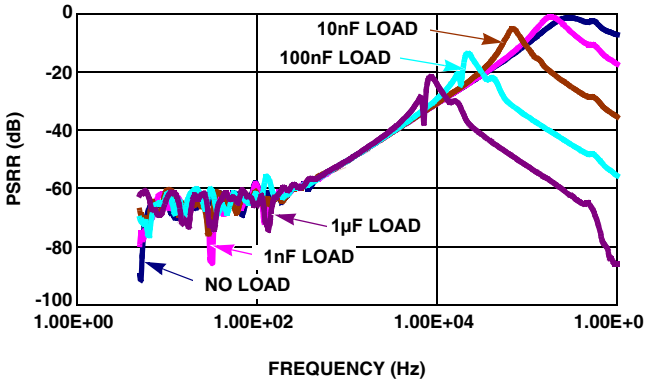


FIGURE 8. PSRR vs CAPACITIVE LOADS

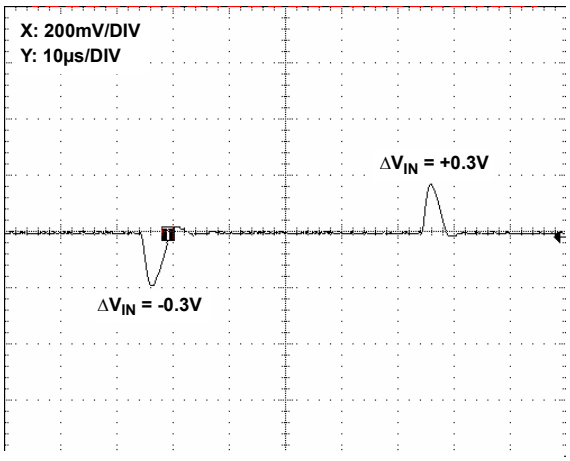


FIGURE 9. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

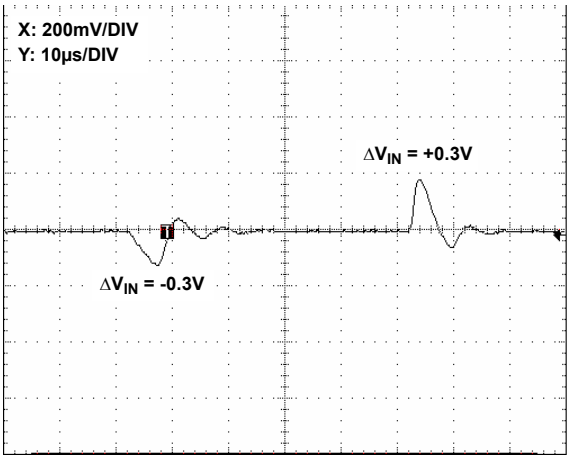


FIGURE 10. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

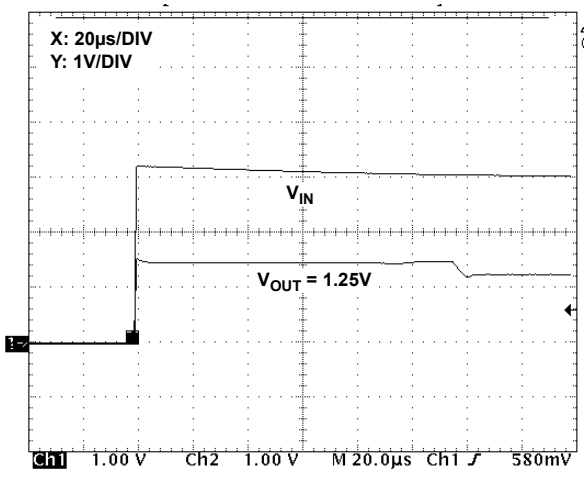


FIGURE 11. TURN-ON TIME

Typical Performance Curves (ISL21007-12) (R_{EXT} = 100kΩ) (Continued)

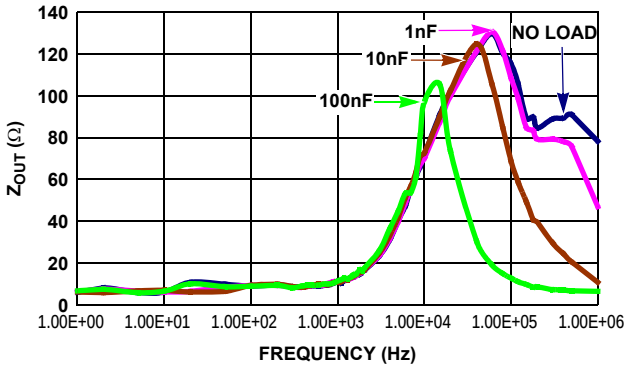


FIGURE 12. Z_{OUT} vs FREQUENCY

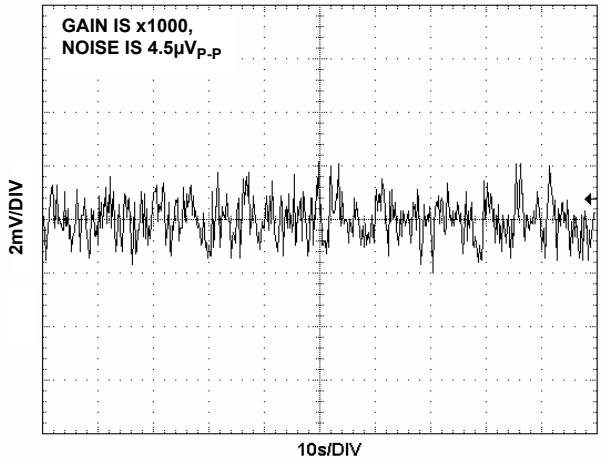


FIGURE 13. V_{OUT} NOISE, 0.1Hz TO 10Hz

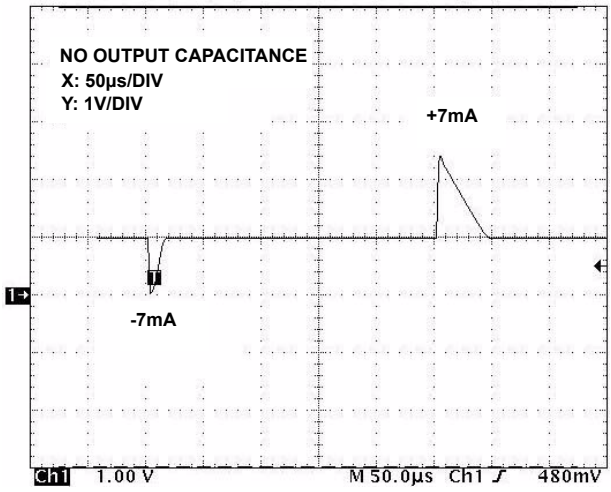


FIGURE 14. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21007-20) (R_{EXT} = 100kΩ)

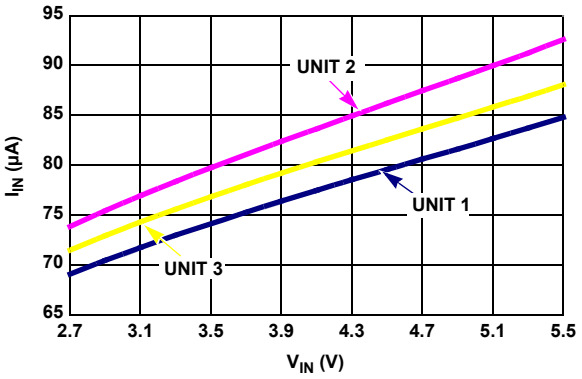


FIGURE 15. I_{IN} vs V_{IN} (3 UNITS)

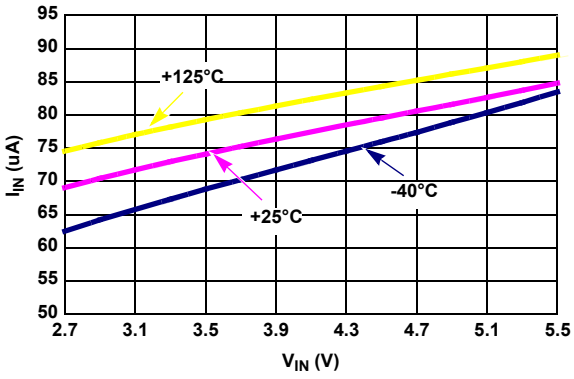


FIGURE 16. I_{IN} vs V_{IN} OVER TEMPERATURE

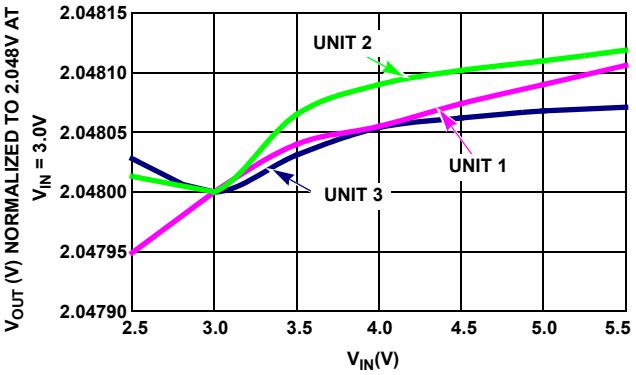


FIGURE 17. LINE REGULATION (3 UNITS)

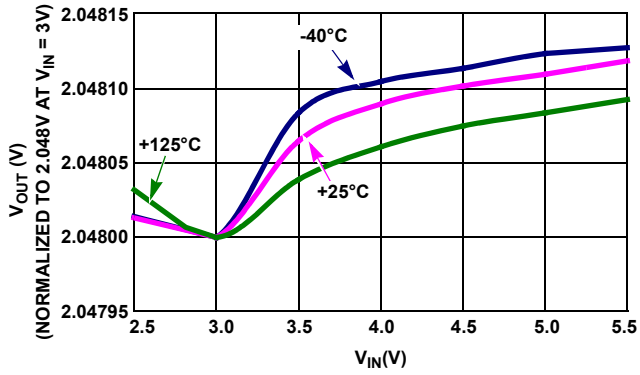


FIGURE 18. LINE REGULATION OVER TEMPERATURE

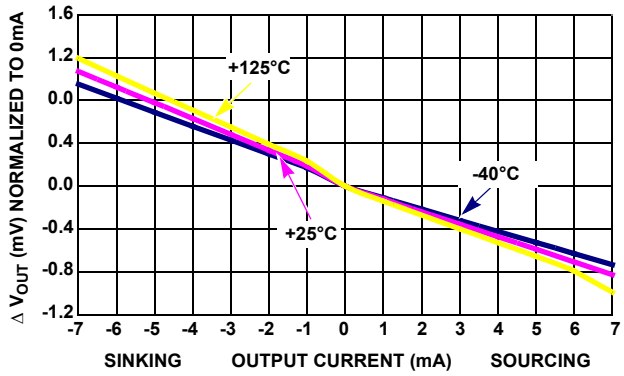


FIGURE 19. LOAD REGULATION OVER TEMPERATURE

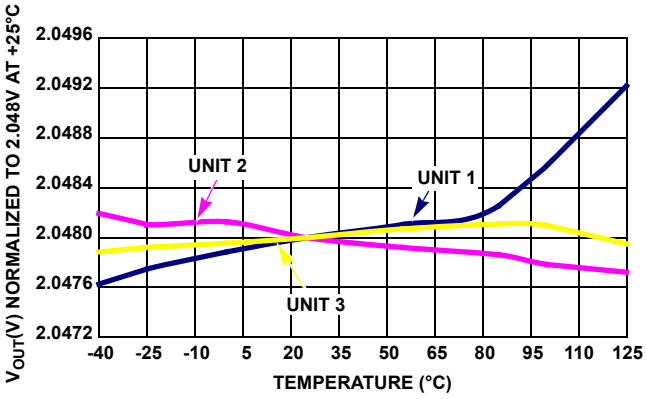


FIGURE 20. V_{OUT} vs TEMPERATURE (3 UNITS)

Typical Performance Curves (ISL21007-20) (R_{EXT} = 100kΩ) (Continued)

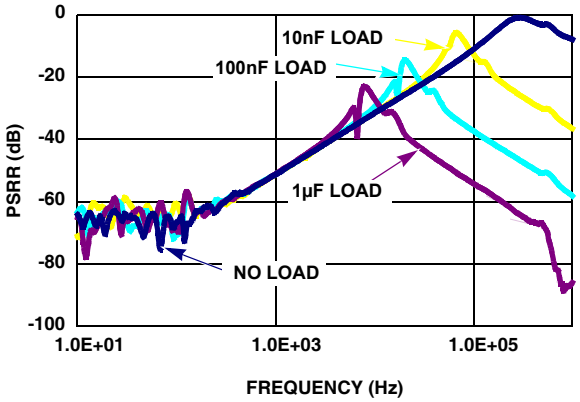


FIGURE 21. PSRR vs CAPACITIVE LOADS

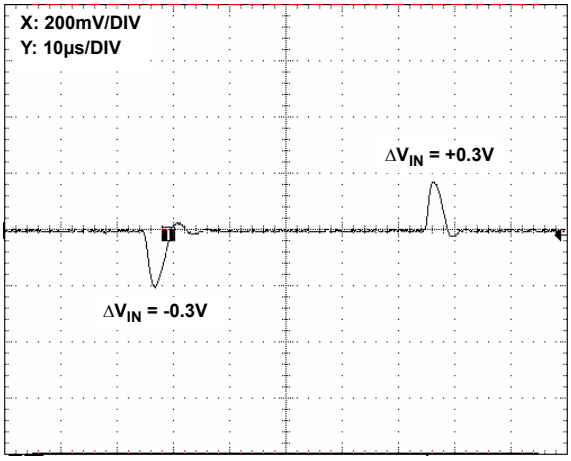


FIGURE 22. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

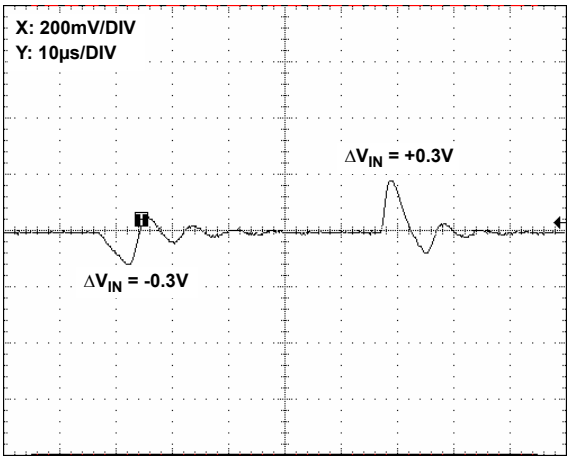


FIGURE 23. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

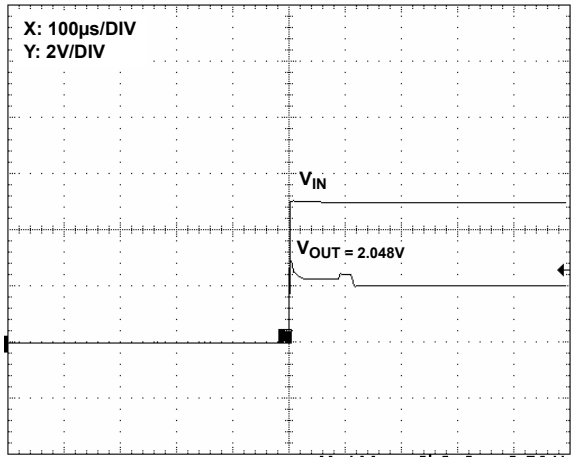


FIGURE 24. TURN-ON TIME

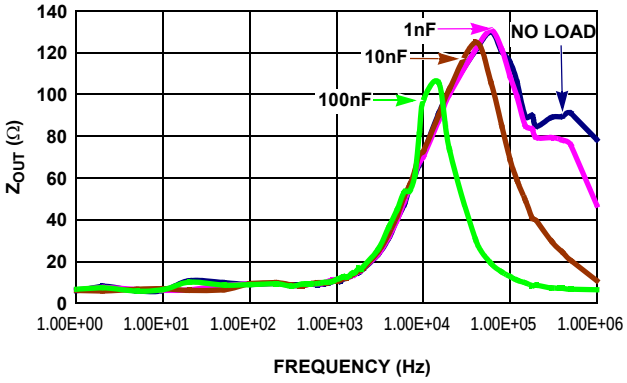


FIGURE 25. Z_{OUT} VS FREQUENCY

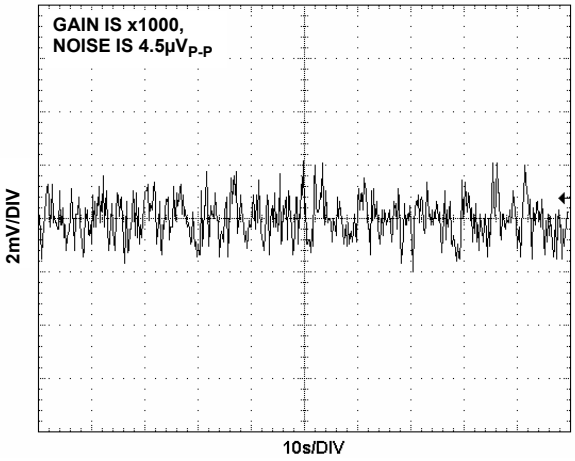


FIGURE 26. V_{OUT} NOISE, 0.1Hz TO 10Hz

Typical Performance Curves (ISL21007-20) (R_{EXT} = 100kΩ) (Continued)

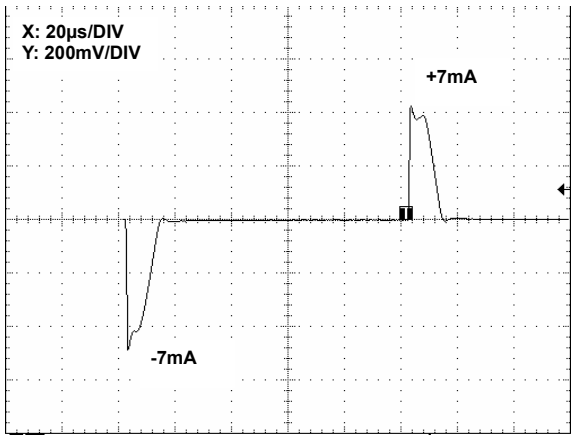


FIGURE 27. LOAD TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

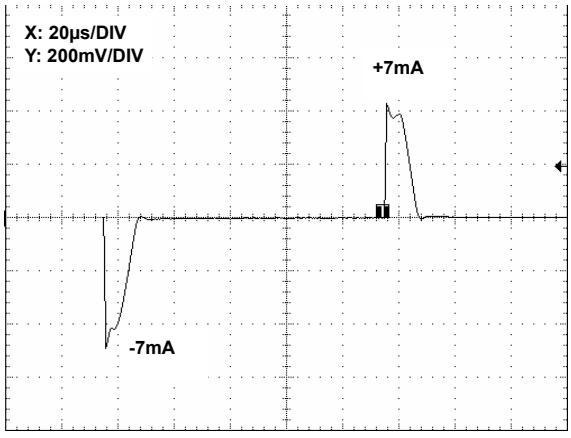


FIGURE 28. LOAD TRANSIENT RESPONSE, NO CAPACITIVE LOAD

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ)

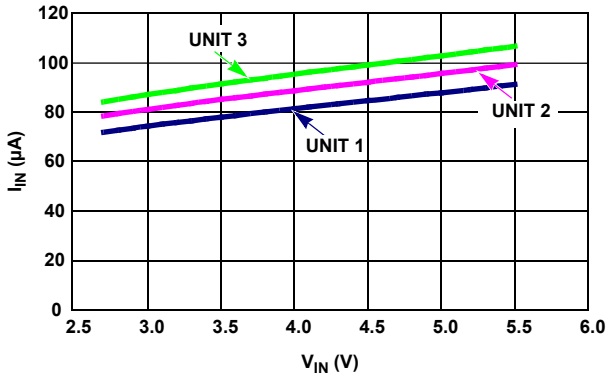


FIGURE 29. I_{IN} vs V_{IN} (3 UNITS)

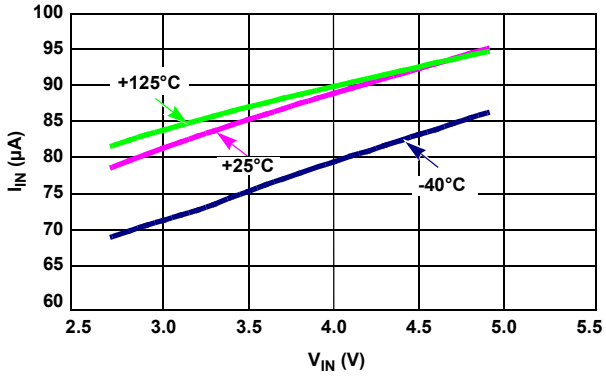


FIGURE 30. I_{IN} vs V_{IN} OVER TEMPERATURE

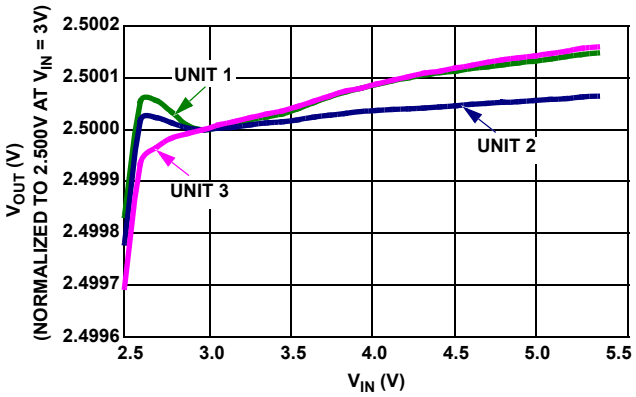


FIGURE 31. LINE REGULATION (3 UNITS)

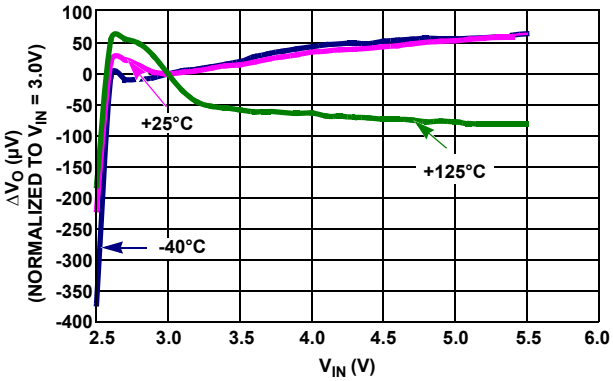


FIGURE 32. LINE REGULATION OVER TEMPERATURE

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ) (Continued)

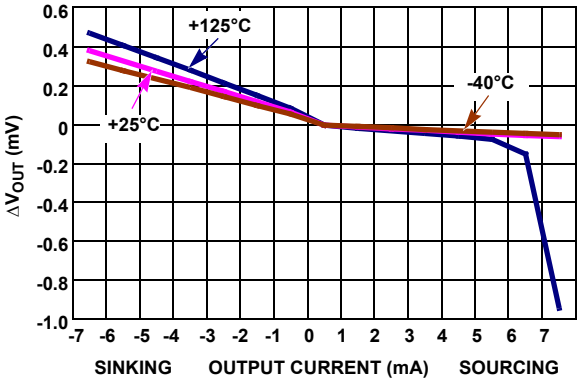


FIGURE 33. LOAD REGULATION OVER TEMPERATURE

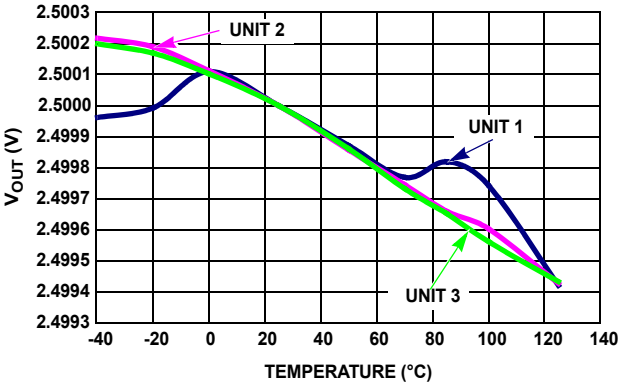


FIGURE 34. V_{OUT} vs TEMPERATURE (3 UNITS)

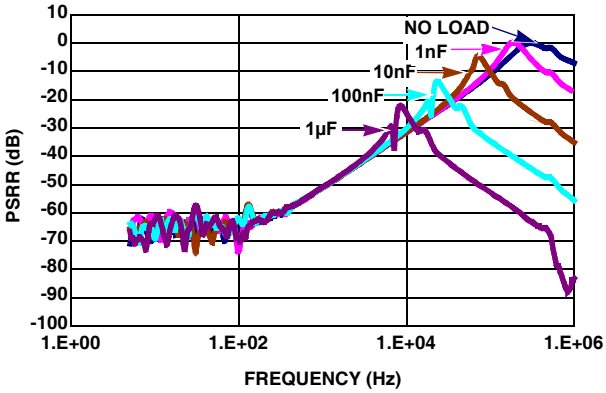


FIGURE 35. PSRR vs CAPACITIVE LOADS

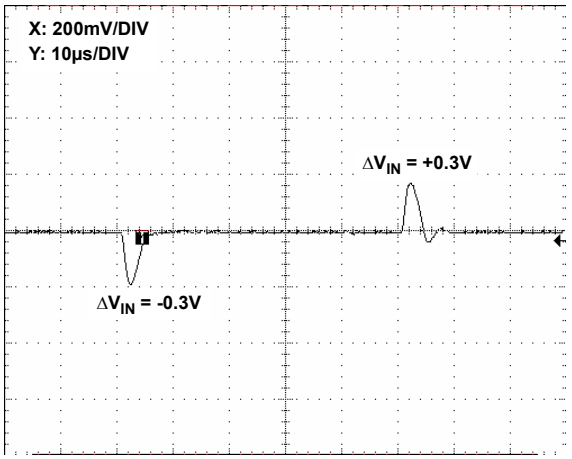


FIGURE 36. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

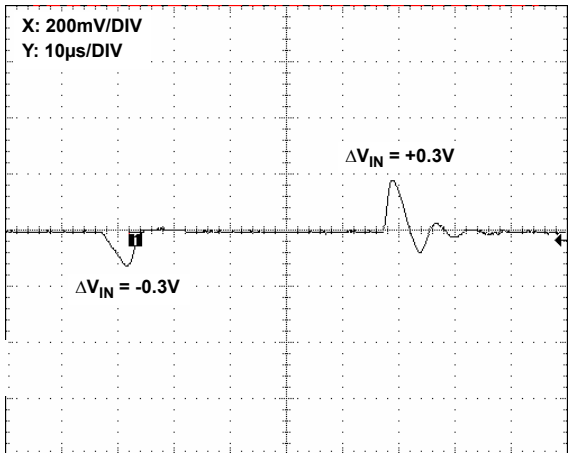


FIGURE 37. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

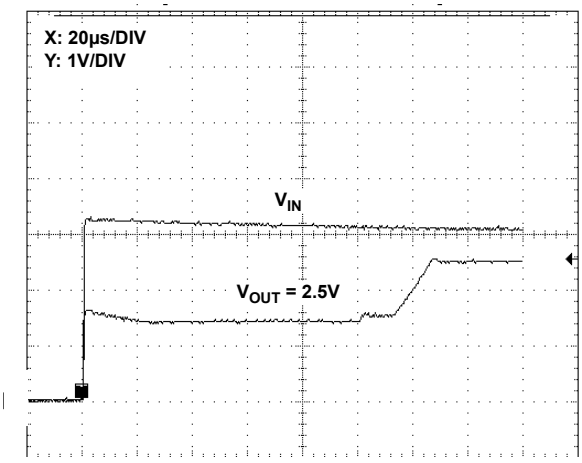


FIGURE 38. TURN-ON TIME

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ) (Continued)

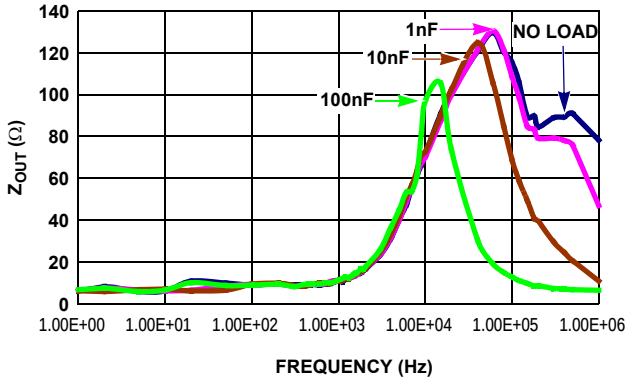


FIGURE 39. Z_{OUT} vs FREQUENCY

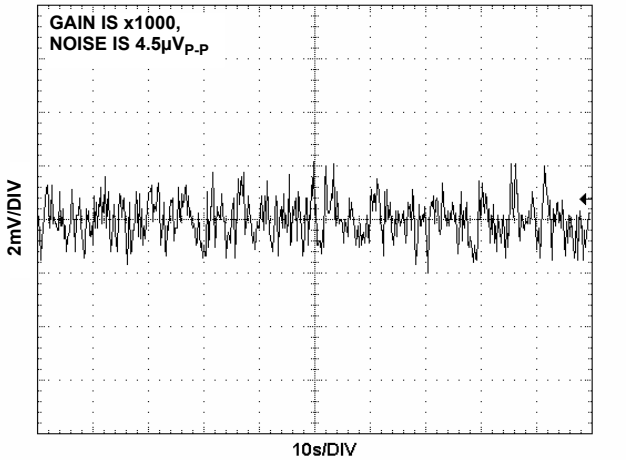


FIGURE 40. V_{OUT} NOISE, 0.1Hz TO 10Hz

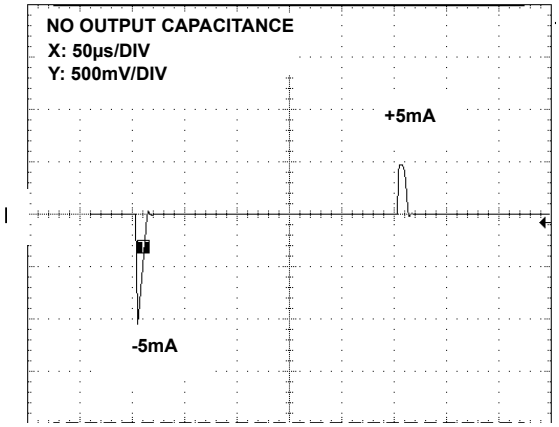


FIGURE 41. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21007-30) (R_{EXT} = 100kΩ)

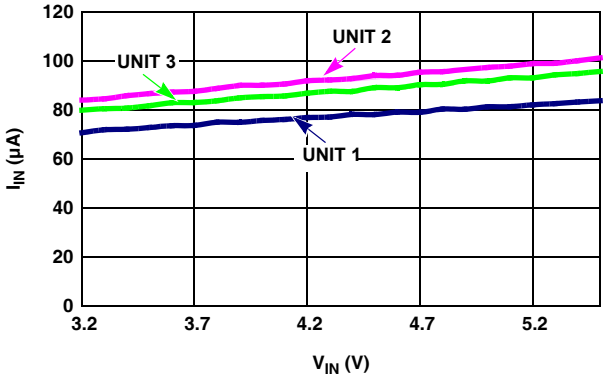


FIGURE 42. I_{IN} vs V_{IN} (3 UNITS)

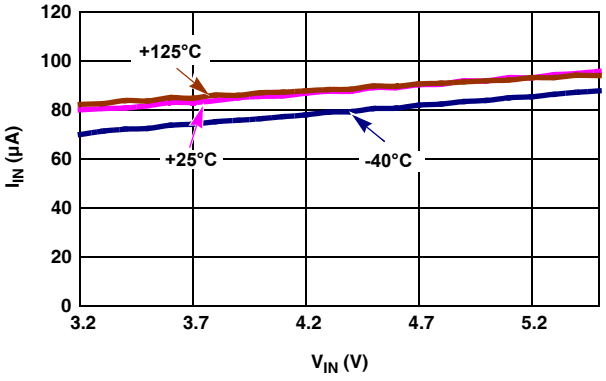


FIGURE 43. I_{IN} vs V_{IN} OVER TEMPERATURE

Typical Performance Curves (ISL21007-30) (R_{EXT} = 100kΩ) (Continued)

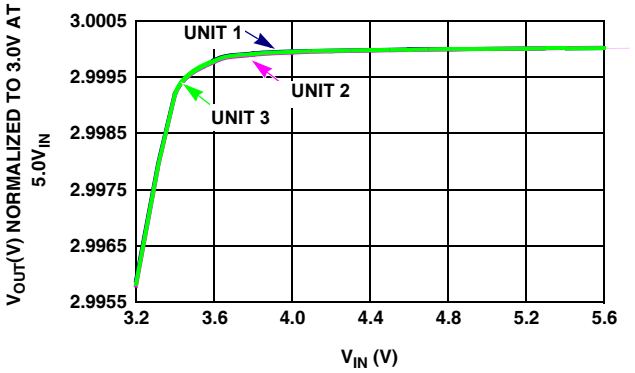


FIGURE 44. LINE REGULATION (3 UNITS)

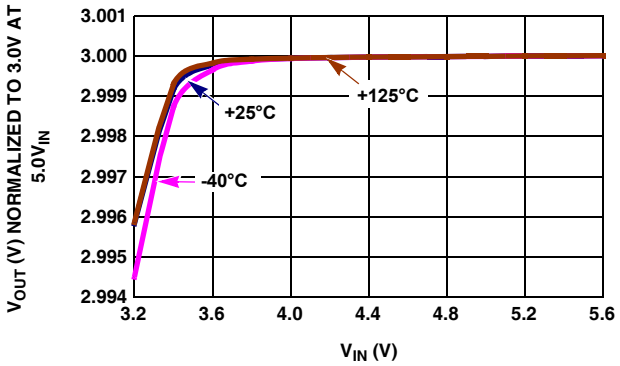


FIGURE 45. LINE REGULATION OVER TEMPERATURE

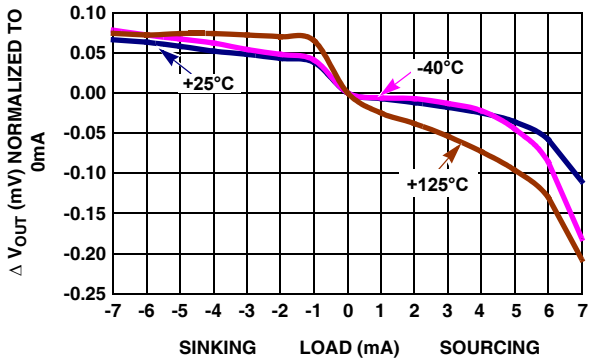


FIGURE 46. LOAD REGULATION OVER TEMPERATURE

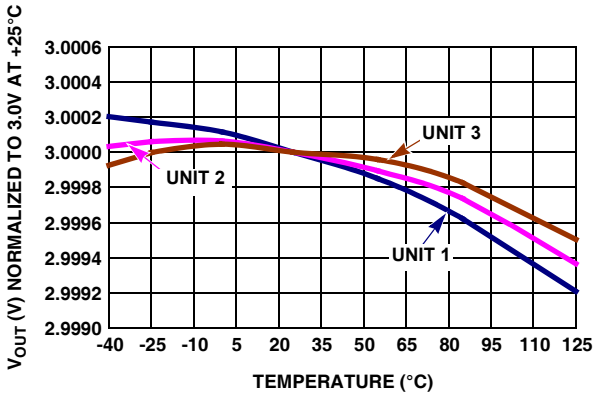


FIGURE 47. V_{OUT} vs TEMPERATURE (3 UNITS)

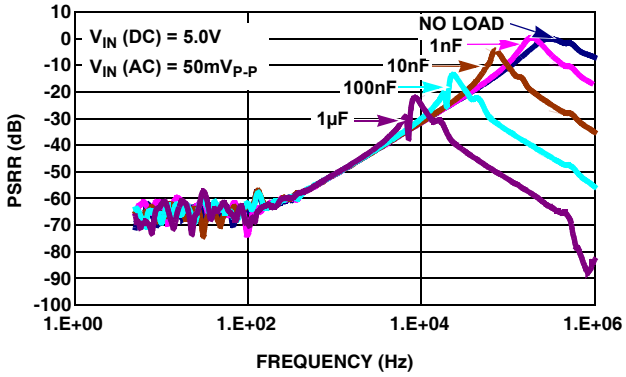


FIGURE 48. PSRR vs CAPACITIVE LOADS

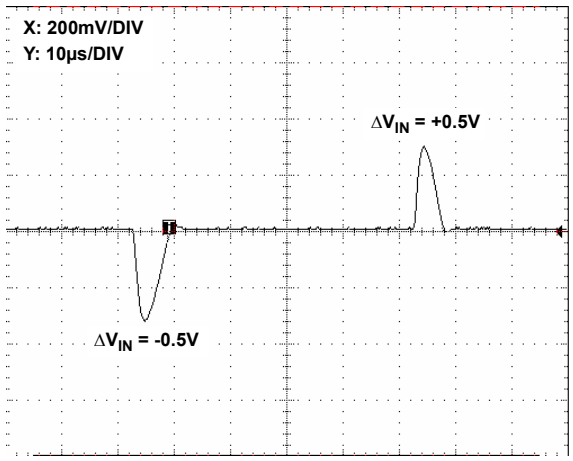


FIGURE 49. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

Typical Performance Curves (ISL21007-30) (R_{EXT} = 100kΩ) (Continued)

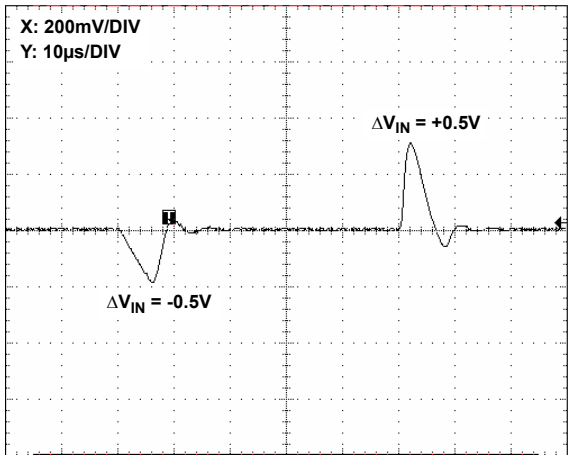


FIGURE 50. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

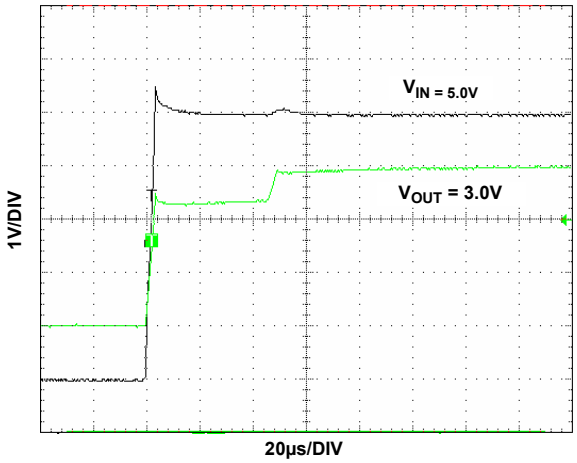


FIGURE 51. TURN-ON TIME

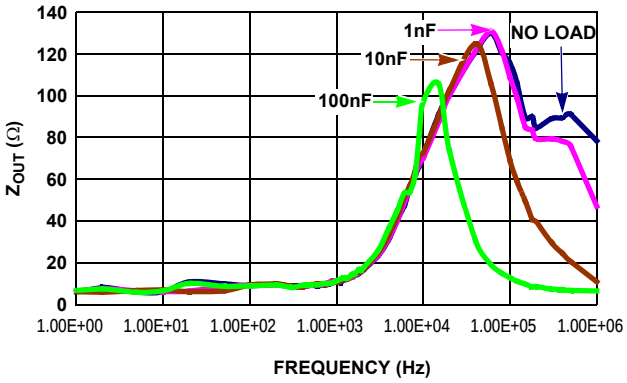


FIGURE 52. Z_{OUT} vs FREQUENCY

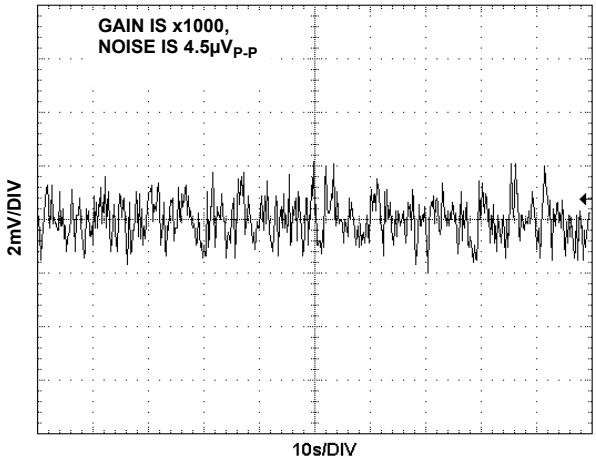


FIGURE 53. V_{OUT} NOISE, 0.1Hz TO 10Hz

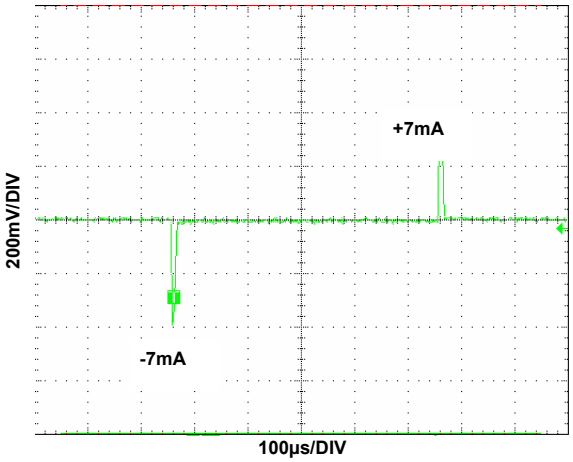


FIGURE 54. LOAD TRANSIENT RESPONSE

Applications Information

FGA Technology

The ISL21007 voltage reference uses floating gate technology to create references with very low drift and supply current. Essentially, the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics that are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Micropower Operation

The ISL21007 consumes extremely low supply current due to the proprietary FGA technology. Low noise performance is achieved using optimized biasing techniques. Supply current is typically 75µA and noise is $4.5\mu V_{P-P}$ benefitting precision, low noise portable applications such as handheld meters and instruments.

Data Converters in particular can use the ISL21007 as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise.

Handling and Board Mounting

FGA references provide excellent initial accuracy and low temperature drift at the expense of very little power drain. There are some precautions to take to ensure this accuracy is not compromised. Excessive heat during solder reflow can cause excessive initial accuracy drift, so the recommended +260°C max temperature profile should not be exceeded. Expect up to 1mV drift from the solder reflow process.

FGA references are susceptible to excessive X-radiation like that used in PC board manufacturing. Initial accuracy can change 10mV or more under extreme radiation. If an assembled board needs to be X-rayed, care should be taken to shield the FGA reference device.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

FGA references provide high accuracy and low temperature drift but some PC board assembly precautions are necessary. Normal Output voltage shifts of 100µV to 1mV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

Post-assembly X-ray inspection may also lead to permanent changes in device output voltage and should be minimized or avoided. If X-ray inspection is required, it is advisable to monitor the reference output voltage to verify excessive shift has not occurred. If large amounts of shift are observed, it is best to add an X-ray shield consisting of thin zinc (300µm) sheeting to allow clear imaging, yet block X-ray energy that affects the FGA reference.

Special Applications Considerations

In addition to post-assembly examination, there are also other X-ray sources that may affect the FGA reference long term accuracy. Airport screening machines contain X-rays and will have a cumulative effect on the voltage reference output accuracy. Carry-on luggage screening uses low level X-rays and is not a major source of output voltage shift, however, if a product is expected to pass through that type of screening over 100 times, it may need to consider shielding with copper or aluminum. Checked luggage X-rays are higher intensity and can cause output voltage shift in much fewer passes, thus devices expected to go through those machines should definitely consider shielding. Note that just two layers of 1/2 ounce copper planes will reduce the received dose by over 90%. The leadframe for the device which is on the bottom also provides similar shielding.

If a device is expected to pass through luggage X-ray machines numerous times, it is advised to mount a 2-layer (minimum) PC board on the top, along with a ground plane underneath, which will effectively shield it from 50 to 100 passes through the machine. Because these machines vary in X-ray dose delivered, it is difficult to produce an accurate maximum pass recommendation.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 4.5µV_{P-P}. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately 40µV_{P-P} with no capacitance on the output. This noise measurement is made with a 2 decade bandpass filter made of a 1-pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10 times the center frequency. Load capacitance up to 1000pF can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21007 is not designed to drive heavily capacitive loads, so for load capacitances above 0.001µF, the noise reduction network shown in Figure 55 on page 17 is recommended. This network reduces noise significantly over the full bandwidth. Noise is reduced to less than 20µV_{P-P} from 1Hz to 1MHz using this network with a 0.01µF capacitor and a 2kΩ resistor in series with a 10µF capacitor. Also, transient response is improved with higher value output capacitor. The 0.01µF value can be increased for better load transient response with little sacrifice in output stability.

Turn-On Time

The ISL21007 devices have low supply current and thus the time to bias up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically 120µs. This is shown in Figure 10. Circuit design must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, (V_{HIGH} – V_{LOW}), and divide by the temperature extremes of measurement (T_{HIGH} – T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted up or down by 2.5% by placing a potentiometer from V_{OUT} to ground, and connecting the wiper to the TRIM pin. The TRIM input is high impedance, so no series resistance is needed. The resistor in the potentiometer should be a low tempco (<50ppm/°C) and the resulting voltage divider should have very low tempco <5ppm/°C. A digital potentiometer such as the ISL95810 provides a low tempco resistance and excellent resistor and tempco matching for trim applications. See Figure 59 and TB473 for further information.

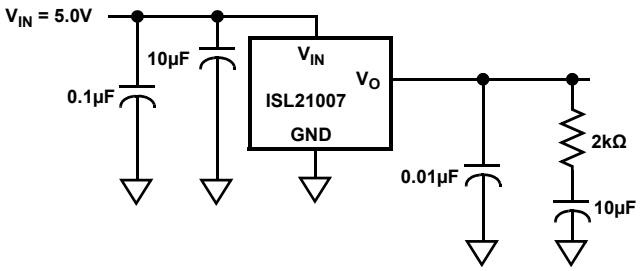


FIGURE 55. HANDLING HIGH LOAD CAPACITANCE

Typical Application Circuits

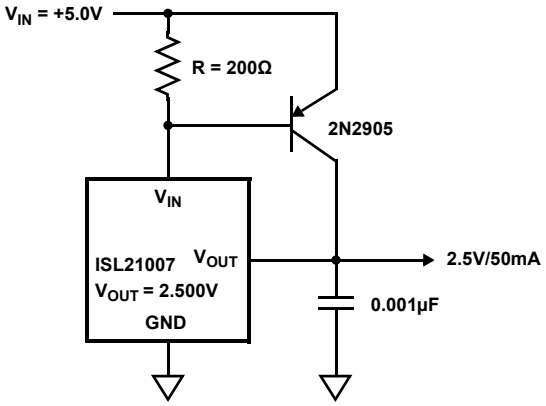


FIGURE 56. PRECISION 2.500V 50mA REFERENCE

Typical Application Circuits (Continued)

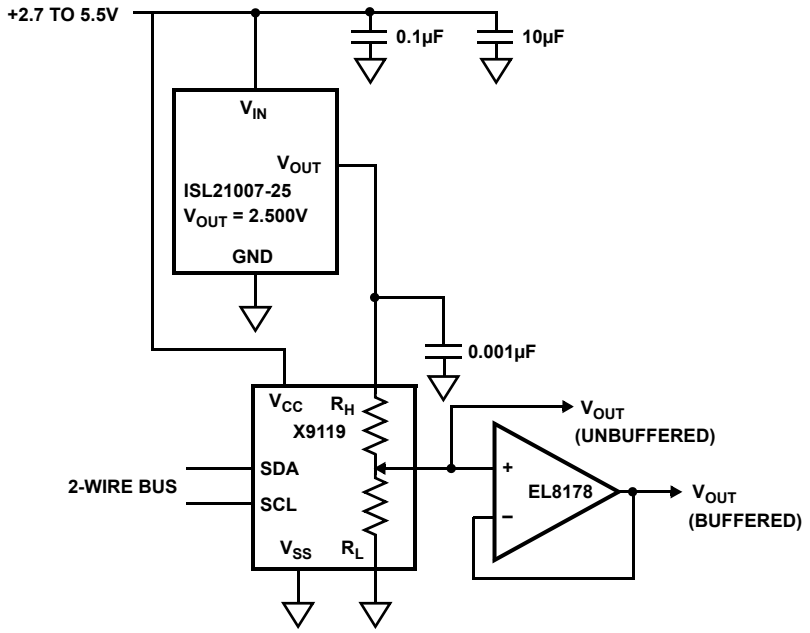


FIGURE 57. 2.500V FULL SCALE LOW-DRIFT, LOW NOISE, 10-BIT ADJUSTABLE VOLTAGE SOURCE

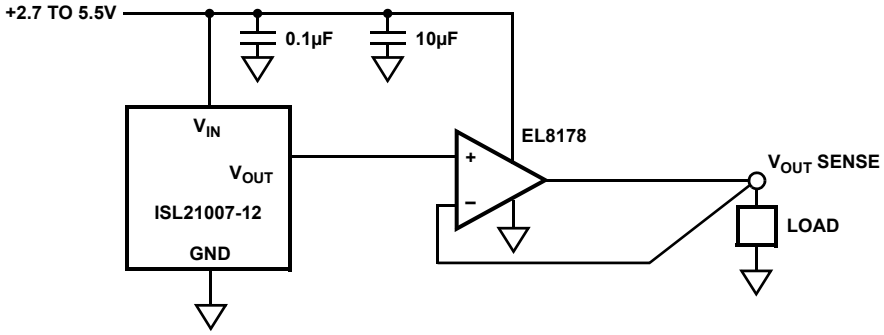


FIGURE 58. KELVIN SENSED LOAD

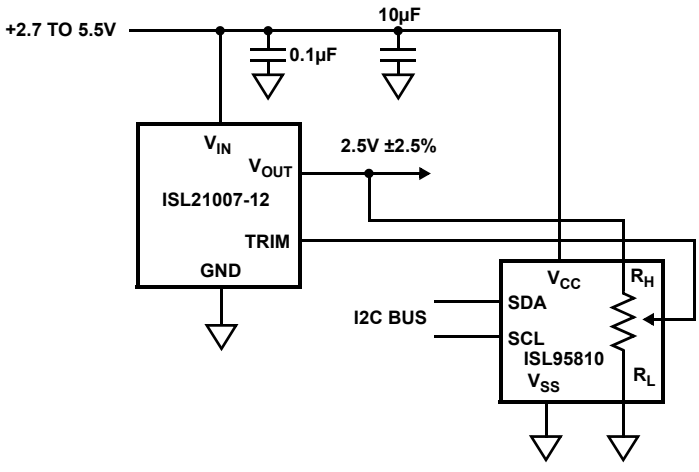


FIGURE 59. OUTPUT ADJUSTMENT USING THE TRIM PIN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jun 9, 2017	FN6326.12	Applied new header/footer. Updated Table 1 on page 1. Updated Related Literature section. Updated Ordering information table. Updated Note 2. Updated About Intersil section.
Sept 2, 2015	FN6326.11	Added Rev History beginning with Revision 11. Added About Intersil verbiage. Removed Initial Accuracy from Features on page 1. Updated Available Options Table on page 1. Updated Ordering Information on page 2. Moved Pin Configuration from page 1 to page 3.

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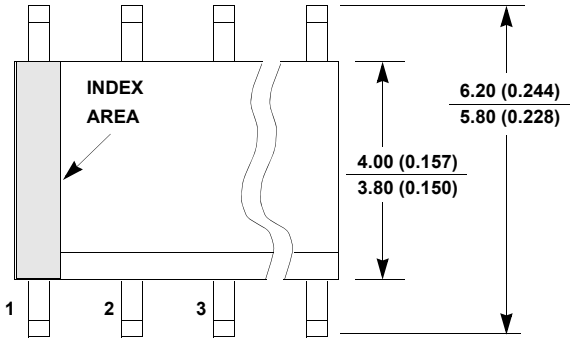
Package Outline Drawing

For the most recent package outline drawing, see M8.15.

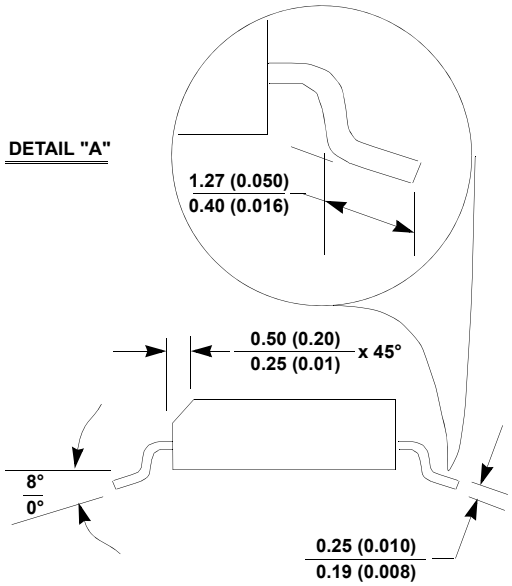
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

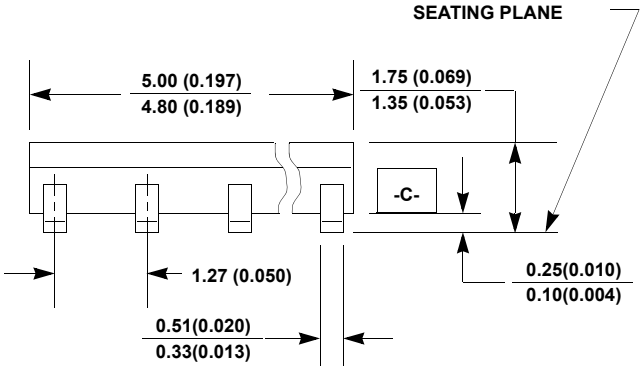
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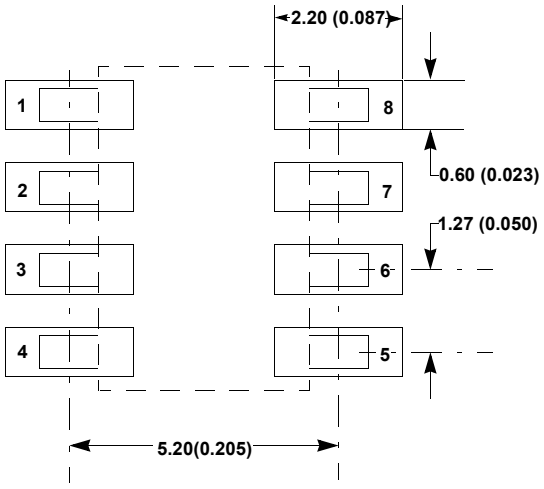
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).