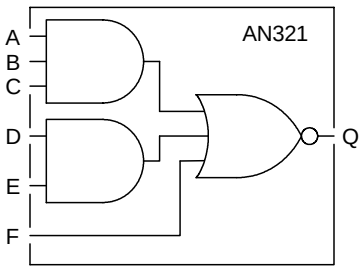
AN321 is an AND/NOR circuit providing the logical function Q = NOT (A.B.C+D.E+F).

Truth Table

A	B	C	D	E	F	Q
L	X	X	L	X	L	H
L	X	X	X	L	L	H
X	L	X	L	X	L	H
X	L	X	X	L	L	H
X	X	L	L	X	L	H
X	X	L	X	L	L	H
X	X	X	X	X	H	L
X	X	X	H	H	X	L
H	H	H	X	X	X	L



Capacitance

	Ci (pF)
A	0.062
B	0.062
C	0.068
D	0.053
E	0.058
F	0.047

Area

1.08 $mils^2$

Power

3.87 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.74	2.10	2.82	0.87	2.21	2.88
	tpdaf	0.51	1.42	1.87	0.50	1.37	1.81
Delay B to Q	tpdbr	0.70	2.05	2.77	0.82	2.16	2.86
	tpdbf	0.51	1.46	1.87	0.59	1.45	1.89
Delay C to Q	tpdcr	0.64	2.09	2.73	0.74	2.11	2.77
	tpdcf	0.46	1.42	1.82	0.66	1.51	1.94
Delay D to Q	tpddr	0.68	2.04	2.70	0.83	2.15	2.83
	tpddf	0.42	1.35	1.79	0.50	1.37	1.81
Delay E to Q	tpder	0.62	2.02	2.67	0.78	2.11	2.81
	tpdef	0.40	1.34	1.76	0.62	1.47	1.90
Delay F to Q	tpdfr	0.52	1.91	2.66	0.73	2.00	2.71
	tpdff	0.35	1.41	1.99	0.63	1.59	2.08
Output Slope A to Q	op_slar	1.66	5.78	7.95	1.73	5.85	7.85
	op_slaf	1.33	3.98	5.25	1.41	3.96	5.27
Output Slope B to Q	op_slbr	1.52	5.62	7.77	1.66	5.76	7.87
	op_slbf	1.33	3.97	5.18	1.47	4.01	5.28

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Output Slope C to Q	op_slcr	1.43	5.86	7.95	1.52	5.75	7.97
	op_slcf	1.31	3.97	5.18	1.57	4.06	5.32
Output Slope D to Q	op_sldr	1.62	5.82	7.81	1.77	5.87	7.86
	op_sldf	1.11	3.75	5.03	1.30	3.75	5.10
Output Slope E to Q	op_sler	1.56	5.77	8.07	1.73	5.80	8.02
	op_slef	1.08	3.73	5.03	1.46	3.86	5.10
Output Slope F to Q	op_slfr	1.58	5.85	7.98	1.85	5.83	7.85
	op_slff	1.02	3.90	5.40	1.32	4.00	5.47