TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1227AP

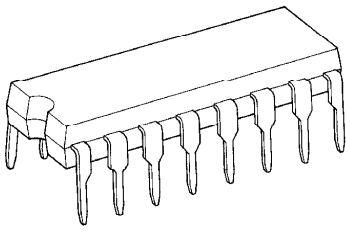
EDTV2 IDENTIFICATION CONTROL SIGNAL DETECTOR

The TA1227AP detects EDTV2 identification signals.
It detects the 27 bits on the 22H and 285H lines of each frame and outputs to the read bus. The methods of detection are following.

B1 to B5, and B24 NRZ signal :
Y signal level detection

B25 to B27 (4/7) fsc :
Y signal level detection at BPF output

B6 to B23 fsc phase modulation signal :
Converts the IQ demodulation signal of the main signal processing IC to a color difference signal and detects the level



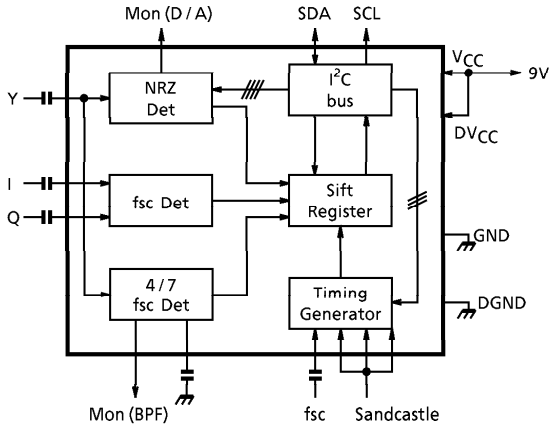
DIP16-P-300-2.54A

Weight : 1.11g (Typ.)

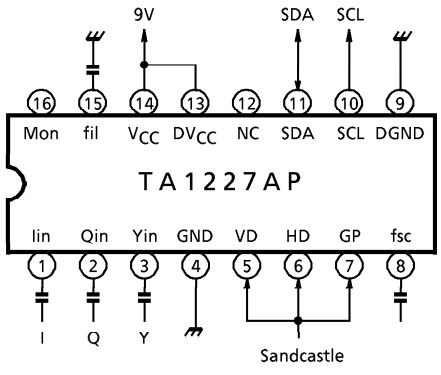
FEATURES

- I^2C bus-controllable
- Y and I, Q inputs
- Compatible with sandcastle pulse (VD, HD, and GP) input
- Auto adjustment of 4/7 fsc BPF f_0

BLOCK DIAGRAM



PIN ASSIGNMENT DIAGRAM

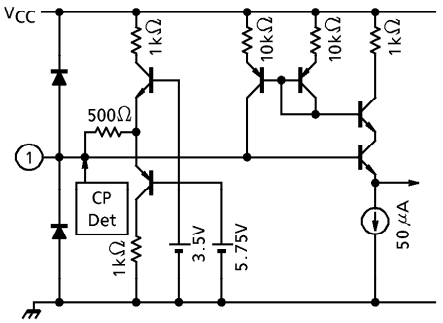
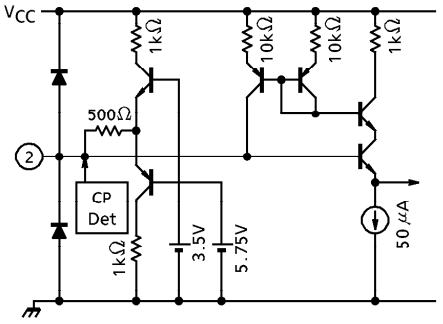
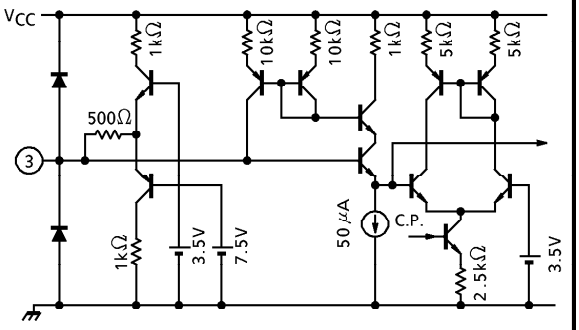
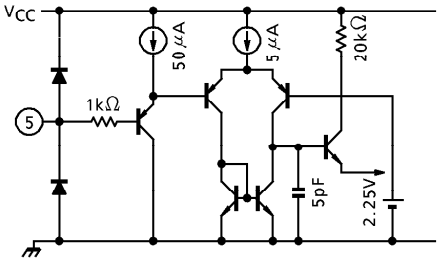


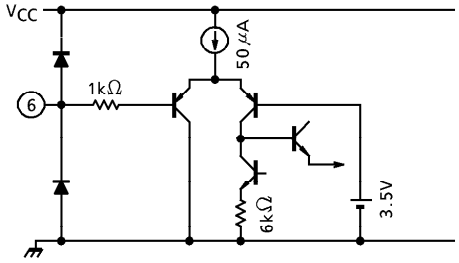
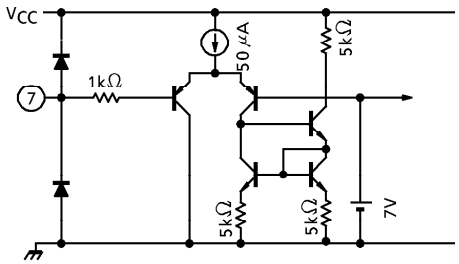
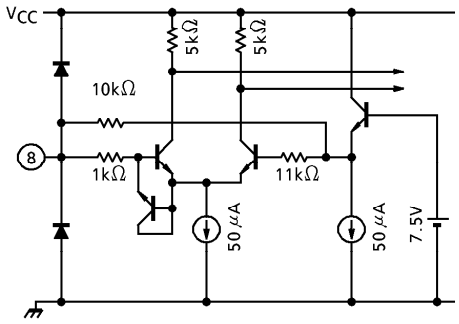
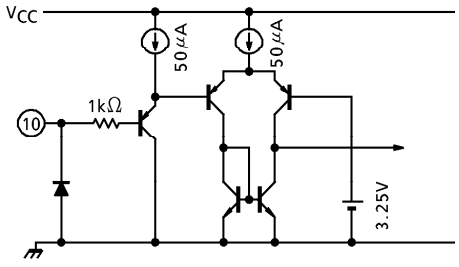
All capacitors are 0.01μF

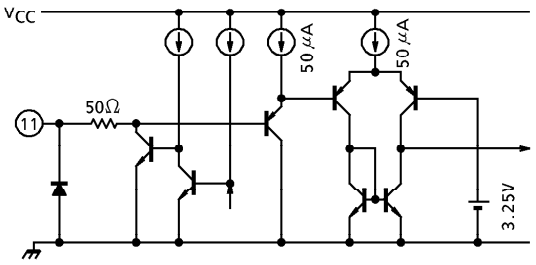
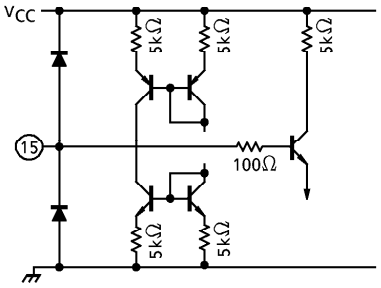
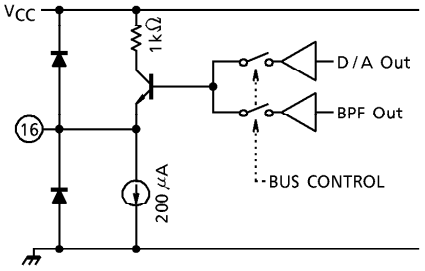
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TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	I input	I signal input terminal. Input the I signal to this terminal via a clamping capacitor (0.01μF recommended). The typical input level is 0.3V_{p-p}. This terminal is used to identify bits 6 to 23 of the identification signal. If no I signal is input, connect this terminal to the AC GND.	
2	Q input	Q signal input terminal. Input the Q signal to this terminal via a clamping capacitor (0.01μF recommended). The typical input level is 0.3V_{p-p}. This terminal is used to identify bits 6 to 23 of the identification signal. If no Q signal is input, connect this terminal to the AC GND.	
3	Y input	Y signal input terminal. Input the Y signal to this terminal via a clamping capacitor (0.01μF recommended). The typical input level is 1.0V_{p-p}. This terminal is used to identify bits 1 to 5 and 24 to 27 of the identification signal.	
4	GND	GND terminal for analog block	—
5	VD input	VD signal input terminal. Input a signal of positive polarity. The threshold level is 1.5V (typ.). The rising phase of the VD signal acts as the trigger to start the HD count and the 22H and 285H lines are identified. This terminal can also be used to input sandcastle pulses to which VD, HD, and GP are multiplexed.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
6	HD input	HD signal input terminal. Input a signal of positive polarity with a width that can accommodate GP. The threshold level is 3.5V (typ.). Note that VD is canceled if HD rises within 1μs of VD rising. This terminal can also be used to input sandcastle pulses to which VD, HD, and GP are multiplexed.	
7	GP input	Gate pulse input terminal. Input a signal of positive polarity. The threshold level is 7.0V (typ.). The read timing for each 27 bits is determined from the rising phase of the GP signal. Note that Y and I, Q inputs are clamped while GP is high. This terminal can also be used to input sandcastle pulses to which VD, HD, and GP are multiplexed.	
8	fsc input	Terminal for input of 3.58MHz continuous signal for the IC's internal reference clock. Input a signal locked to the color subcarrier of the video signal to be demodulated. The typical input level is $0.6V_{p\text{-}p}$.	
9	D.GND	GND pin for digital block	—
10	SCL	SCL input terminal for I^2C bus. The threshold level is 2.5V.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
11	SDA	SDA I/O terminal for I^2C bus. The threshold level is 2.5V. The current flowing through this terminal should not exceed 3.0mA.	
12	N.C.	This terminal is not connected and should be left open.	—
13	D.V_{CC}	Power supply pin for the digital block. Apply 9.0V (typ.).	—
14	V_{CC}	Power supply terminal for the analog block. Apply 9.0V (typ.).	—
15	f_0 adjustment	Terminal for connecting f_0 automatic adjustment filter of 4/7fsc BPF. The recommended capacitance is 0.01μF.	
16	Monitor output	Terminal for monitoring DAC output for NRZ-Compared level and 4/7fsc BPF output. Write Data D4 of the I^2C bus switches functions. When "0", the pin is set for DAC output : when "1", for monitoring BPF output.	

I²C BUS MAP

MODE	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
WRITE (Slave Address : BC HEX)	Timing (100)			Monitor (0)	NRZ-Det. level (1000)			
READ (Slave Address : BD HEX)	B1	B2	B3	B4	B5	B6	B7	B8
	B9	B10	B11	B12	B13	B14	B15	B16
	B17	B18	B19	B20	B21	B22	B23	B24
	B25	B26	B27	—	—	—	P.O.R.	Busy

( ) : Default values are shown in parenthesis.

I²C BUS CONTROL

	Timing [sc]	
	001	– 3
	010	– 2
	011	– 1
*	100	0
	101	1
	110	2
	111	3

	Monitor	
*	0	NRZ-Ref. level
	1	BPF

	NRZ-Det. level	[IRE]	[mV_{p-p}]
	0000	10	71.4
	0001	12	85.7
	0010	14	100.0
	0011	16	114.3
	0100	18	128.6
	0101	20	142.9
	0110	22	157.1
	0111	24	171.4
*	1000	26	185.7
	1001	28	200.0
	1010	30	214.3
	1011	32	228.6
	1100	34	242.9
	1101	36	257.1
	1110	38	271.4
	1111	40	285.7

1sc = 280ns (1 / fsc)

* Default value

Timing : The phase of the sampling pulse for reading each 27 bits of the identification signal can be adjusted by 7sc in 1sc steps. Don't use the data (000).

Monitor : Switches the signal output from pin 16.

NRZ-Det. level : Adjusts the NRZ detection level.
The det. level can be adjusted by 30IRE (= 214mV) in 2IRE steps.
There are errors within a tolerance ±3IRE (= ±21.4mV) against upper values.

P.O.R. (Power On Reset) : This bit shows that the bus data has been reset to the default value when the power is turned ON. After the POR, this bit is "1" for the first data output, then "0" for subsequent output. POR is applied at V_{CC} = 6V (typ.).

Busy : This bit is "1" while reading the 27 bits of the identification signal on the 22H and 285H lines, and "0" at other times.

I²C BUS TRANSMISSION AND RECEPTION METHODS

Slave address

A6	A5	A4	A3	A2	A1	A0	W / R
1	0	1	1	1	1	0	0 / 1

Data transmission format (Write mode)

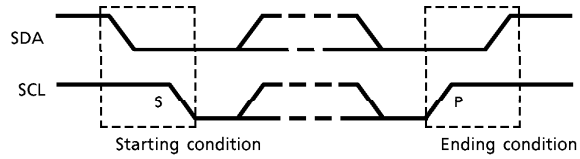
S	Slave address	0	A	Transmission data	A	P

7 bits (MSB) — 8 bits (MSB) — End condition

S : Starting condition

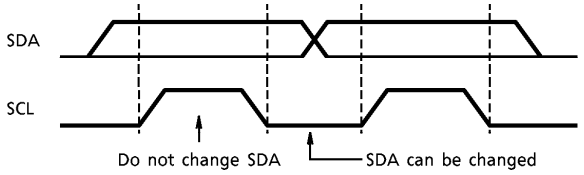
A : Acknowledgment

Starting and ending conditions

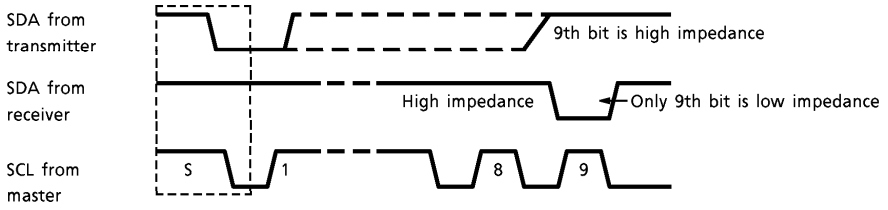


Purchase of TOSHIBA I²C components conveys a license under the philips I²C patent rights to use these components in an I²C system, provided that the system conforms to the I²C standard specification as defined by philips.

Bit transmission



Acknowledgment



Data reception format (Read mode)

S	Slave address	1	A	Received data	A		A	Received data	$\overline{A}$	P

7 bits (MSB) — 8 bits (MSB)

When receiving data, the master transmitter changes to a receiver immediately after the first acknowledgment, while the slave receiver changes into the transmitter.
The master always creates the end condition.
Detailed specifications conform to the PHILIPS I²C Specification.

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	14.0	V
Power Dissipation	P_D	1380 (Note)	mW
Operating Temperature	T_{opr}	−20~65	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 11.2mW for each increase of 1°C.

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 9V, D.V_{CC} = 9V, and Ta = 25°C unless otherwise specified)

PIN No.	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
13	D.V_{CC}	D.V_{CC}	8.1	9.0	9.9	V	—
14	V_{CC}	V_{CC}	8.1	9.0	9.9	V	—
1	I Input Amplitude	Iin	0.15	0.3	0.35	V_{p-p}	When ID signal demodulated
2	Q Input Amplitude	Qin	0.15	0.3	0.35	V_{p-p}	When ID signal demodulated
3	Y Input Amplitude	Yin	0.8	1.0	1.2	V_{p-p}	Amplitude between bottom of sync and 100% white
5	VD Input Voltage	VDin	1.8	—	9.0	V	Pulse high level
6	HD Input Voltage	HDin	3.8	—	9.0	V	Pulse high level
7	GP Input Voltage	GPin	7.3	—	9.0	V	Pulse high level
8	fsc Input Amplitude	fsc in	0.3	0.6	—	V_{p-p}	—
9	VD Rise Phase	t_{VD}	1085	—	1130	μs	The rising phase should be before the starting point in the 22 / 285H lines.
10	GP Rise Phase	t_{GP}	5.6	—	7.3	μs	After fall in H.sync (While adjusting from −3sc to +3sc)
11	GP Width	W_{GP}	1.0	—	—	μs	—

* HD must be input with a line blanking interval such that its width accommodates GP.

ELECTRICAL CHARACTERISTICS (V_{CC} = 9.0V, D.V_{CC} = 9.0V and Ta = 25°C unless otherwise specified)

DC CHARACTERISTICS

Terminal voltages

PIN No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	REMARKS
1	I Input	V1	—	3.80	4.25	4.70	V	Pin 7 : greater than 7V
2	Q Input	V2	—	3.80	4.25	4.70	V	Pin 7 : greater than 7V
3	Y Input	V3	—	3.80	4.25	4.70	V	Pin 7 : greater than 7V
4	GND	—	—	—	0	—	V	—
8	fsc Input	V8	—	6.20	6.75	7.30	V	—
9	D.GND	—	—	—	0	—	V	—
13	D.V_{CC}	D.V_{CC}	—	—	9.0	—	V	—
14	V_{CC}	V_{CC}	—	—	9.0	—	V	—
15	f_0 Auto Adjustment	V15	—	1.0	1.5	2.0	V	—
16	Monitor Output	V16		3.1	3.6	4.1	V	D/A output

Current consumption

PIN No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT
13	D.V_{CC}	D.I_{CC}	—	23.0	30.0	37.0	mA
14	V_{CC}	I_{CC}	—	10.0	12.5	15.0	mA

AC CHARACTERISTICS

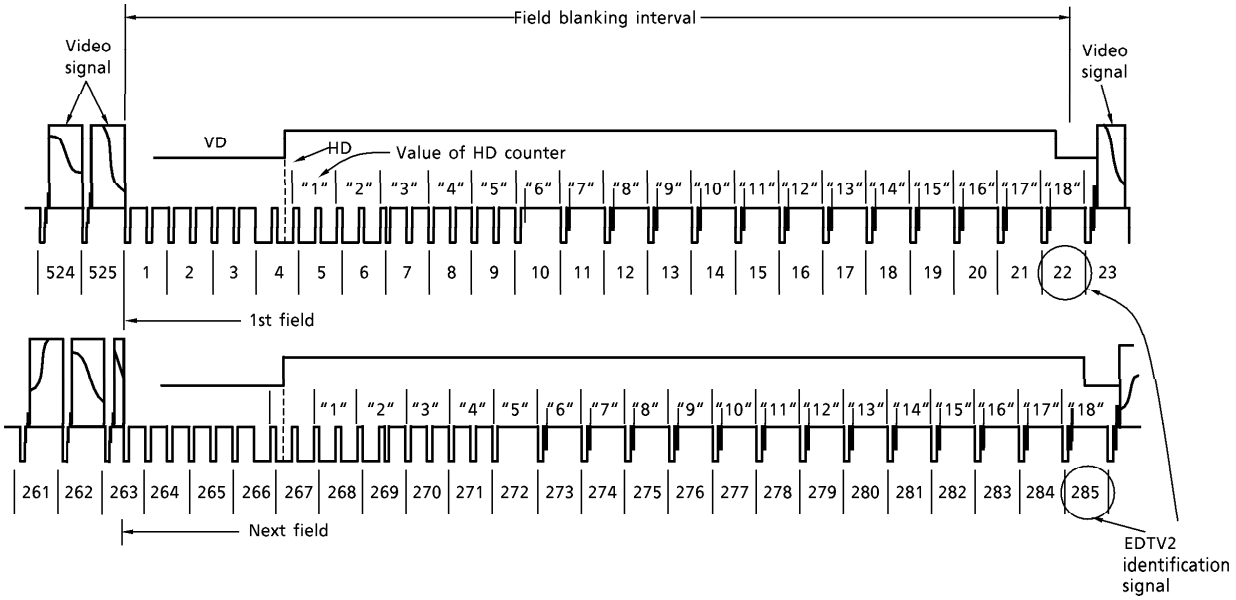
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	REMARKS
VD Threshold Level	V_{VDth}	—	1.3	1.5	1.7	V	Design value
HD Threshold Level	V_{HDth}	—	3.3	3.5	3.7	V	Design value
GP Threshold Level	V_{GPth}	—	6.8	7.0	7.2	V	Design value
NRZ Detection Errors	Δ_{NRZ}	—	−3	0	+3	IRE	Against the level set by bus
		—	−21.4	0	+21.4	mV	
4/7fsc Detection Level	V_{47fsc}	—	—	118	150	mV_{p-p}	Design value, f = 2.04545MHz
BPF Attenuation	G_1	—	20	—	—	dB	Design value, f = 1MHz
	$G_{3.08}$	—	20	25	—	dB	Design value, f = 3.08MHz
	$G_{3.58}$	—	30	35	—	dB	Design value, f = 3.579545MHz
	$G_{4.5}$	—	35	40	—	dB	Design value, f = 4.5MHz
BPF Group Delay	τ_{47fsc}	—	—	1.2	—	μs	Design value, f = 2.04545MHz
Sampling Start Phase (Note)	t_{SP}	—	2.79	3.07	3.35	μs	Design value, should be later than rise in GP.

(Note) Bus data : default

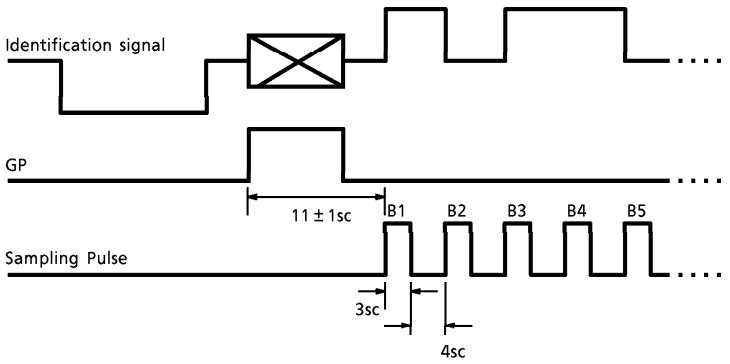
VD, HD, AND GP INPUT TIMING

In the TA1227AP, the rise in VD triggers the start of the HD count. A window is opened between the 17th and 18th fall in HD during which GP is sampled (see figure). The rise in the sampled GP is used as a reference for creating a sampling pulse for reading the bits of the EDTV2 identification signal. Therefore, it should be set so that VD rises during the 4H and 267H lines. The sampling pulse for the first bit rises 11sc after the rise in the reference gate pulse. The pulse width ratio is 3 : 4 (high : low). The sampling pulse phasing is under bus control (− 3sc to + 3cs).
The threshold levels of the respective pulses are : VD : 1.5V, HD : 3.5V, and GP : 7.0V. Note that, if HD rises within 1μs of a rise in VD, that VD is canceled.
The TA1227AP will accept the input of sandcastle pulses to which VD, HD, and GP are multiplexed.

HD, VD TIMINGS



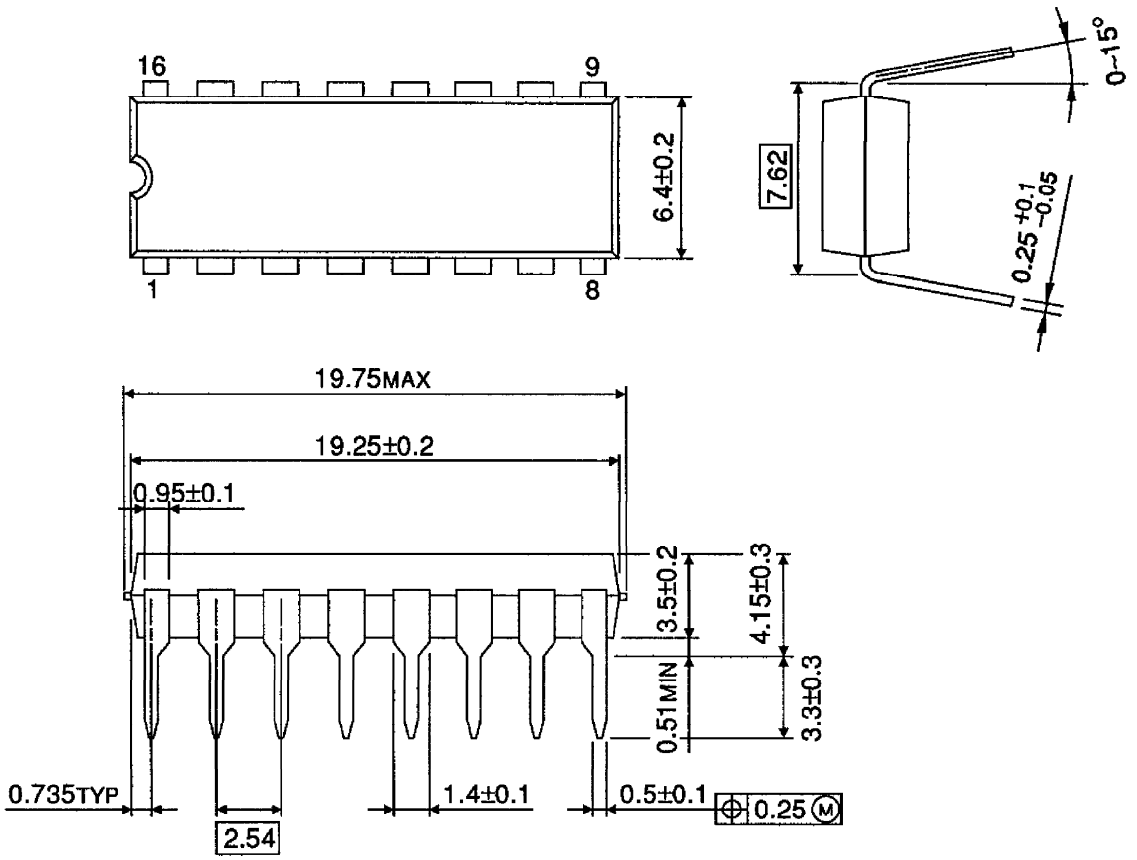
22 / 285H LINE



OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm



Weight : 1.00g (Typ.)