# SN74LV14A 六路施密特触发反相器

## 1 特性

- $V_{CC}$ 工作电压范围为 2V 至 5.5V
- 5V 时 $t_{pd}$ 最大值为 10ns
- $V_{CC}$ = 3.3V、$T_A$ = 25°C 时，
  $V_{OLP}$（输出接地反弹）典型值小于 0.8V
- $V_{CC}$ = 3.3V、$T_A$ = 25°C 时，
  $V_{OHV}$（输出 $V_{OH}$ 下冲）典型值大于 2.3V
- 所有端口上均支持以混合模式电压运行
- $I_{off}$ 支持局部断电模式运行
- 闩锁性能超过 250mA，
  符合 JESD 17 规范的要求

## 2 应用

- 网络交换机
- 可穿戴保健和健身设备
- PDA
- LCD 电视
- 电力基础设施

## 3 描述

这些六路施密特触发反相器需在 2V 至 5.5V $V_{CC}$ 下运行。

SN74LV14A 器件包含六个独立的反相器。这些器件执行布尔函数 $Y = \overline{A}$。

**封装信息**

| 器件型号 | 封装 (1) | 封装尺寸（标称值） |
|---|---|---|
| SN74LV14A | TVSOP (14) | 3.60mm × 4.40mm |
| | SOIC (14) | 8.65mm × 3.91mm |
| | SSOP (14) | 6.20mm × 5.30mm |
| | TSSOP (14) | 5.00mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

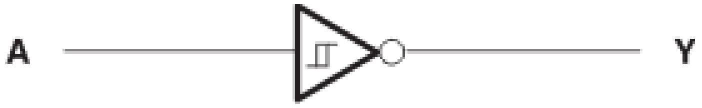

图 3-1. 简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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| • 通篇更新了表格、图和交叉参考的格式 | 1 |

| Changes from Revision J (September 1997) to Revision K (September 2014) | Page |
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| • 将文档更新为新的 TI 数据表格式 | 1 |
| • 删除了“订购信息”表 | 1 |
| • 添加了“应用” | 1 |
| • 添加了“器件信息”表 | 1 |
| • Added Pin Functions table | 3 |
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| • Added Power Supply Recommendations and Layout sections | 12 |

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# 5 Pin Configuration and Functions

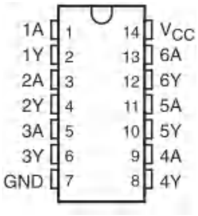

**图 5-1. SN74LV14A D, DB, DGV, NS OR PW Package Top View**

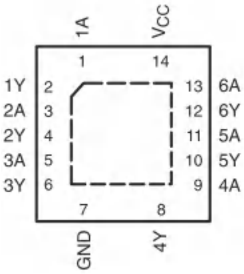

**图 5-2. SN74LV14A RGY Package Top View**

## Pin Functions

| PIN | | | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|
| NAME | SN74LV14A | | | |
| | D, DB, DGV, NS, PW | RGY | | |
| 1A | 1 | 1 | I | Input 1A |
| 1Y | 2 | 2 | O | Output 1Y |
| 2A | 3 | 3 | I | Input 2A |
| 2Y | 4 | 4 | O | Output 2Y |
| 3A | 5 | 5 | I | Input 3A |
| 3Y | 6 | 6 | O | Output 3Y |
| 4Y | 8 | 8 | O | Output 4Y |
| 4A | 9 | 9 | I | Input 4A |
| 5Y | 10 | 10 | O | Output 5Y |
| 5A | 11 | 11 | I | Input 5A |
| 6Y | 12 | 12 | O | Output 6Y |
| 6A | 13 | 13 | I | Input 6A |
| GND | 7 | 7 | — | Ground Pin |
| NC | — | — | — | No Connection |
| $V_{CC}$ | 14 | 14 | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *节 6.1* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *节 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |
| | | Machine Model | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN74LV14A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV14A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D | DB | DGV | NS | PW | RGY | |
| | | 14 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 94.9 | 107.4 | 130.4 | 91.4 | 122.6 | 57.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.3 | 59.9 | 53.4 | 49.0 | 51.3 | 70.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.2 | 54.7 | 63.5 | 50.2 | 64.4 | 33.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.7 | 21.0 | 7.3 | 15.3 | 6.8 | 3.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.9 | 51.2 | 62.8 | 49.8 | 63.8 | 33.7 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | – | – | – | 14.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | SN74LV14A –40°C to 85°C | | | SN74LV14A –40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ | Positive-going threshold | | 2.5 V | | | 1.75 | | | 1.75 | V |
| | | | 3.3 V | | | 2.31 | | | 2.31 | |
| | | | 5 V | | | 3.5 | | | 3.5 | |
| $V_{T-}$ | Negative-going threshold | | 2.5 V | 0.75 | | | 0.75 | | | V |
| | | | 3.3 V | 0.99 | | | 0.99 | | | |
| | | | 5 V | 1.5 | | | 1.5 | | | |
| $\Delta V_T$ ($V_{T+}$ – $V_{T-}$) | Hysteresis | | 2.5 V | 0.25 | | | 0.25 | | | V |
| | | | 3.3 V | 0.33 | | | 0.33 | | | |
| | | | 5 V | 0.5 | | | 0.5 | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –50 μA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | | |
| | | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 50 μA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | 0 to 5.5 V | | | ±1 | | | ±1 | μA |
| $I_{CC}$ | Static supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | μA |
| $I_{off}$ | Input/Output Power-Off Leakage Current | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | | 5 | μA |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2.3 | | | 2.3 | | pF |
| | | | 5 V | | 2.3 | | | 2.3 | | |

## 6.6 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV14A –40°C to 85°C | | SN74LV14A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 10.2(1) | 19.7(1) | 1 | 22 | 1 | 23 | ns |
| | | | $C_L$ = 50 pF | | 13.3 | 24 | 1 | 27 | 1 | 28 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.7 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV14A –40°C to 85°C | | SN74LV14A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 7.3(1) | 12.8(1) | 1 | 15 | 1 | 16 | ns |
| | | | $C_L$ = 50 pF | | 9.6 | 16.3 | 1 | 18.5 | 1 | 19.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV14A –40°C to 85°C | | SN74LV14A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 5.1(1) | 8.6(1) | 1 | 10 | 1 | 11 | ns |
| | | | $C_L$ = 50 pF | | 6.7 | 10.6 | 1 | 12 | 1 | 13 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.9 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| | | SN74LV14A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic | | 0.2 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic | | –0.1 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic | | 3.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 6.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF f = 10 MHz | 3.3 V | 8.8 | pF |
| | | | 5 V | 9.6 | |

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## 6.11 Typical Characteristics

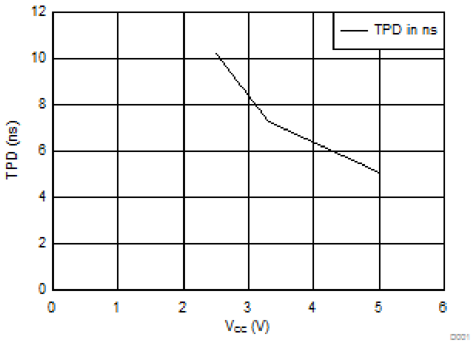

图 6-1. TPD vs $V_{CC}$

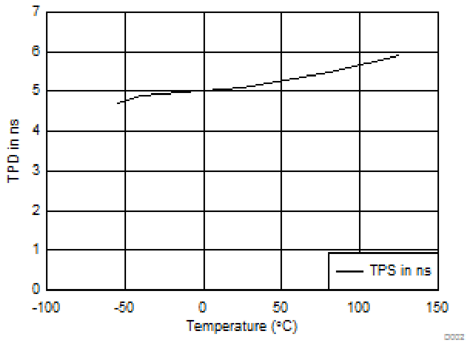

图 6-2. TPD vs Temperature

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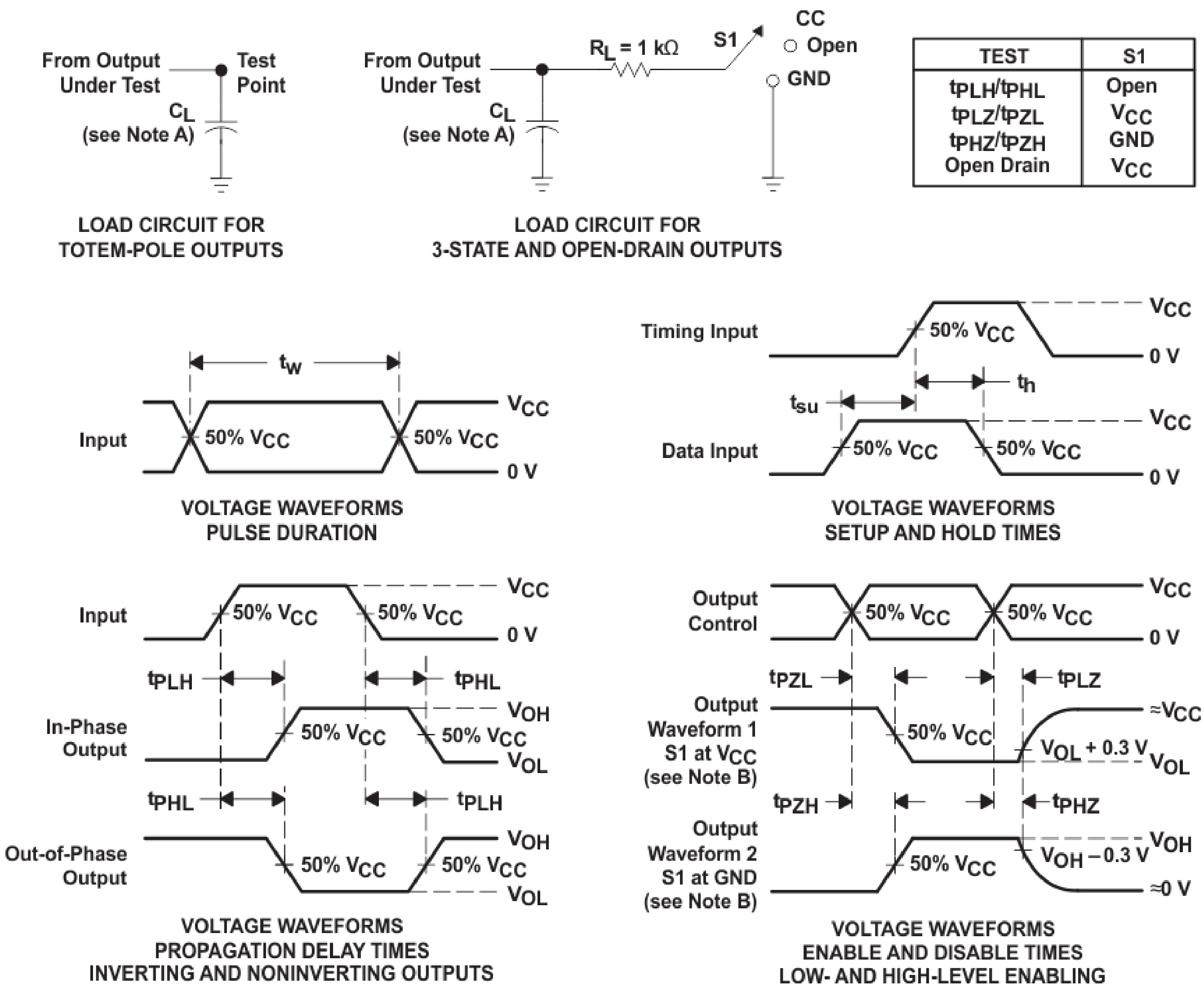
# 7 Parameter Measurement Information

## 7.1



A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR $\leqslant$ 1 MHz, $Z_O = 50\ \Omega$, $t_r \leqslant 3$ ns, $t_f \leqslant 3$ ns.

D. The outputs are measured one at a time, with one input transition per measurement.

E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.

H. All parameters and waveforms are not applicable to all devices.

**图 7-1. Load Circuit and Voltage Waveforms**

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# 8 Detailed Description

## 8.1 Overview

These hex Schmitt-trigger inverters are designed for 2 V to 5.5 V $V_{CC}$ operation.

The SN74LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

These devices are fully specified for partial-power-down application using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.2 Functional Block Diagram

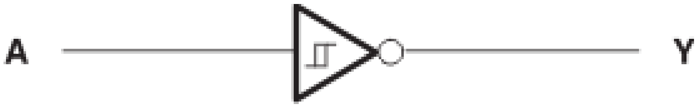

图 8-1. Logic Diagram, Each Inverter (Positive Logic)

## 8.3 Feature Description

- Wide operating voltage range
  - Operates From 2 V to 5.5 V
- Allows up or down voltage translation
  - Inputs and outputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V
- Schmitt-trigger inputs allow for slow or noisy inputs

## 8.4 Device Functional Modes

表 8-1. Function Table (Each Inverter)

| INPUT(1) A | OUTPUT(2) Y |
|---|---|
| H | L |
| L | H |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

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## 9 Application and Implementation

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**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 9.1 Application Information

Schmitt triggers should be used anytime you need to translate a sign wave into a square wave as shown in 图 9-1. They may also be used where a slow or noisy input needs to be sped up or cleaned up as shown in 图 9-2.

### 9.2 Typical Application

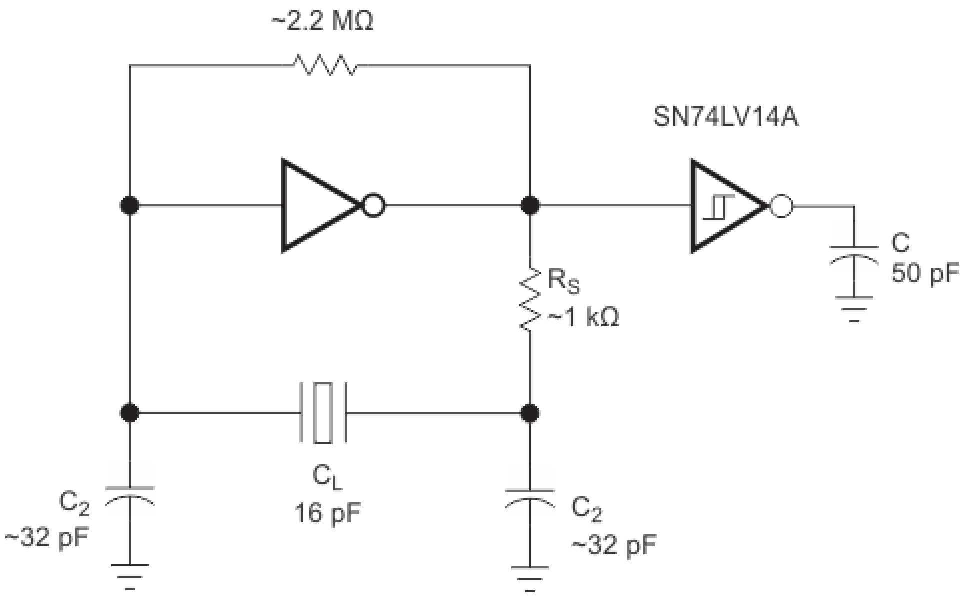

图 9-1. Oscillator Application Schematic

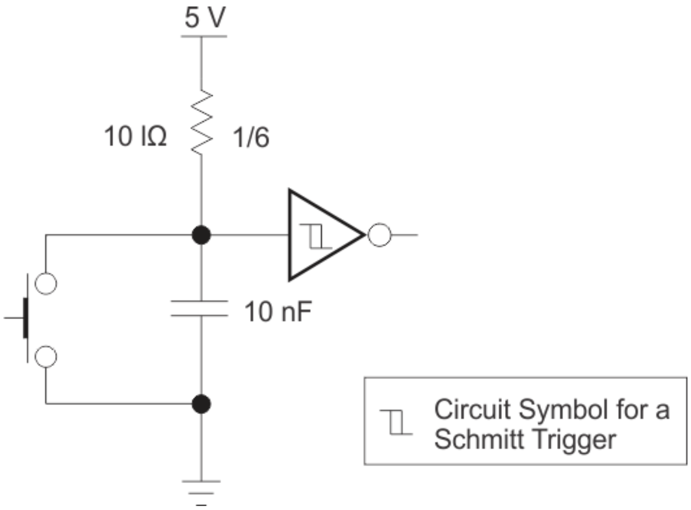

图 9-2. Switch De-bouncer Schematic

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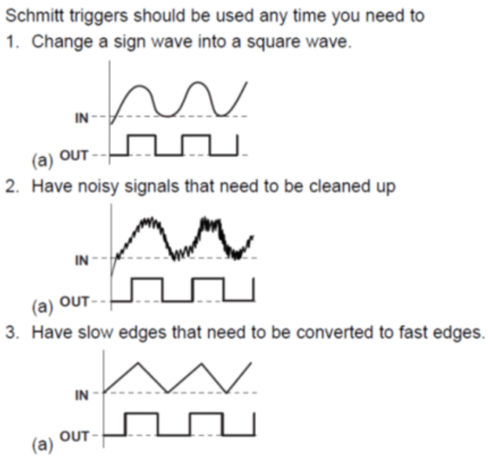
### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
    - For rise time and fall time specifcations, see Δt/ΔV in *节 6.3* table.
    - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in *节 6.3* table.
    - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC.}$
2. Recommend Output Conditions:
    - Load currents should not exceed 35 mA per output and 50 mA total for the part.

### 9.2.3 Application Curves


Schmitt triggers should be used any time you need to

1. Change a sign wave into a square wave.
2. Have noisy signals that need to be cleaned up
3. Have slow edges that need to be converted to fast edges.

图 9-3. Schmitt Trigger Curves

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 *6.3* table.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple $V_{CC}$ terminals then 0.01 µF or 0.022 µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1.0 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the 图 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

### 11.2 Layout Example

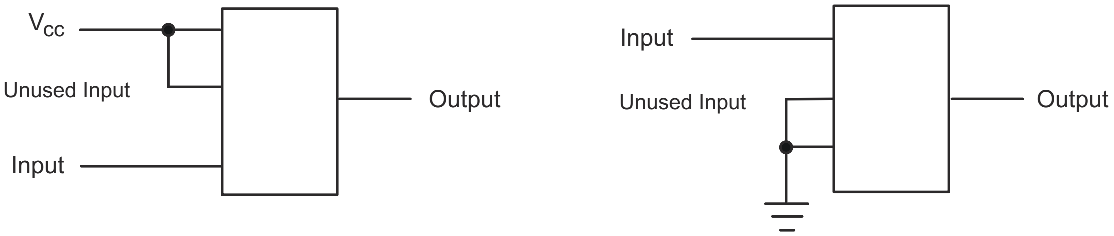


**图 11-1. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LV14A | Click here | Click here | Click here | Click here | Click here |
| SN74LV14A | Click here | Click here | Click here | Click here | Click here |

## 12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV14AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV14A | Samples |
| SN74LV14APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14APWRG3 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV14A | Samples |
| SN74LV14ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV14A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV14A :**

- Automotive : SN74LV14A-Q1

- Enhanced Product : SN74LV14A-EP

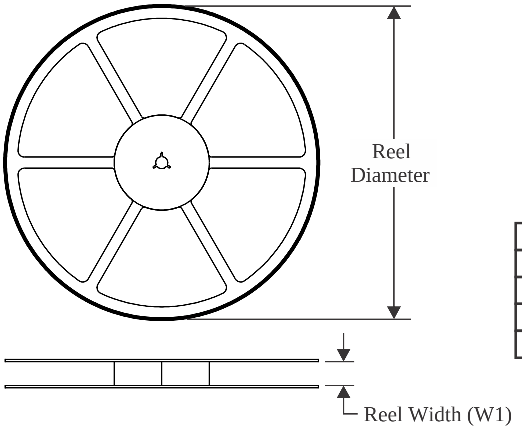
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

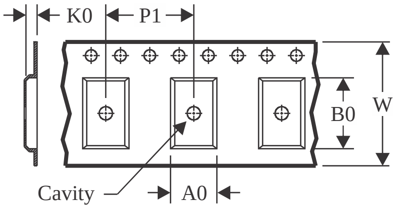
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

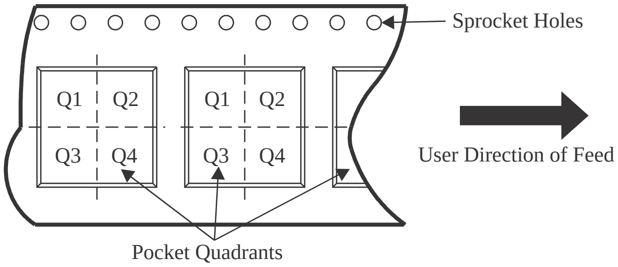


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

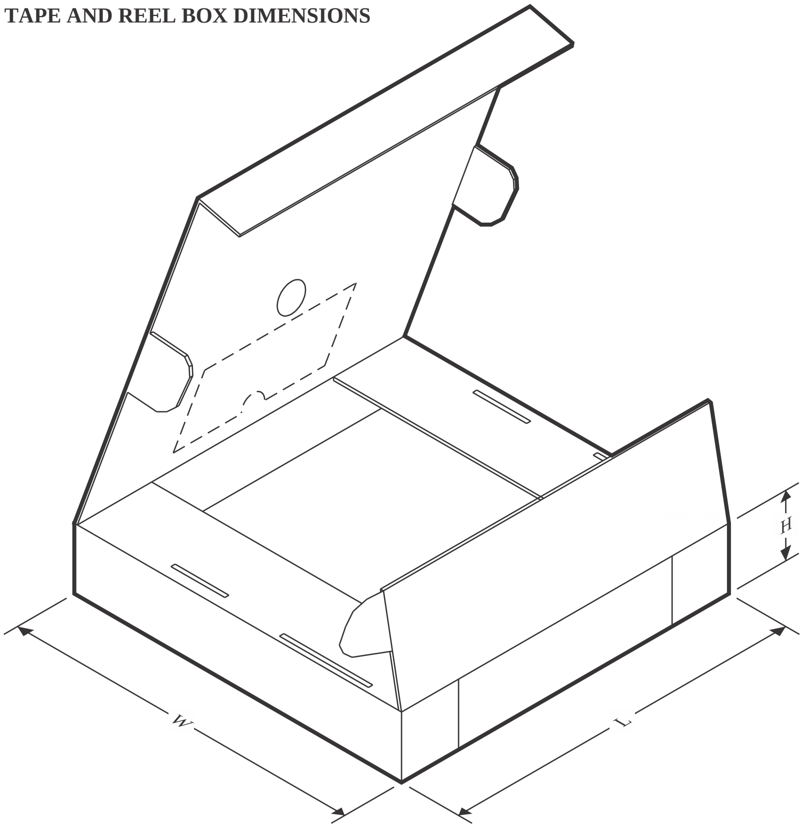
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV14ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV14ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV14ADRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV14ADRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV14ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74LV14APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14APWRG3 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14APWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV14ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

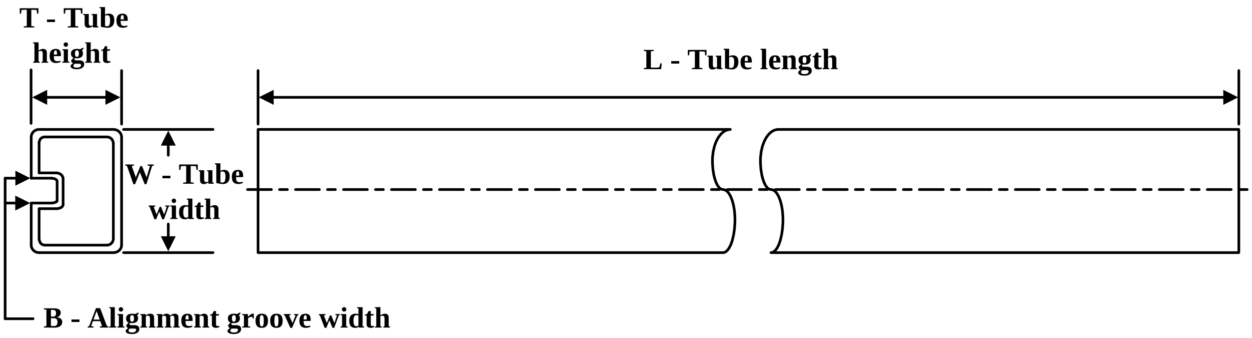
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV14ADBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV14ADGVR | TVSOP | DGV | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV14ADR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV14ADRG4 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV14ADRG4 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LV14ANSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV14APWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV14APWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV14APWRG3 | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV14APWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV14APWT | TSSOP | PW | 14 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LV14ARGYR | VQFN | RGY | 14 | 3000 | 356.0 | 356.0 | 35.0 |

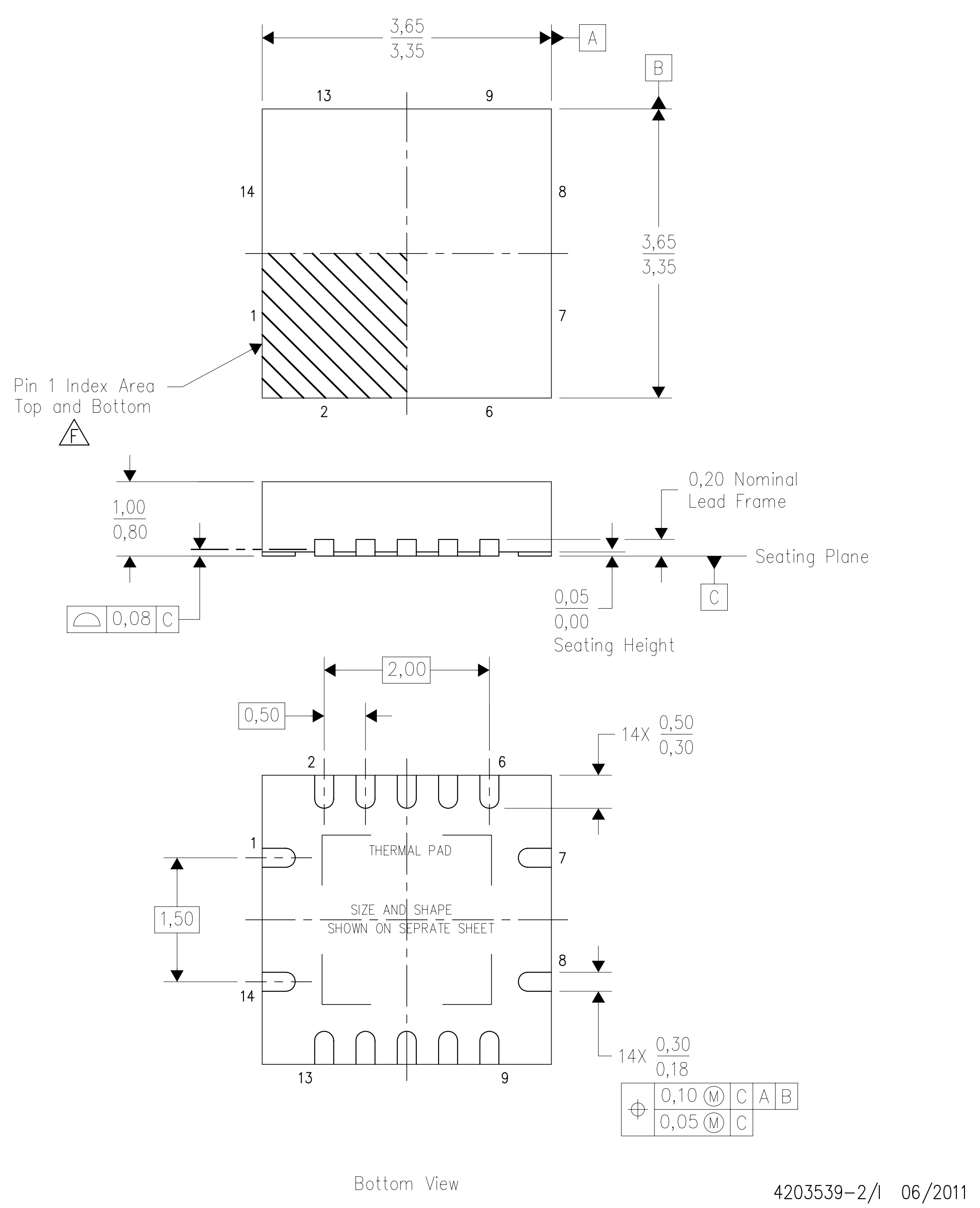
## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LV14AD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN74LV14AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LV14APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LV14APWG4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

## RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- △F Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

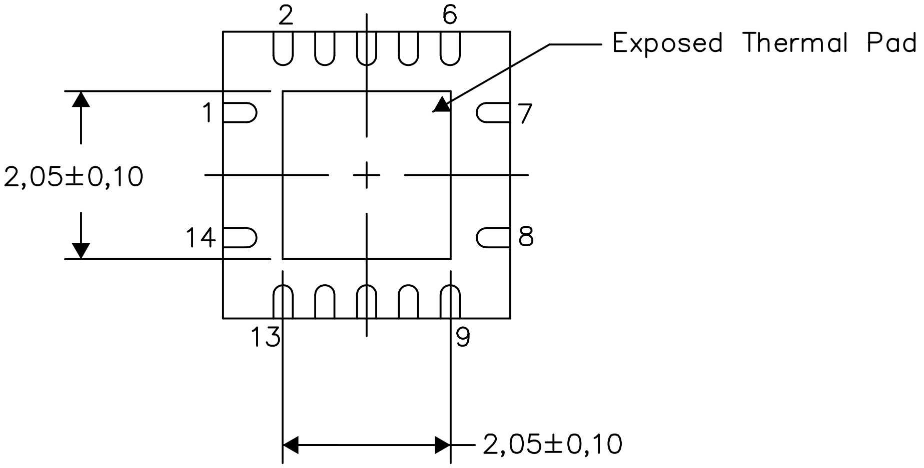
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



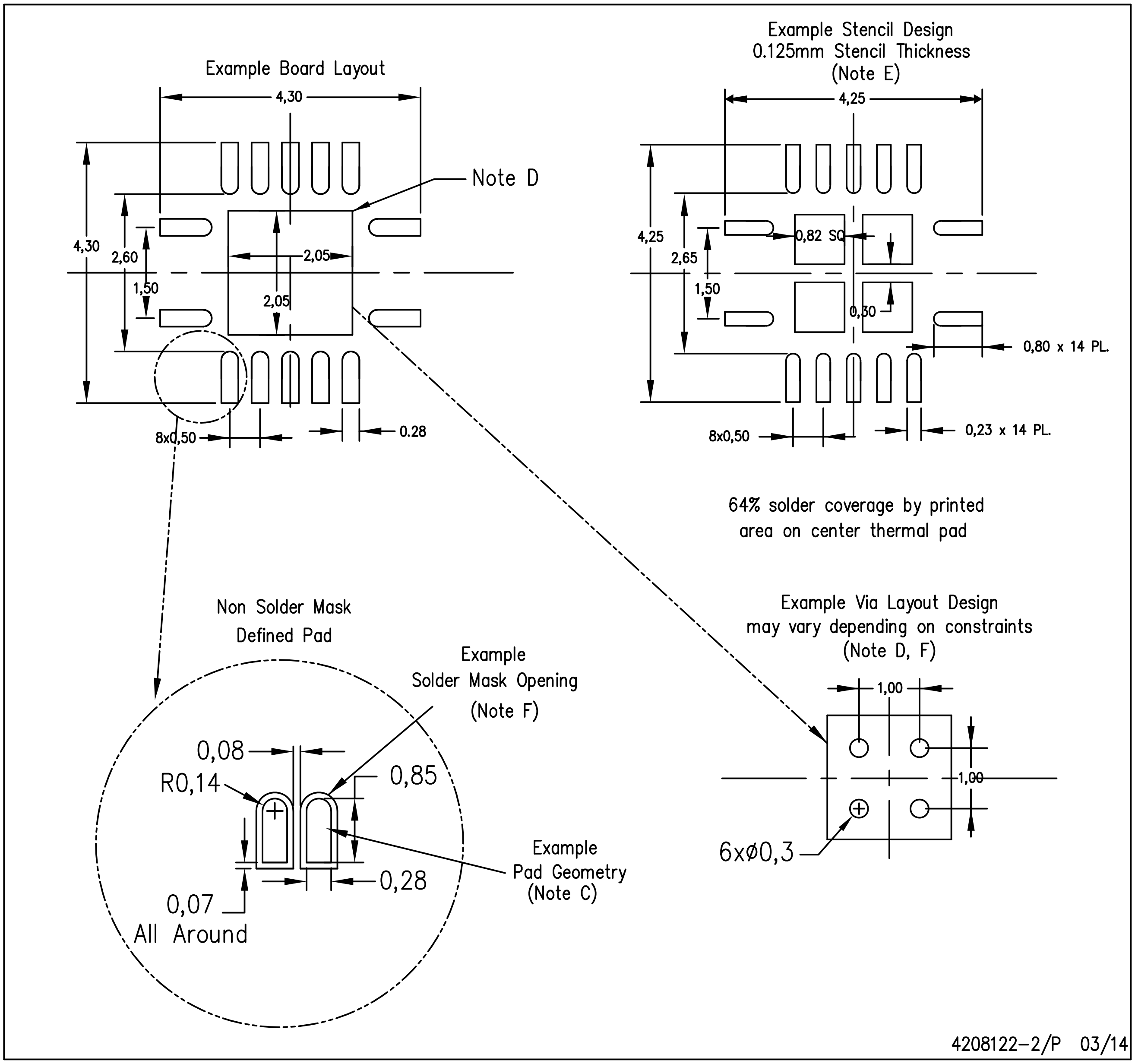
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

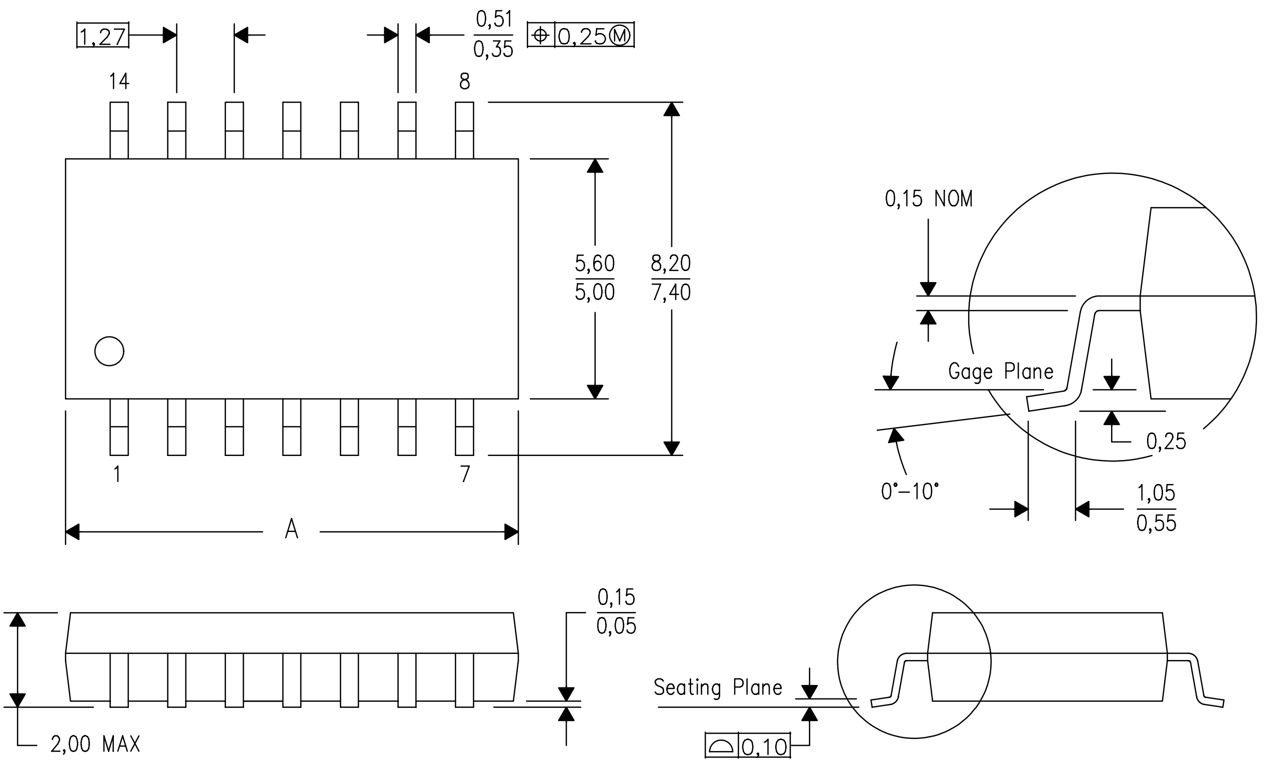
## RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



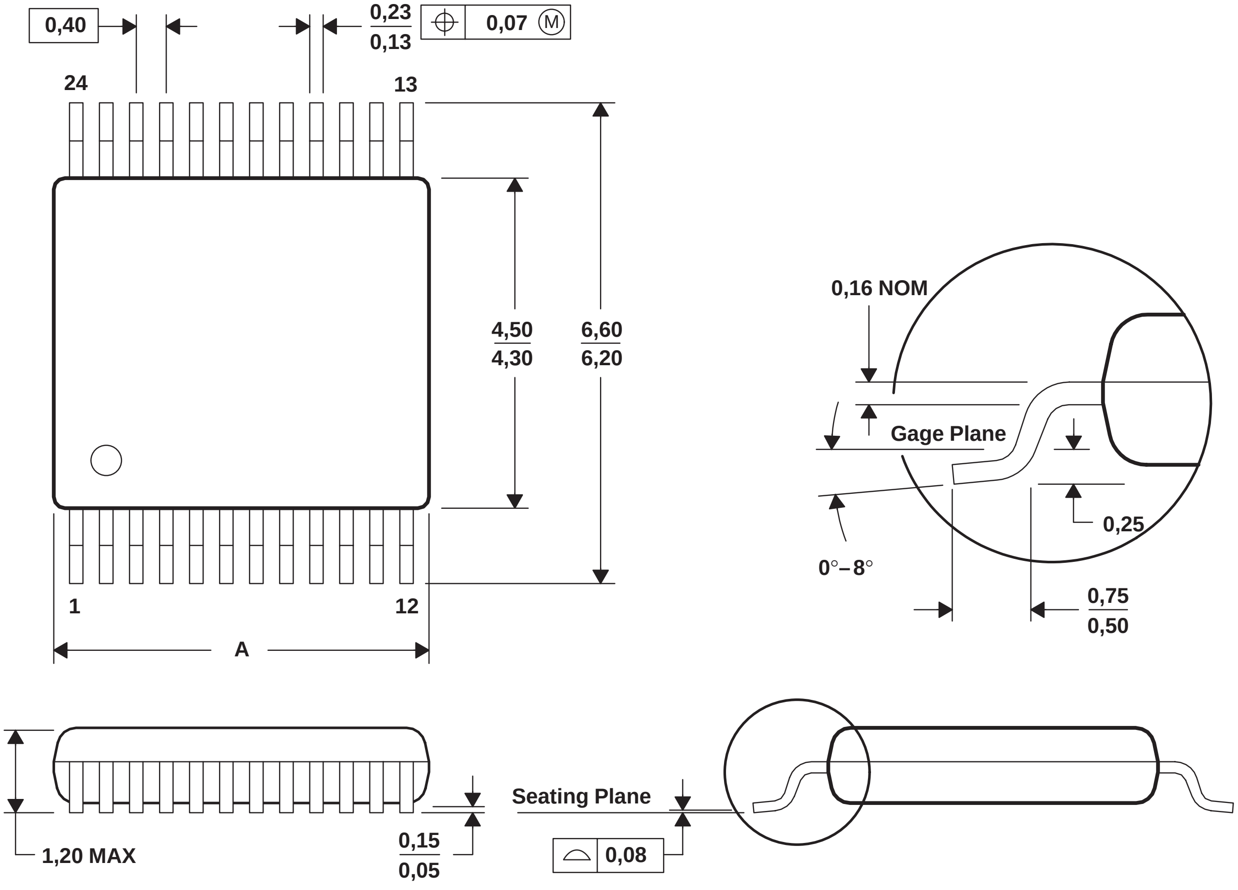
| PINS ** / DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

**24 PINS SHOWN**

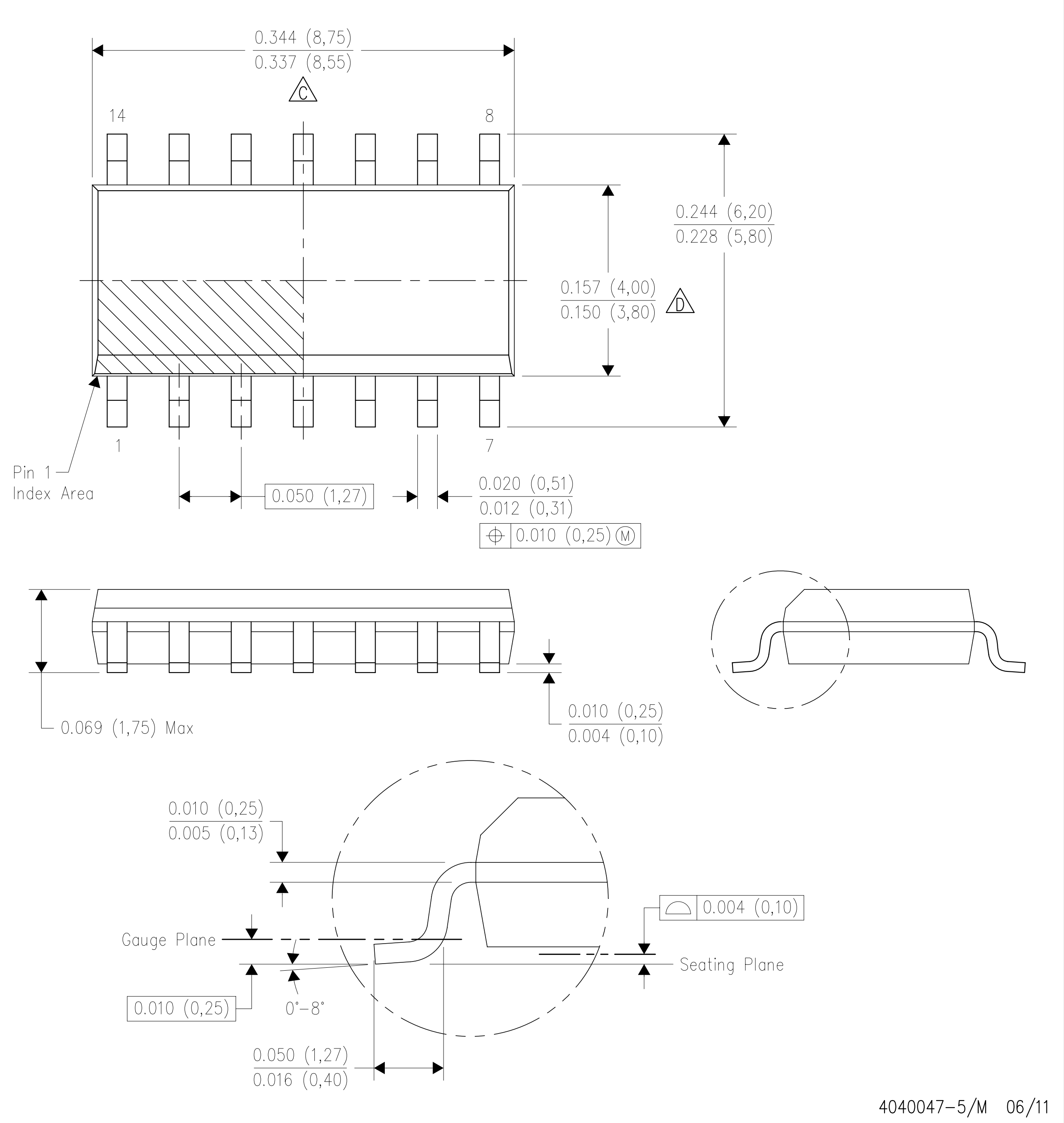


| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

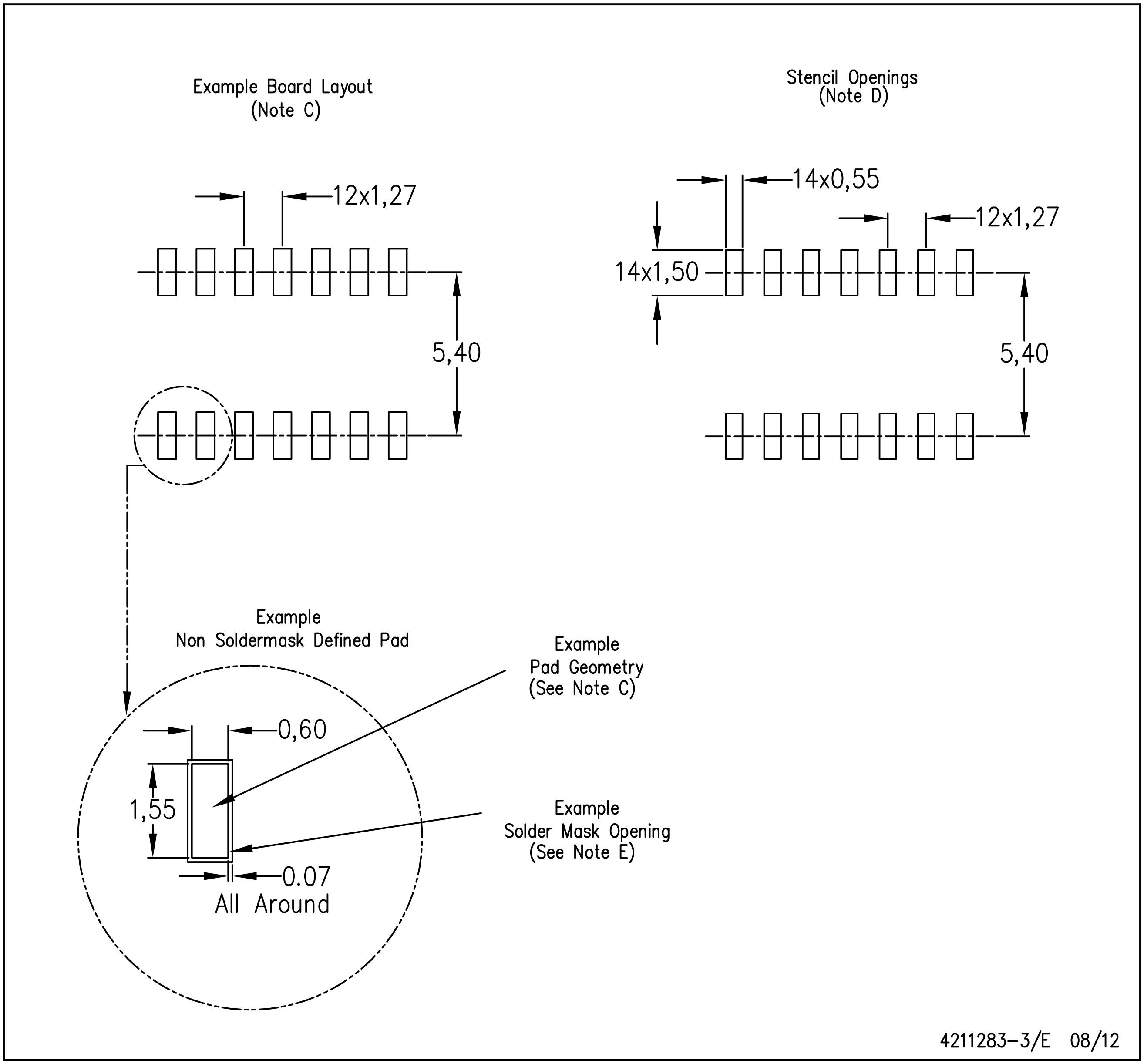
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



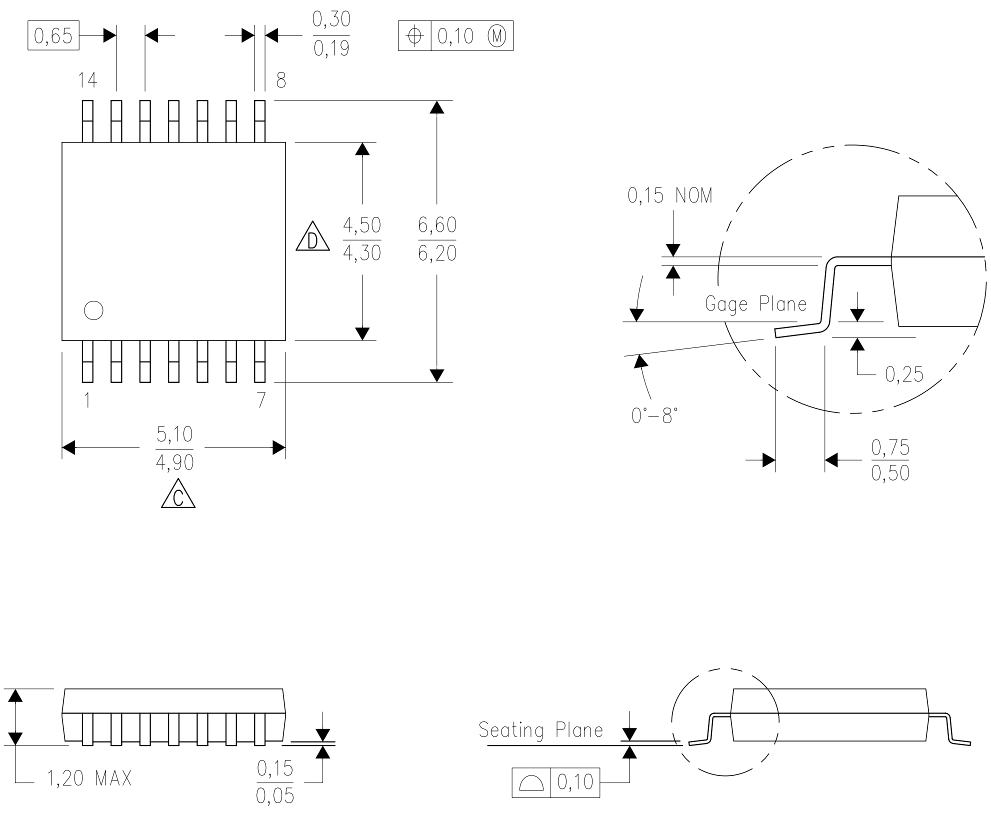
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

## D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

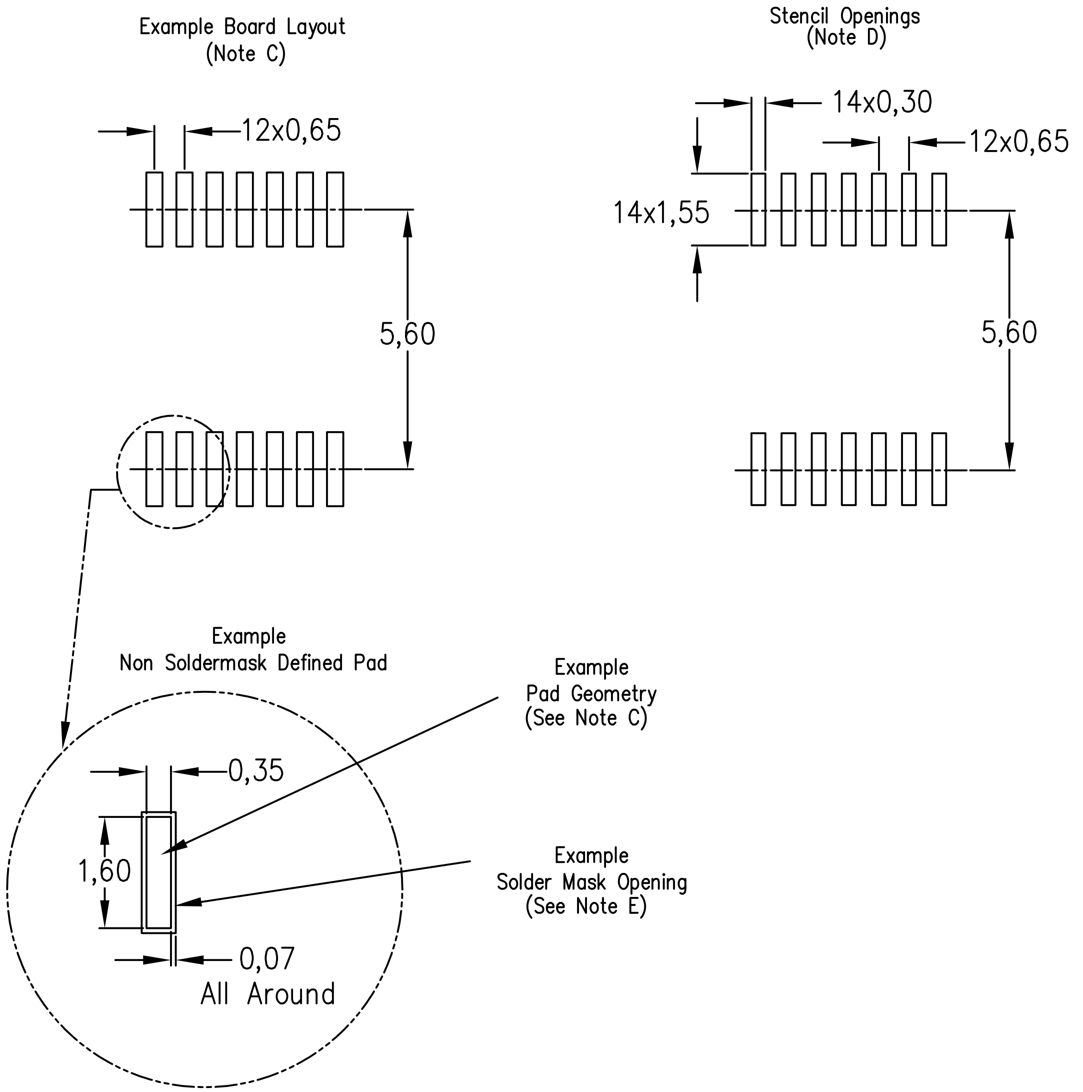
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE



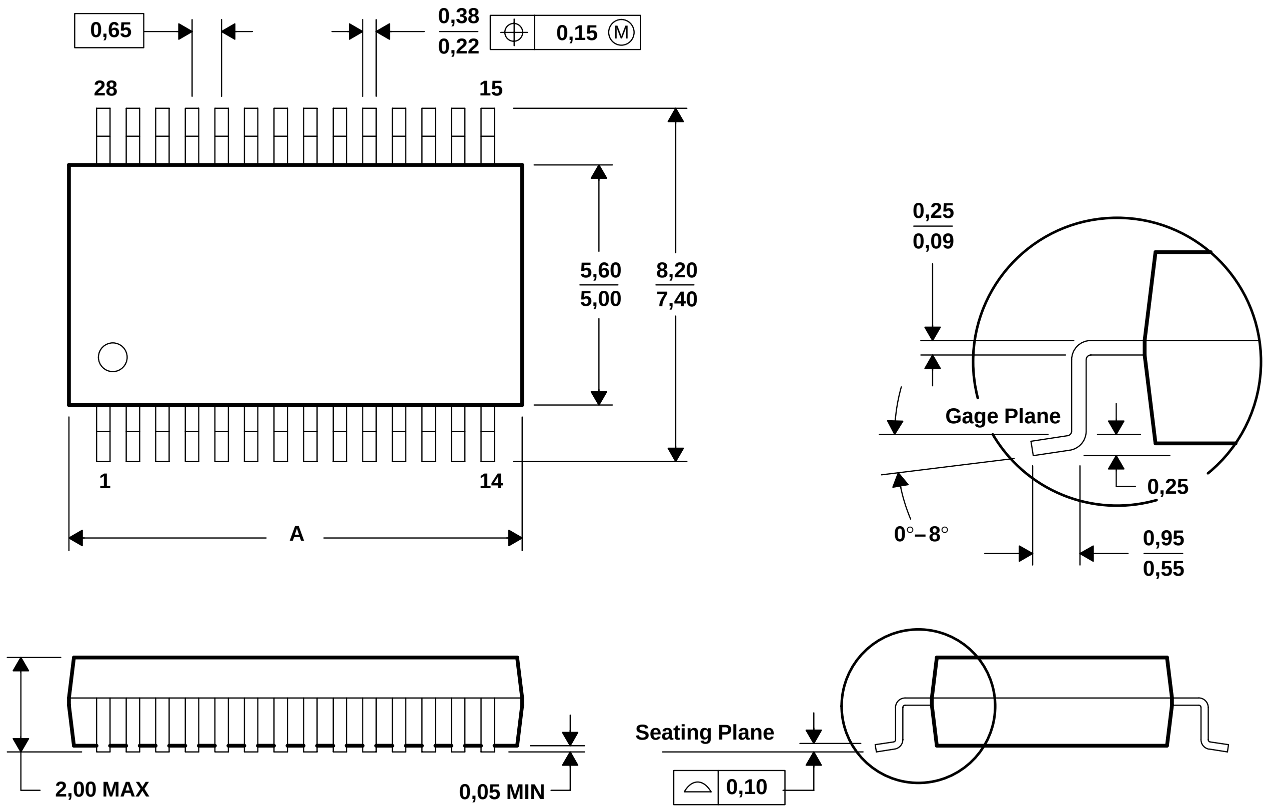
4211284–2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE

**28 PINS SHOWN**



| PINS **<br>DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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