MC145446A

Product Preview

Single-Chip 300-Baud Modem with DTMF Transceiver

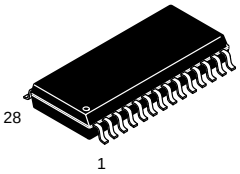
The MC145446A is a silicon gate CMOS frequency shift keying (FSK) modem intended for use with telemeter systems or remote control systems over the telephone network. It replaces the MC145446.

This device is compatible with CCITT V.21 and contains the entire circuit that provides a full–duplex or half–duplex 300–baud data communication over a pair of telephone lines. This device also includes the DTMF generator/receiver and call progress tone detector (CPTD).

The differential line driver has the capability of driving 0 dBm into a 600 Ω load with a single 5 V power supply. The transmit level is controlled by the programmable attenuator in 1 dB steps.

This device also includes a serial control interface and internal control and status registers that permit a CPU to exercise the following built–in features:

- Single 5 V Power Supply
- Compatible with CCITT V.21
- DTMF Generator and Receiver for All 16 Standard Digits
- Capable of Driving 0 dBm into a 600 Ω Load (V_{CC} = 5 V)
- AGC (Auto Gain Control) Amplifier for DTMF Receiver
- Imprecise Call Progress Tone (400 Hz) Detector
- A Transmit Attenuator Programmable in 1 dB Steps
- 2100 Hz Answer Tone Generator
- Serial Control Interface
- Analog Loopback Configuration for Self Test
- Power–Down Mode, Less than 1 μA

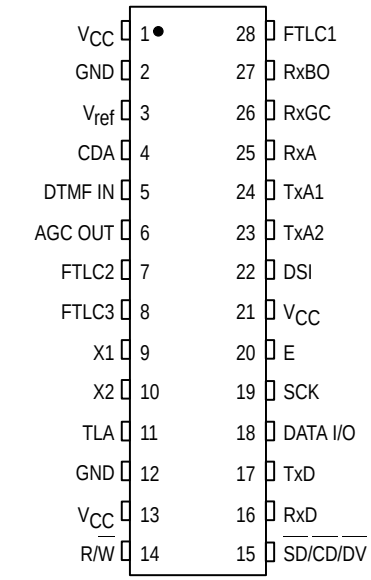


FW SUFFIX
SOP
CASE 751M

ORDERING INFORMATION

MC145446AFW	SOP

PIN ASSIGNMENT

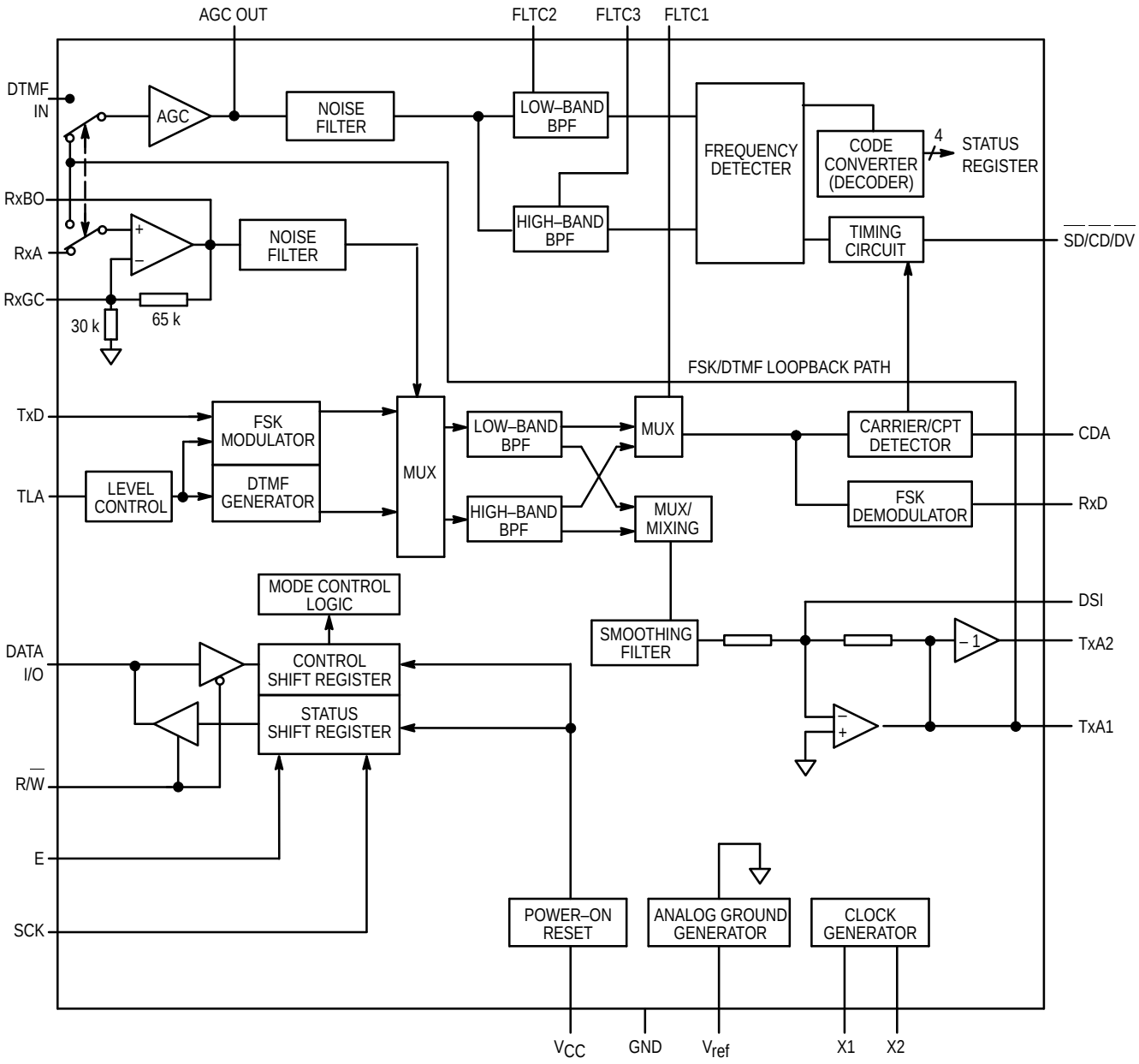


This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
7/96

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to 7.0	V
DC Input Voltage	V_{in}	– 0.5 to V_{CC} + 0.5	V
DC Output Voltage	V_{out}	– 0.5 to V_{CC} + 0.5	V
Clamp Diode Current per Pin	I_{IK}, I_{OK}	± 20	mA
DC Current per Pin	I_{out}	± 25	mA
Power Dissipation	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5	5.5	V
DC Input Voltage	V_{in}	0	—	V_{CC}	V
DC Output Voltage	V_{out}	0	—	V_{CC}	V
Input Rise Time	t_r	0	—	500	ns
Input Fall Time	t_f	0	—	500	ns
Crystal Frequency	f_{osc}	—	3.579545	—	MHz
Operating Temperature Range	T_A	–20	25	70	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	H Level	V_{IH}		3.15	—	—	V
	L Level	V_{IL}		—	—	1.1	
Output Voltage	H Level	V_{OH}	I_{OH} = 20 µA	V_{CC} – 0.1	V_{CC} – 0.01	—	V
	L Level	V_{OL}	I_{OL} = 20 µA I_{OL} = 2 mA	— —	0.01 —	0.1 0.4	
Input Current TxD, E, SCK, DATA I/O, R/W		I_{in}	$V_{in} = V_{CC}$ or GND	—	± 1.0	± 10.0	µA
Quiescent Supply Current		I_{CC}	FSK Mode	—	8	—	mA
			DCMF Receive Mode	—	10	—	
Power–Down Supply Current		I_{CC}	Power–Down Mode 1	—	—	500	µA
			Power–Down Mode 2	—	—	1	µA

TRANSMIT CARRIER CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Carrier Frequency Channel 1	Mark “1”	f_{1M}	Crystal Frequency 3.579545 MHz	974	980	986	Hz
	Space “0”	f_{1S}		1174	1180	1186	
Carrier Frequency Channel 2	Mark “1”	f_{2M}		1644	1650	1656	
	Space “0”	f_{2S}		1844	1850	1856	
Answer Tone		f_{ans}		2090	2100	2110	
Transmit Carrier Level		V_O*	Attenuator = 0 dB $R_{TLA} = \infty$, R_L = 1.2 kΩ, $V_{TxA1} - V_{TxA2}$	—	7	—	dBm
Second Harmonic Energy		V_{2h}*		—	– 46	—	dBm
Out–of–Band Energy		V_{OE}*		Figure 2			dBm

* $V_{TxA1} - V_{TxA2}$, R_L = 1.2 kΩ

TRANSMIT ATTENUATOR CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Attenuator Range		A_{RNG}		0	—	15	dB
Attenuator Accuracy	1 dB – 5 dB	A_{ACC}		– 0.5	—	0.5	dB
	6 dB – 9 dB			– 1	—	1	
	10 dB – 15 dB			– 1.7	—	1	

RECEIVER CHARACTERISTICS (INCLUDES HYBRID, DEMODULATOR, AND CARRIER DETECTOR)
(V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance		R_{IRX}	RxA Pin	50	—	—	kΩ
Receiver Carrier Amplitude		V_{IRX}		– 48	—	– 12	dBm
Carrier Detect Threshold	OFF to ON	V_{CDON}	CDA = 1.2 5V f_{in} = 1.0 kHz	—	– 44	—	dBm
	ON to OFF	V_{CDOF}		—	– 47	—	
Hysterisis (V_{CDON} – V_{CDOF})		HYS		2	—	—	dB
Carrier Detect Timing	OFF to ON	T_{CDON}	CD1 = 0, CD0 = 0	—	450	—	ms
			CD1 = 0, CD0 = 1	—	10	—	
			CD1 = 1, CD0 = 0	—	10	—	
			CD1 = 1, CD0 = 1	—	70	—	
	ON to OFF	T_{CDOFF}	CD1 = 0, CD0 = 0	—	35	—	
			CD1 = 0, CD0 = 1	—	35	—	
			CD1 = 1, CD0 = 0	—	20	—	
			CD1 = 1, CD0 = 1	—	15	—	

CPTD CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Bandpass Filter Center Frequency		f_c		—	400	—	Hz
Bandpass Filter – 3 dB Band Width		Δ_{BW}		—	140	—	Hz
Tone Detect Level	OFF to ON	V_{TDON}	CDA = 1.25 V f_{in} = 400 Hz	—	– 44	—	dBm
	ON to OFF	V_{TDOF}		—	– 47	—	
Tone Detect Timing	OFF to ON	T_{TDON}		—	10	—	ms
	ON to OFF	T_{TDOF}		—	25	—	

DTMF TRANSMIT CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Tone Output Level	Low Group	V_{fl}	Attenuator = 0 dB RTLA = ∞ Crystal Frequency 3.579545 MHz Single Tone Mode V_{TxA1} – V_{TxA2}, R_L = 1.2 kΩ	—	2.5	—	dBm
	High Group	V_{fh}		—	3.5	—	
High Group Pre–Emphasis		P_E		0	—	3	dB
DTMF Distortion		DIST		—	5	—	%
DTMF Frequency Variation		Δf_V		– 1	—	1	%
Out–of–Band Energy		V_{OE}		Figure 1			dB
Setup Time		t_{osc}		—	4	—	ms

DTMF RECEIVER CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance				50	—	—	kΩ
Detect Signal Level (Each Tone)				– 48	—	0	dBm
Twist (High Group Tone/Low Group Tone				– 10	—	10	dB
Frequency Detect Band Width (Figure 4)				±1.5% ±2Hz	—	—	—
Frequency No–Detect Band Width (Figure 4)				—	—	± 3.5	%
DTMF Detect Timing	OFF to ON	T_{CDON}	CD1 = 0, CD0 = 1	—	25	—	ms
			CD1 = 1, CD0 = 0	—	30	—	
			CD1 = 1, CD0 = 1	—	40	—	
	ON to OFF	T_{CDOFF}	CD1 = 0, CD0 = 1	—	25	—	
			CD1 = 1, CD0 = 0	—	35	—	
			CD1 = 1, CD0 = 1	—	25	—	

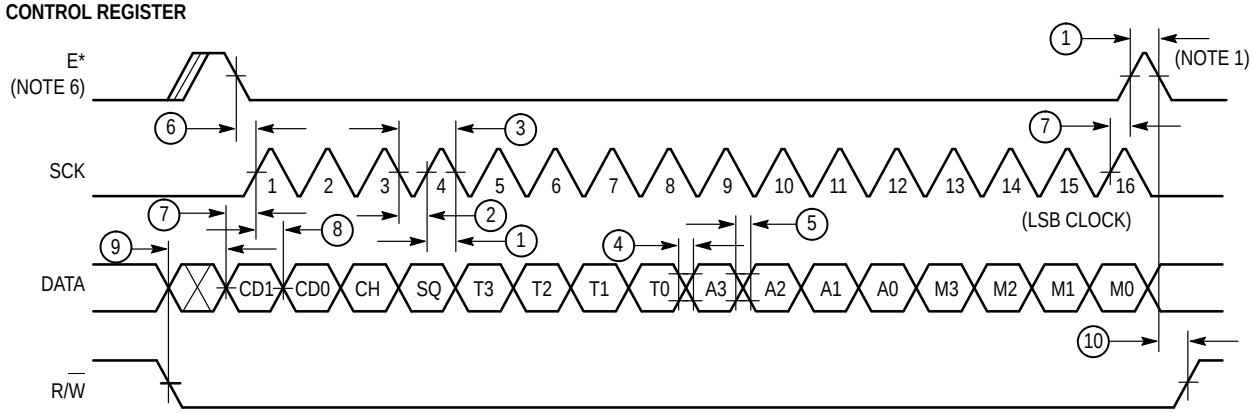
DEMODULATOR CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Bit Bias	ID	Input Level = – 24 dBm S/N = 4 dB	—	5	—	%
Bit Error Rate (CCITT Line Simulation, 511–Bit Pattern)	BER		—	0.00001	—	—

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = – 20 to 70°C)

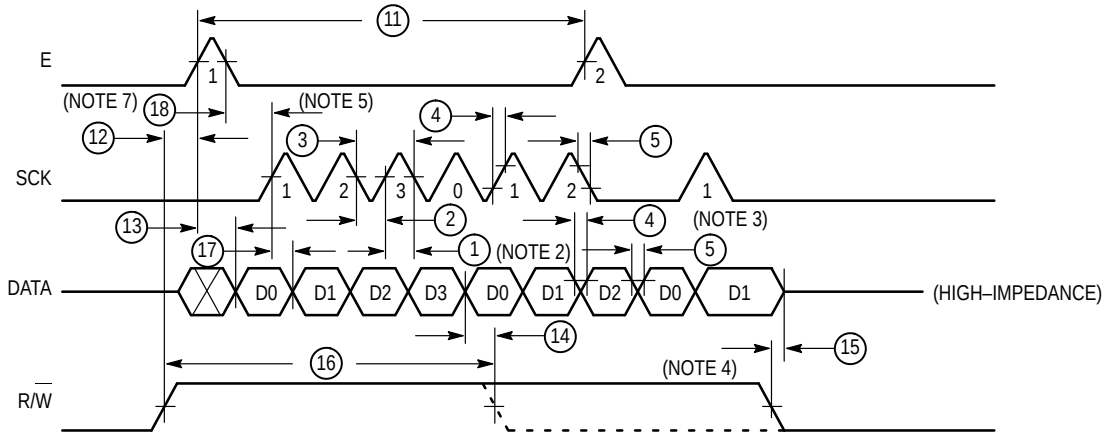
Characteristic		Symbol	Timing Diagram Reference No.	Min	Typ	Max	Unit
Input Pulse Width (H) E, SCK		t_{wh}	1	50	—	—	ns
Input Pulse Width (L) E, SCK		t_{wl}	2	50	—	—	ns
Clock Cycle		t_c	3	100	—	—	ns
Input Rise Time		t_r	4	—	—	2	µs
Input Fall Time		t_f	5	—	—	2	µs
Recovery Time E to SCK		t_{rec}	6, 18	50	—	—	ns
Setup Time	DATA to SCK	t_{su}	7	50	—	—	ns
	$\overline{R/W}\downarrow$ to DATA		9	100	—	—	ns
	$\overline{R/W}\uparrow$ to DATA		12	50	—	—	ns
Hold Time	SCK to DATA	t_h	8	50	—	—	ns
	E to $\overline{R/W}$		10	50	—	—	ns
	DATA to $\overline{R/W}$		14	50	—	—	ns
	$\overline{R/W}$ to DATA		15	50	—	—	ns
Read Data Delay Time	E to DATA	t_d	13	—	—	50	ns
	SCK to DATA		17	—	—	50	ns
Enable Minimum Interval		t_{we}	11	—	—	450	ns
Mode Switch Minimum Interval		t_{wm}	16	—	—	600	ns

CONTROL REGISTER



* The enable signal corresponds to preceding data format.

STATUS REGISTER



NOTES:
1. The data in front of the enable signal pulse will be latched.
2. The latched data will be repeated until there is an enable pulse.
3. The detected data will be updated with the next enable pulse.
4. After the R/W pin becomes INACTIVE, the data will be lost.
5. D1 corresponds to Clock1.
6. The enable and the SCK signals need to be set at the logic low level when the R/W signal changes.
7. The SCK must be held at low level when the enable signal is at high level.

Figure 1. Serial Data Input Timing

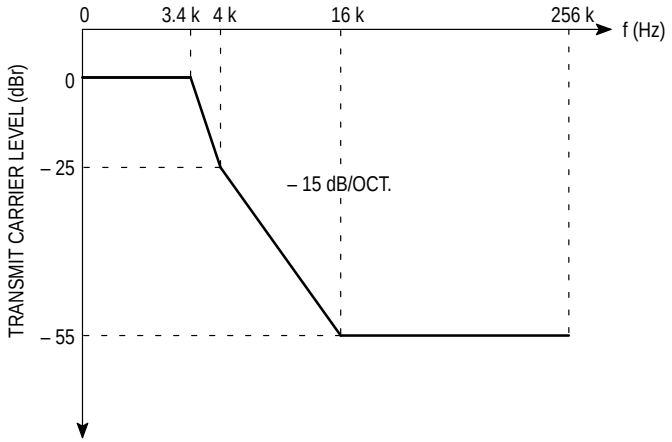


Figure 2. Out–of–Band Energy

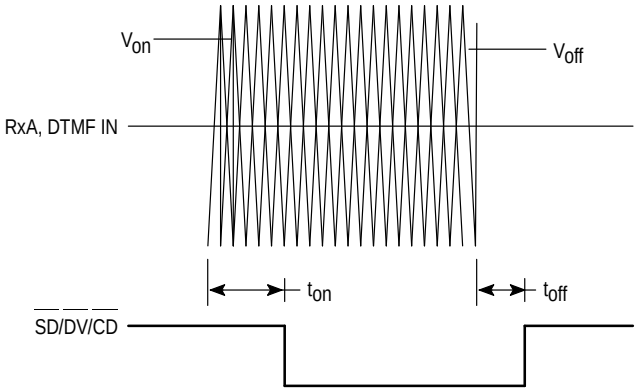


Figure 3. FSK, DTMF Carrier Detect Timing

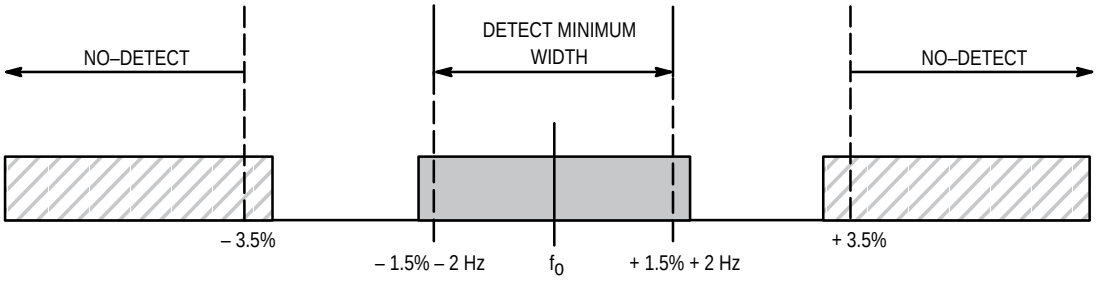


Figure 4. DTMF Frequency Detect Bandwidth

PIN DESCRIPTIONS

V_{CC}
Positive Power Supply (Pins 1, 13, 21)

The digital supply pins, which are connected to the positive power supply (5 V).

GND
Ground Pins (Pins 2, 12)

The ground pins are connected to the system ground.

V_{ref}
Reference Analog Ground (Pin 3)

This pin provides the analog ground voltage, which is internally regulated to $V_{CC}/2$. It should be decoupled to the GND with 0.1 μF and 100 μF capacitors.

X1
Crystal Oscillator Output (Pin 9)

A 3.579545 MHz ± 0.1% crystal oscillator is tied to this pin with the other end connected to X2.

X2
Crystal Oscillator Input (Pin 10)

A 3.579545 MHz ± 0.1% crystal oscillator is tied to this pin with the other end connected to X1. X2 may also be driven directly from an appropriate external source.

SCK
Serial Clock Input (Pin 19)

This pin is the clock input for the 16–bit control resistor and the 4–bit status resistor. The serial data is captured into the control register, or is shifted out of the status register on the rising edge of SCK.

DATA I/O
Serial Data Input/Output (Pin 18)

This pin is the 16–bit control register input, which determines the operation mode, DTMF tone, transmit attenuation (receiver gain), carrier detect time, channel, and transmit squelch. This pin is also the four–bit status register output which indicates the received DTMF tone (hexadecimal codes).

E
Enable Input (Pin 20)

When the R/$\overline{W}$ pin is at logic low, high level on the E pin makes the 16–bit control register data transparent to the mode control logic so that the device operation is changed. While this pin is at logic low, the control register and the mode control logic are isolated. The E pin must NOT be held high while the control register data is being changed.

When the R/W pin is at logic high, the rising edge of E transfers the four–bit DTMF data from the DTMF decoder to the status register. Then the first bit (LSB = D0) is presented at the Data I/O pin.

R/$\overline{W}$
Read/Write Data Switch (Pin 14)

This pin is used for controlling the I/O direction of the Data I/O pin.

TxD
Transmit Data Input (Pin 17)

This pin is the transmit data input. When the device is in FSK mode, the mark frequency is generated when this pin is at the logic high level. The space frequency is generated when the pin is at a logic low.

RxD
Receive Data Output (Pin 16)

This pin is the receive data output. When the device is in the FSK mode, a high logic level of this pin indicates that the mark carrier frequency has been received, and a low logic level indicates the space carrier frequency has been received.

$\overline{SD}/\overline{CD}/\overline{DV}$
Carrier/Call Progress Tone Detect/DTMF Data Valid Detect (Pin 15)

This pin works as a carrier detector in the FSK mode, whereas it works as the call progress tone detector in the CPTD mode and as the receive DTMF detector in the DTMF Rx mode. The output goes to a logic low level when the input signal reaches the minimum threshold of the detect level that is adjusted by the CDA voltage. When this pin is logic high, the receive data output (RxD) is clamped high to avoid the error that may occur with the loop noise.

In DTMF Rx mode, the logic low on this pin indicates that the valid DTMF frequencies are detected. The received tone is decoded to four–bit data, then stored in the DTMF decoder by the falling edge of DV.

TxA1
Non–Inverting Transmit Analog Carrier Output (Pin 24)

This pin is the line driver non–inverting output. A 7 dBm (typ) differential output voltage can be obtained by connecting a 1.2 kΩ load resistor between Tx1 and Tx2. Attention must be paid so as not to exceed this level when an external input is added to the DSI pin. A telephone line (600 Ω) is driven through an external 600 Ω resistor (see the Application Circuit). In this case, the output level becomes about a half of the differential output.

TxA2
Inverting Transmit Analog Carrier Output (Pin 23)

This pin is the line driver inverting output. The signal is equal in magnitude, but 180° out of phase with the TxA1 (refer to TxA1).

RxA
Receive Signal Input (Pin 25)

This pin is the carrier signal input, and is enabled when the device is in FSK or CPTD mode.

RxGC
Receive Gain Adjust (Pin 26)

This pin is used to adjust the receive buffer gain. To adjust the gain, a resistor may be added between this pin and the RxBO pin (refer to the Block Diagram). This pin may be held open when the gain adjustment is not needed.

RxBO
Receive Buffer Output (Pin 27)

This pin is the receive buffer output.

DTMF IN
DTMF Receive Input (AGC Amp Input) (Pin 5)

This pin is the receive DTMF signal input. It is enabled when the device is in the DTMF receive mode.

AGC OUT
AGC Output (Pin 6)

This pin is used by the manufacturer to test the auto gain control amplifier. It should be held open in normal operation.

DSI
Driver Summing Input (Pin 22)

This pin is the inverting input of the line driver. An external signal may be transmitted through an external series resistor R_{DSI}. The differential gain $G_{DSI} = (V_{TxA1} - V_{TxA2})/V_{DSI}$ is determined by the following equation:

$$G_{DSI} = -2Rf / R_{DSI}, Rf \sim 20\ k\Omega$$

Note that the programmable transmit attenuator does not affect in this case.

The DSI pin should be held open when not in use.

CDA
Carrier Detect Level/CPTD Level Control (Pin 4)

The carrier/call progress tone detect level is adjusted by the CDA pin voltage.

When this pin is held open, the CDA voltage is set to 1.25 V ($V_{CC} = \pm 5$ V) by an internal divider. Then the detect level is set at – 44 dBm (typ) for off to on, and – 47 dBm (typ) for on to off, and the hysteresis is set minimum 2 dB. This pin has a very high input impedance so it should be connected to GND with a 0.1 μF capacitor to keep it under the regulations. An external voltage may be applied to this pin to adjust the carrier detect threshold. The following equations may be used to find the CDA voltage required for a given threshold voltage:

$$V_{CDA} = 245 \times V_{on}$$
$$V_{CDA} = 347 \times V_{off}$$

TLA
Transmit Carrier Level Adjust (Pin 11)

This pin is used to adjust the transmit carrier level that is determined by the value of the resistor (RTLA) connected between this pin and the GND. The maximum level can be obtained when this pin is shorted to GND (RTLA = 0).

FTLC1
FSK Filter Test (Pin 28)

This pin is a high–impedence filter output. It may be used for testing the FSK filter characteristics, and is reserved for manufacturer's use only. In normal operation, this pin should be decoupled to V_{ref} with a 0.1 μF capacitor.

FTLC2
DTMF Receive Low Group Filter Test (Pin 7)

This pin is a high–impedence filter output. It may be used for testing the DTMF receive high goup bandpass filter characteristics, and is reserved for manufacturer's use only. In normal operation, this pin should be decoupled to V_{ref} with a 0.1 μF capacitor.

FTLC3
DTMF Receive High Group Filter Test (Pin 8)

This pin is a high–impedence filter output. It may be used for testing the DTMF receive high group bandpass filter characteristics, and is reserved for manufacturer's use only. In normal operation, this pin should be decoupled to V_{ref} with a 0.1 μF capacitor.

SERIAL CONTROL INTERFACE

The following six functions are determined by the 16 bits of serial data in the control register.

CONTROL REGISTER

FUNCTION MODE :	M3	M2	M1	M0
TRANSMIT ATTENUATOR :	A3	A2	A1	A0
TRANSMIT TONE FREQUENCY :	T3	T2	T1	T0
TRANSMIT SQUELCH :	SQ			
CHANNEL :	CH			
CARRIER DETECT TIME :	CD1	CD0		

The received DTMF tones are indicated by the four bits of data in the status register.

STATUS REGISTER

RECEIVE TONE FREQUENCY :	D3	D2	D1	D0

Figure 1 presents the timing diagram of 16–bit control register input and four–bit status output. When the R/W pin is in logic low, the 16–bit data is captured into the control register at the rising edge of SCK and latched in the mode control logic to update the function mode at logic high input to the E pin. When the R/W pin is in logic high, the status register is selected to read out the received DTMF data, the four–bit data in the DTMF decoder is loaded into the status register, and the first bit (D0) is presented at the Data I/O on the rising edge of E. The following bits are repeatedly shifted out as D1–D2–D3–D0–D1–... by the rising edges of SCK.

CONTROL REGISTER BIT MAP DESCRIPTION

FUNCTION MODE (M3 to M0)

One of the following modes is selected from the four–bit data (M3 to M0) shown in Table 1. Table 2 presents each output status; the functions are described below.

Table 1. Function Mode Truth Table

M3	M2	M1	M0	Function Mode
0	0	0	0	FSK
0	0	0	1	FSK Analog Loopback
0	0	1	0	CPTD
0	0	1	1	Answer Tone
0	1	0	0	DTMF Transmit
0	1	0	1	Single Tone
0	1	1	0	Power–Down 1
0	1	1	1	Power–Down 2
1	0	0	0	DTMF Receive
1	0	0	1	DTMF Analog Loopback

FSK Mode

The transmitter and the receiver work as an FSK modulator/demodulator. The SD pin goes low when a valid FSK signal is detected.

DTMF Transmit Mode

The transmitter works as a DTMF tone generator. The receiver is disabled.

CPTD (Call Progress Tone Detect) Mode

The receiver works as a 400 Hz call progress tone detector. The CD pin goes low when a valid call progress tone is detected.

Answer Tone Mode

The transmitter works as a 2100 Hz answer tone generator. The receiver is disabled.

FSK Analog Loopback Mode

The transmitter, working as the FSK modulator, is internally connected to the receiver working as the FSK demodulator. This feature is used for the device self test.

DTMF Receive Mode

The receiver works as a DTMF tone receiver. The $\overline{DV}$ goes low when a valid DTMF tone is detected. The transmitter is disabled.

DTMF Analog Loopback Mode

The transmitter, working as a DTMF tone generator, is internally connected to the receiver working as DTMF tone receiver. The DV goes low when the receiver detects a valid DTMF tone. This feature is used for the device self test.

Single Tone Mode

The transmitter generates one of the eight frequencies of the DTMF tone. The receiver is disabled.

Power–Down Mode 1

Whole internal circuits, except the oscillator, are disabled and all outputs except the X1 pin go to the high–impedance state. The supply current decreases to 500 μA (max).

Power–Down Mode 2

Whole internal circuits, including the oscillator, are disabled and all outputs go to the high–impedance state. The supply current decreases to 1.0 μA (max).

Transmit Attenuator/AGC Gain Set (A3 to A0)

Four–bit serial data (A3 – A0) sets up the analog transmit level in the FSK, answer tone, DTMF, analog loopback, and single tone mode. The range of the transmit attenuator is 0 to 15 dB in 1 dB steps. The attenuator, however, does not affect the external signal input from the DSI. These bits also determine the AGC amplifier gain in the DTMF receive mode. In normal operation, “Automatic” may be selected so that the gain is automatically adjusted corresponding to the input signal level. See Table 3 for a detailed description.

Transmit Tone Frequency (T3 to T0)

These four bits (T3 to T0) determine the DTMF tone frequencies in DTMF transmit and DTMF analog loopback mode, and determine the single tone frequency in the single tone mode. Tone frequency assignments with reference to T3 – T0 are shown in Table 4.

Table 2. Output Status

Function Mode	Output Pin		
	RxD	SD/CD/DV	TxA1, TxA2
FSK	Receive Digital Data	Carrier Detect Signal	FSK
FSK Loopback			
Call Progress Tone	H	CPTD Signal	$V_{CC}/2$
Answer Tone	H	H	Answer Tone
DTMF Transmit	H	H	DTMF Tone
Single Tone	H	H	Single Tone
Power–Down 1, 2	High Impedance	High Impedance	High Impedance
DTMF Receive	H	DV Signal	$V_{CC}/2$
DTMF Loopback			DTMF Tone

Table 3. Transmit Attenuator/AGC Gain Set Truth Table

A3	A2	A1	A0	Attenuation (dB)	AGC Gain Step (dB)
0	0	0	0	0	– 5.0
0	0	0	1	1	– 2.5
0	0	1	0	2	0.0
0	0	1	1	3	2.5
0	1	0	0	4	5.0
0	1	0	1	5	7.5
0	1	1	0	6	10.0
0	1	1	1	7	12.5
1	0	0	0	8	15.0
1	0	0	1	9	17.5
1	0	1	0	10	20.0
1	0	1	1	11	Clamp
1	1	0	0	12	Automatic
1	1	0	1	13	—
1	1	1	0	14	—
1	1	1	1	15	—

Table 4. Tone Frequency Truth Table

T3/D3	T2/D2	T1/D1	T0/D0	Tone Frequency (Hz)			
				DTMF Mode			Single Tone Mode
				Low Group	High Group	Keyboard Equivalent	
0	0	0	0	941	1633	D	941
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633
1	1	1	1	852	1633	C	1633

Transmit Squelch

The 1–bit serial data (SQ) controls the transmit analog squelch. The FSK signal, DTMF tones, single tone, and answer tone are disabled, then TxA1 and TxA2 will be clamped to $V_{CC}/2$ when the transmit squelch goes to the Enable (SQ = 1) state. The transmit squelch does not affect the external signal from the DSI.

Table 5. Transmit Squelch Truth Table

SQ	Squelch
1	Enable
0	Disable

Channel

When the function mode is either on the FSK or analog loopback mode, the transmit and receive channel is set up with a 1–bit serial data (CH).

Table 6. Channel Truth Table

CH	Channel
1	1 (Originate)
0	2 (Answer)

Carrier Detect Time

The carrier and DTMF tone detect timing are determined by two–bit serial data (CD1, CD0). The timing diagram is shown in Figure 3.

Table 7. Carrier/DTMF Detect Time Truth Table

CD1	CD0	FSK Mode Carrier Detect Time (typ)		DTMF Receive Mode Carrier Detect Time (typ)	
		t_{on} (ms)	t_{off} (ms)	t_{on} (ms)	t_{off} (ms)
0	0	450	35	Reserved	
0	1	10	35	25	25
1	0	10	20	30	35
1	1	70	15	40	25

Power–On Reset

When the power is switched on, this device is entered into Power–Down Mode 2 by the internal power–on reset circuit.

STATUS REGISTER BIT MAP DESCRIPTION

Received Tone Frequency (D3 to D0)

This four–bit data (D3 to D0) indicates the received DTMF tones. The first bit (D0) is presented at Data I/O on the rising edge of E, and the following bits (D1–D2–D3–D0–D1– ...) are shifted out and presented on the next rising edge of SCK.

The data configuration corresponding to each tone is shown in Table 4.

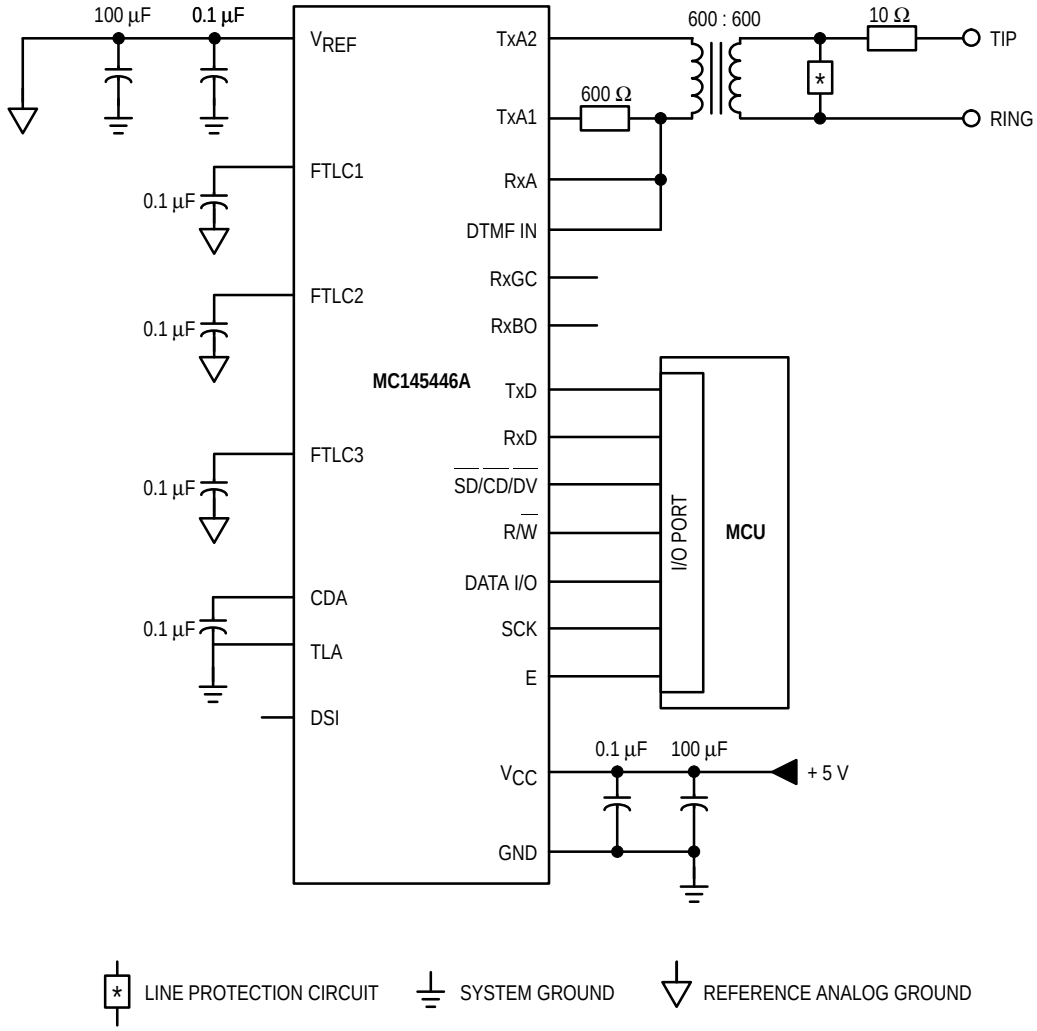
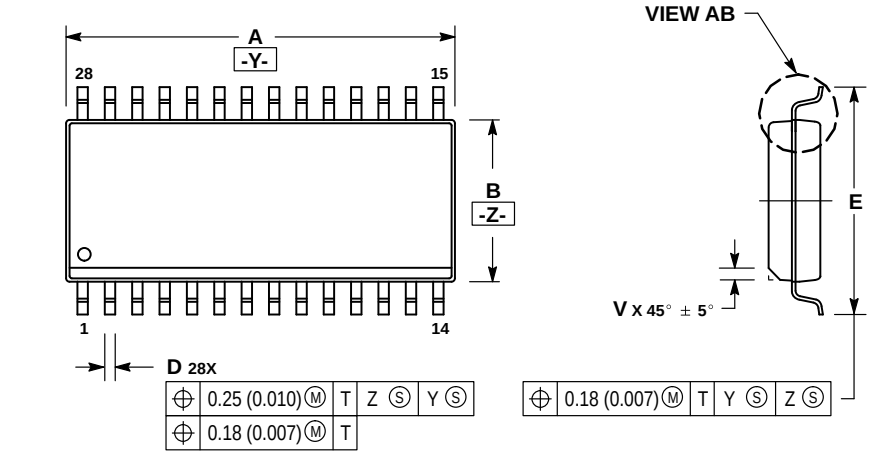


Figure 5. Application Circuit

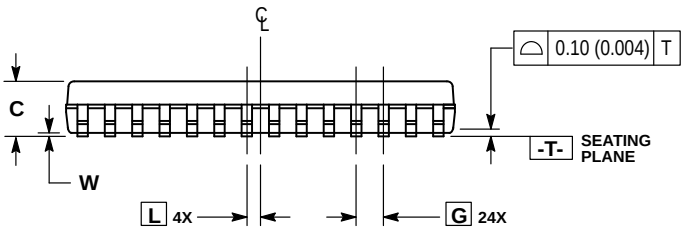
PACKAGE DIMENSIONS

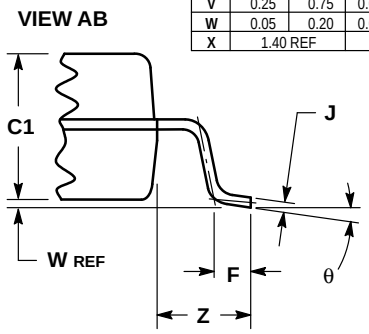
FW SUFFIX
SOP
CASE 751M–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.65 (0.026).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.03	0.701	0.710
B	7.40	7.62	0.291	0.300
C	—	2.65	—	0.104
C1	2.25	2.45	0.090	0.096
D	0.35	0.51	0.014	0.020
E	10.00	10.60	0.394	0.414
F	0.40	0.70	0.016	0.028
G	1.27 BSC		0.050 BSC	
J	0.10	0.25	0.004	0.010
L	0.635 BSC		0.025 BSC	
θ	—	8°	—	8°
V	0.25	0.75	0.010	0.030
W	0.05	0.20	0.002	0.008
X	1.40 REF		0.110 REF	





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