

# SN74S225

## 16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- DC to 10-MHz Data Rate
- 3-State Outputs
- Packaged in Standard Plastic 300-mil DIPs

### description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 easily can be expanded in multiples of 48 words or of 10 bits as shown in Figure 3. The 3-state outputs controlled by a single output-enable ( $\overline{OE}$ ) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently, utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two ways:

- In applications not requiring a gated clock control, best results are achieved by applying the clock input to one of the clocks while tying the other clock input high.
- In applications needing a gated clock, the load clock (gate control) must be high for the FIFO to load on the next clock pulse.

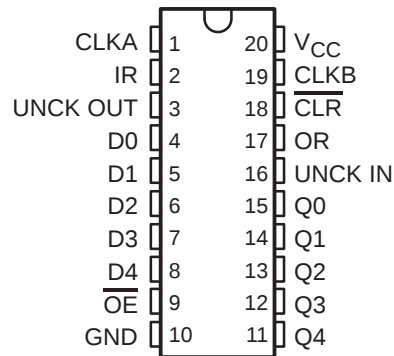
CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state, with a common control input ( $\overline{OE}$ ). When  $\overline{OE}$  is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active. The clear ( $\overline{CLR}$ ) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

The SN74S225 is characterized for operation from 0°C to 70°C.

N PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

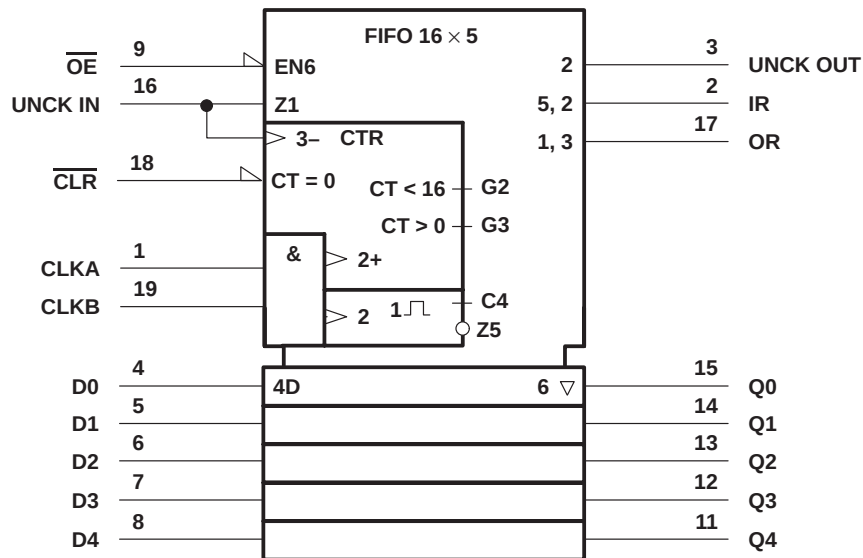
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WITH 3-STATE OUTPUTS

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logic symbol†

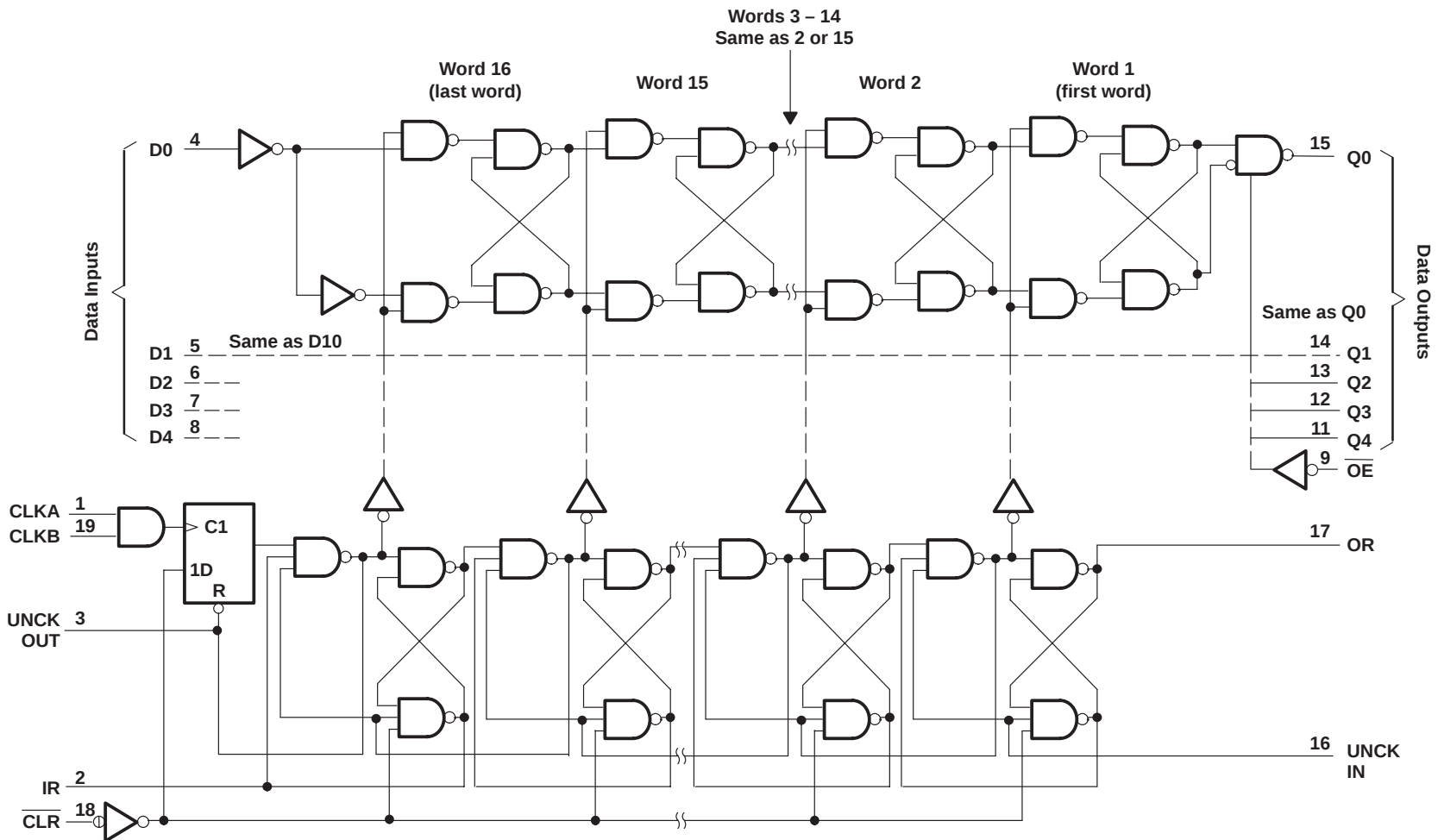


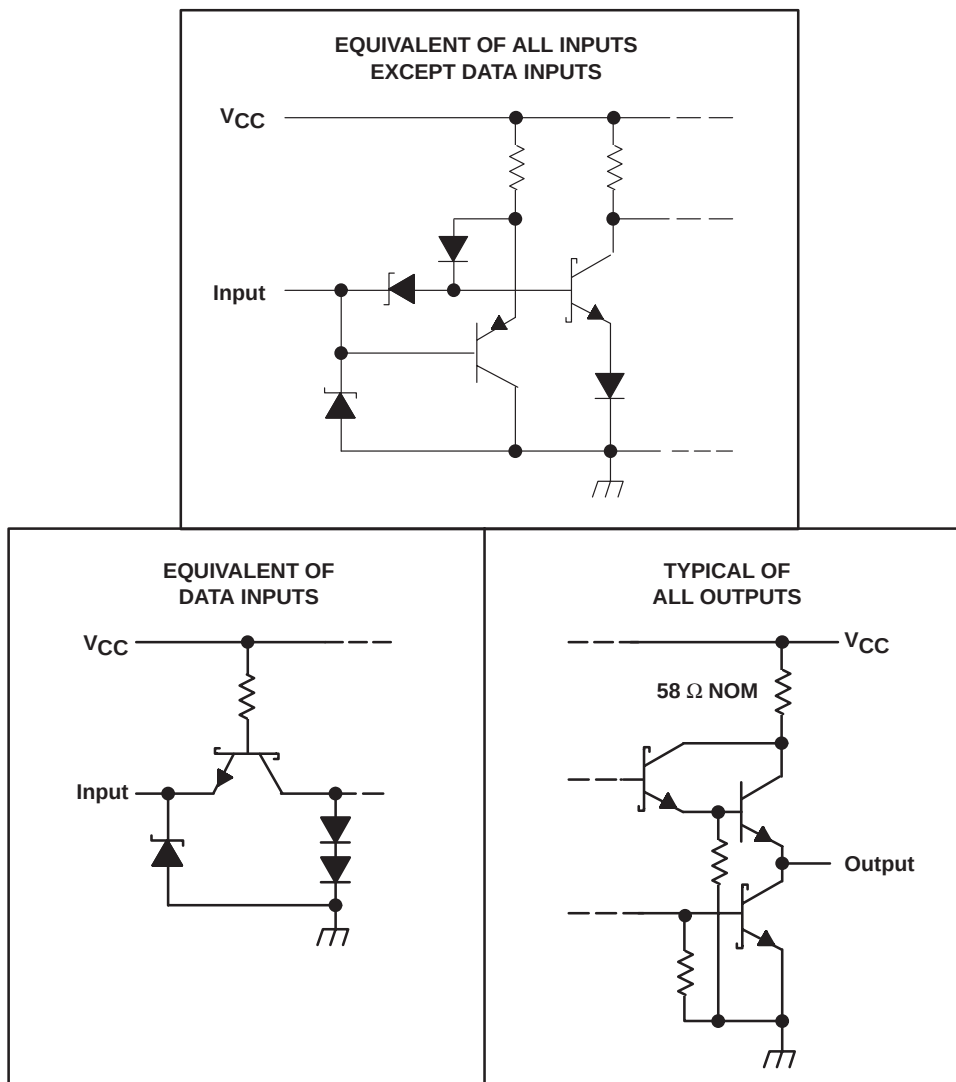
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

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functional block diagram



**schematics of inputs and outputs****absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

|                                                       |                 |
|-------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$ (see Note 1)           | –0.5 V to 7 V   |
| Input voltage range, $V_I$                            | –0.5 V to 5.5 V |
| Off-state output voltage range                        | –0.5 V to 5.5 V |
| Package thermal impedance, $\theta_{JA}$ (see Note 2) | 67°C/W          |
| Storage temperature range, $T_{stg}$                  | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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### recommended operating conditions

|                 |                                | MIN  | NOM | MAX  | UNIT |
|-----------------|--------------------------------|------|-----|------|------|
| V <sub>CC</sub> | Supply voltage                 | 4.75 | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       | 2    |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |      |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current      |      |     | –6.5 | mA   |
|                 |                                |      |     | –3.2 |      |
| I <sub>OL</sub> | Low-level output current       |      |     | 16   | mA   |
|                 |                                |      |     | 8    |      |
| T <sub>A</sub>  | Operating free-air temperature | 0    |     | 70   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                    |            | TEST CONDITIONS           |                           | MIN | TYP <sup>†</sup> | MAX   | UNIT |
|------------------------------|------------|---------------------------|---------------------------|-----|------------------|-------|------|
| V <sub>IK</sub>              |            | V <sub>CC</sub> = 4.75 V, | I <sub>I</sub> = –18 mA   |     |                  | –1.2  | V    |
| V <sub>OH</sub>              | Q outputs  | V <sub>CC</sub> = 4.75 V, | I <sub>OL</sub> = –6.5 mA | 2.4 | 2.9              |       | V    |
|                              | All others | V <sub>CC</sub> = 4.75 V, | I <sub>OL</sub> = –3.2 mA | 2.4 | 2.9              |       |      |
| V <sub>OL</sub>              | Q outputs  | V <sub>CC</sub> = 4.75 V, | I <sub>OL</sub> = 16 mA   |     | 0.35             | 0.5   | V    |
|                              | All others | V <sub>CC</sub> = 4.75 V, | I <sub>OL</sub> = 8 mA    |     | 0.35             | 0.5   |      |
| I <sub>OZH</sub>             |            | V <sub>CC</sub> = 5.25 V, | V <sub>O</sub> = 2.4 V    |     |                  | 50    | μA   |
| I <sub>OZL</sub>             |            | V <sub>CC</sub> = 5.25 V, | V <sub>O</sub> = 0.5 V    |     |                  | –50   | μA   |
| I <sub>I</sub>               |            | V <sub>CC</sub> = 5.25 V, | V <sub>I</sub> = 5.5 V    |     |                  | 1     | mA   |
| I <sub>IH</sub>              | Data       | V <sub>CC</sub> = 5.25 V, | V <sub>I</sub> = 2.7 V    |     |                  | 40    | μA   |
|                              | All others |                           |                           |     |                  | 25    |      |
| I <sub>IL</sub>              | Data       | V <sub>CC</sub> = 5.25 V, | V <sub>I</sub> = 0.5 V    |     |                  | –1    | mA   |
|                              | All others |                           |                           |     |                  | –0.25 |      |
| I <sub>OS</sub> <sup>‡</sup> |            | V <sub>CC</sub> = 5.25 V, | V <sub>O</sub> = 0        | –30 |                  | –100  | mA   |
| I <sub>CC</sub> <sup>§</sup> |            | V <sub>CC</sub> = 5.25 V  |                           |     | 80               | 120   | mA   |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> Duration of the short circuit should not exceed one second.

<sup>§</sup> I<sub>CC</sub> is measured with all inputs grounded and the outputs open.

### timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

|                    |                                  | MIN               | NOM | MAX | UNIT |
|--------------------|----------------------------------|-------------------|-----|-----|------|
| f <sub>clock</sub> | Clock frequency                  |                   |     | 10  | MHz  |
| t <sub>w</sub>     | Pulse duration                   | CLKA or CLKB high | 25  |     | ns   |
|                    |                                  | UNCK IN low       | 7   |     |      |
|                    |                                  | CLR low           | 40  |     |      |
| t <sub>su</sub>    | Setup time before CLKA↑ or CLKB↑ | Data (see Note 3) | –20 |     | ns   |
|                    |                                  | CLR inactive      | 25  |     |      |
| t <sub>h</sub>     | Hold time after CLKA↑ or CLKB↑   |                   | 70  |     | ns   |

NOTE 3: Data must be set up within 20 ns after the load-clock positive transition.



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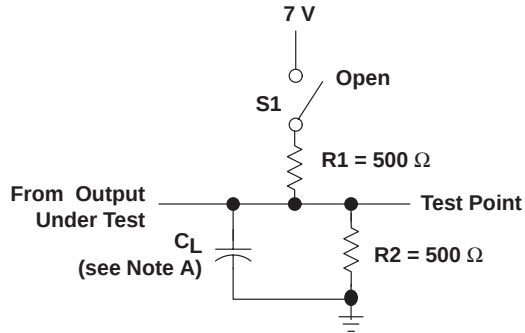
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

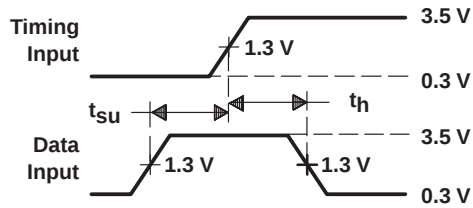
| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS        | MIN | TYP <sup>†</sup> | MAX | UNIT |
|------------------|-----------------|----------------|------------------------|-----|------------------|-----|------|
| f <sub>max</sub> | CLKA            |                | C <sub>L</sub> = 30 pF | 10  | 20               |     | MHz  |
|                  | CLKB            |                |                        | 10  | 20               |     |      |
|                  | UNCK IN         |                |                        | 10  | 20               |     |      |
| t <sub>w</sub>   | UNCK OUT        |                | C <sub>L</sub> = 30 pF | 7   | 14               |     | ns   |
| t <sub>dis</sub> | OE              | Any Q          | C <sub>L</sub> = 5 pF  |     | 10               | 25  | ns   |
| t <sub>en</sub>  | OE              | Any Q          | C <sub>L</sub> = 30 pF |     | 25               | 40  | ns   |
| t <sub>PLH</sub> | UNCK IN         | Any Q          | C <sub>L</sub> = 30 pF |     | 50               | 75  | ns   |
| t <sub>PHL</sub> |                 |                |                        |     | 50               | 75  |      |
| t <sub>PLH</sub> | CLKA or CLKB    | OR             | C <sub>L</sub> = 30 pF |     | 190              | 300 | ns   |
| t <sub>PLH</sub> | UNCK IN         | OR             | C <sub>L</sub> = 30 pF |     | 40               | 60  | ns   |
| t <sub>PHL</sub> |                 |                |                        |     | 30               | 45  |      |
| t <sub>PHL</sub> | CLR             | OR             | C <sub>L</sub> = 30 pF |     | 35               | 60  | ns   |
|                  | CLKA or CLKB    | UNCK OUT       |                        |     | 25               | 45  |      |
|                  | UNCK IN         |                |                        |     | 270              | 400 |      |
|                  | CLKA or CLKB    | IR             |                        |     | 55               | 75  |      |
| t <sub>PLH</sub> | UNCK IN         | IR             | C <sub>L</sub> = 30 pF |     | 255              | 400 | ns   |
|                  | CLR             |                |                        |     | 16               | 35  |      |
|                  | OR↑             | Any Q          |                        |     |                  | 10  |      |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

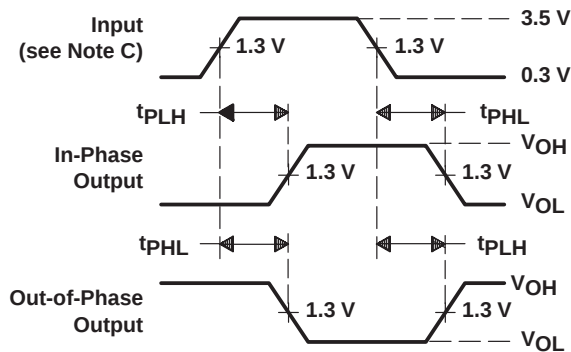
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS

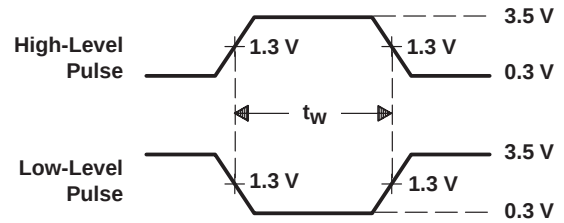


VOLTAGE WAVEFORMS  
SET UP AND HOLD TIMES

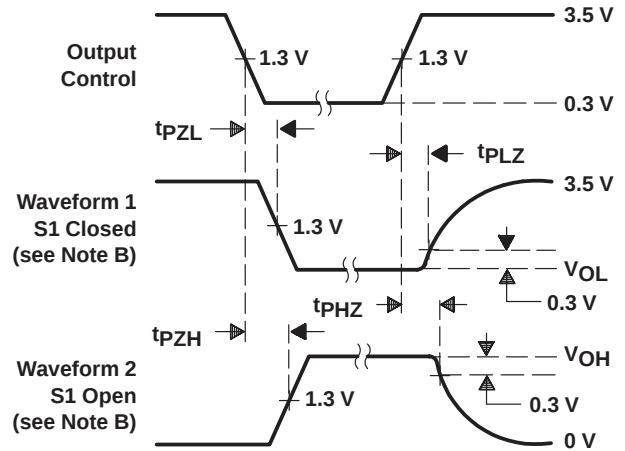


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

| PARAMETER |           | S1     |
|-----------|-----------|--------|
| $t_{en}$  | $t_{PZH}$ | Open   |
|           | $t_{PZL}$ | Closed |
| $t_{dis}$ | $t_{PHZ}$ | Open   |
|           | $t_{PLZ}$ | Closed |
| $t_{pd}$  | $t_{PLH}$ | Open   |
|           | $t_{PHL}$ | Open   |



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

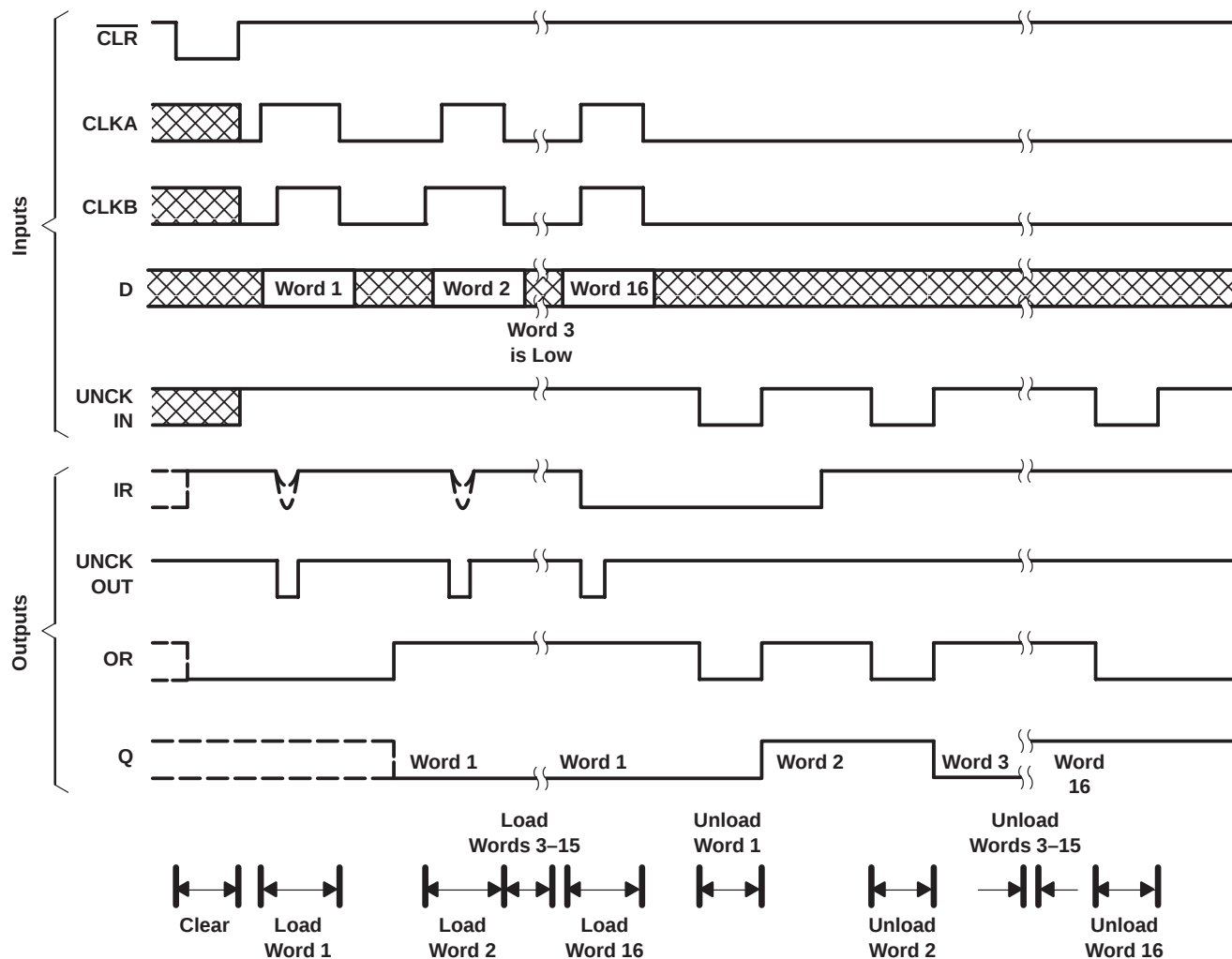


Figure 2. Typical Waveforms for a 16-Word FIFO

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## APPLICATION INFORMATION

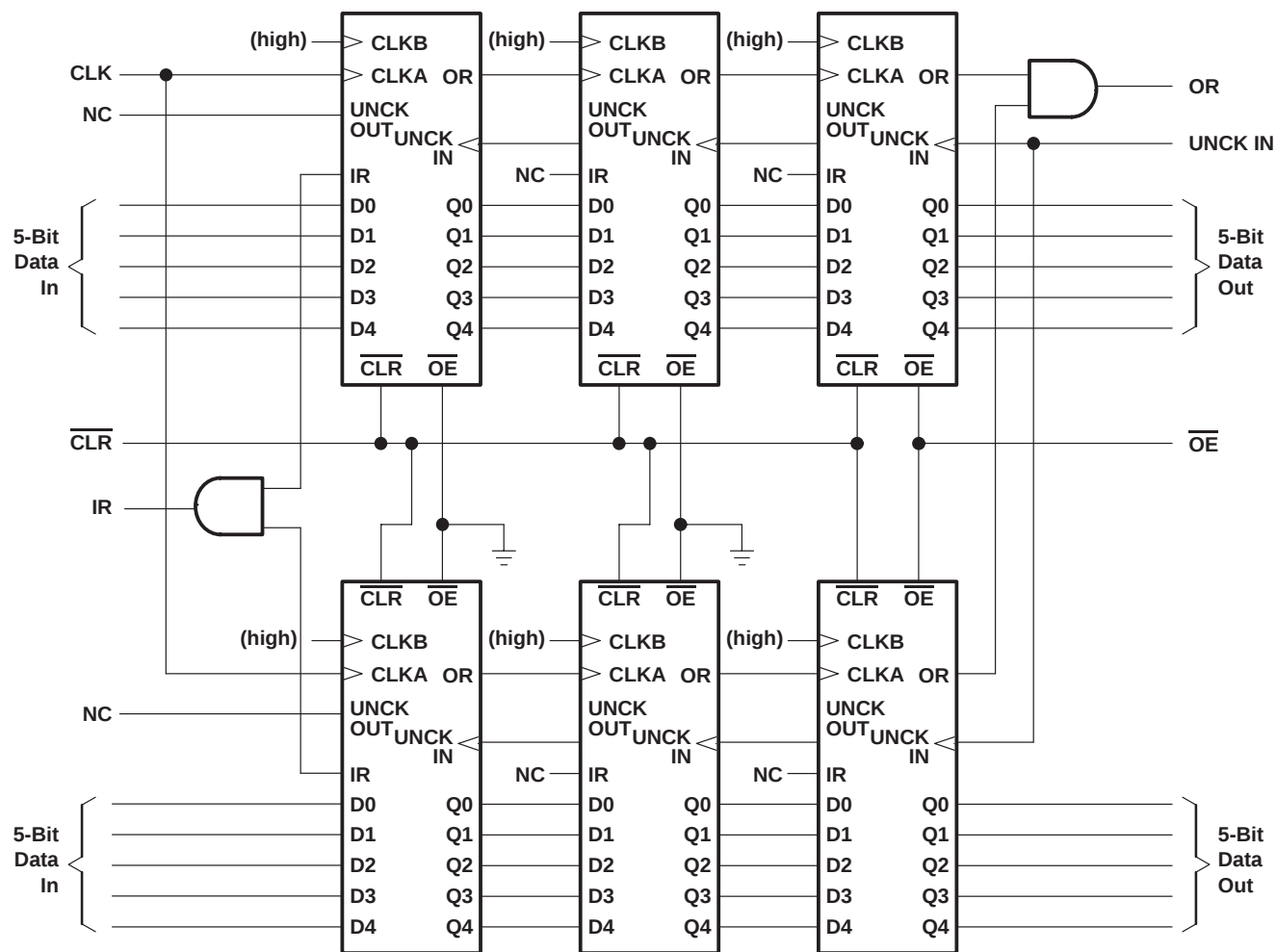


Figure 3. Word-Width Expansion: 48 × 10 Bits

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74S225N        | NRND          | PDIP         | N                  | 20   | 20             | RoHS &<br>Non-Green | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74S225N               |         |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TUBE



\*All dimensions are nominal

| Device    | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74S225N | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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