Description

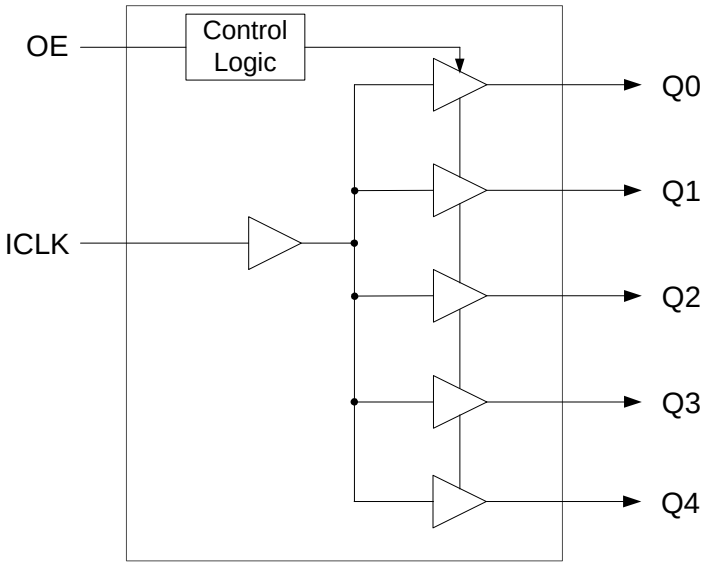
The 5V2305S is a low skew, single input to five output, clock buffer. The 5V2305S has best in class additive phase Jitter of sub 50 fsec.

The 5V2305S also supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in various packages and can operate from a 1.8V to 3.3V supply.

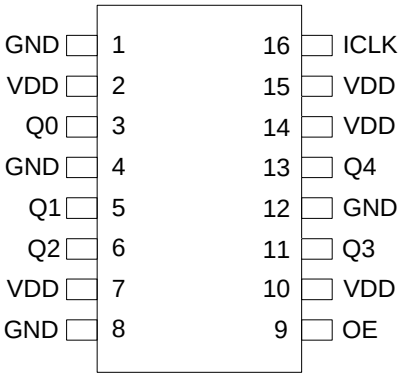
Features

- Extremely low RMS Additive Phase Jitter: 50fs
- Low output skew: 20ps
- Packaged in 16-pin TSSOP and small 2mm x 2mm 10-pin DFN
- Pb (lead) free package
- Low power CMOS technology
- Operating voltages of 1.8V to 3.3V
- Extended temperature range (-40°C to +105°C)

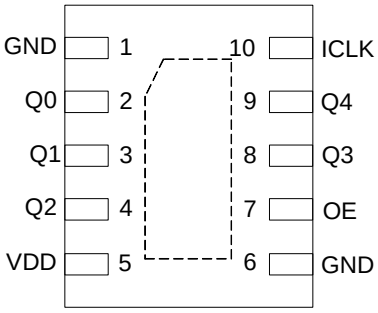
Block Diagram



Pin Assignments



16-pin (173 mil) TSSOP



10-pin DFN (2x2mm)

Pin Descriptions

Pin Name	Pin Number		Pin Type	Pin Description
	16-pin TSSOP	10-pin DFN		
VDD	2, 7, 10, 14, 15	5	Power	DC power supply. Connect to 1.8V to 3.3V.
GND	1, 4, 8, 12	1, 6	Power	Power supply ground.
ICLK	16	10	Input	Reference input clock.
Q0	3	2	Output	Clock Output 0. Same frequency as CLKIN.
Q1	5	3	Output	Clock Output 1. Same frequency as CLKIN.
Q2	6	4	Output	Clock Output 2. Same frequency as CLKIN.
Q3	11	8	Output	Clock Output 3. Same frequency as CLKIN.
Q4	13	9	Output	Clock Output 4. Same frequency as CLKIN.
OE	9	7	Input	Active High Output Enable pin. When this pin is high, all outputs are enabled and active. When this pin is low, all outputs are driven low.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD on pin 2 and GND on pin 4, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 5V2305S is capable of, careful attention must be paid to board layout. Essentially, all five outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5V2305S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (extended)	-40° to +105°C
Storage Temperature	-65° to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7 x VDD		1.89	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage. OE	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, OE	V_{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V_{OH}	I_{OH} = -10 mA	1.3			V
Output Low Voltage	V_{OL}	I_{OL} = 10mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		18		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7 x VDD		2.625	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage. OE	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, OE	V_{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	1.8			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		25		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7 x VDD		3.465	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage. OE	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, OE	V_{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.2			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		30		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, C_L=5 pF		0.6	1.0	ns
Output Enable Time	t_{EN}	C_L < 5 pF			3	cycles
Output Disable Time	t_{DIS}	C_L < 5 pF			3	cycles
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		135MHz, Note 1	1.5	2.2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		20	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

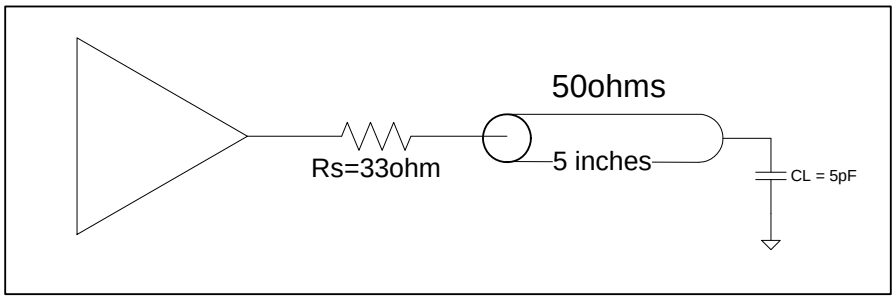
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, C_L=5 pF		0.6	1.0	ns
Output Enable Time	t_{EN}	C_L < 5 pF			3	cycles
Output Disable Time	t_{DIS}	C_L < 5 pF			3	cycles
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		135MHz, Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		20	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, C_L=5 pF		0.6	1.0	ns
Output Enable Time	t_{EN}	C_L < 5 pF			3	cycles
Output Disable Time	t_{DIS}	C_L < 5 pF			3	cycles
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		135MHz, Note 1	1.5	2.1	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		20	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

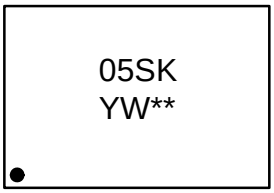
Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Test Load and Circuit



Marking Diagrams

16-pin TSSOP

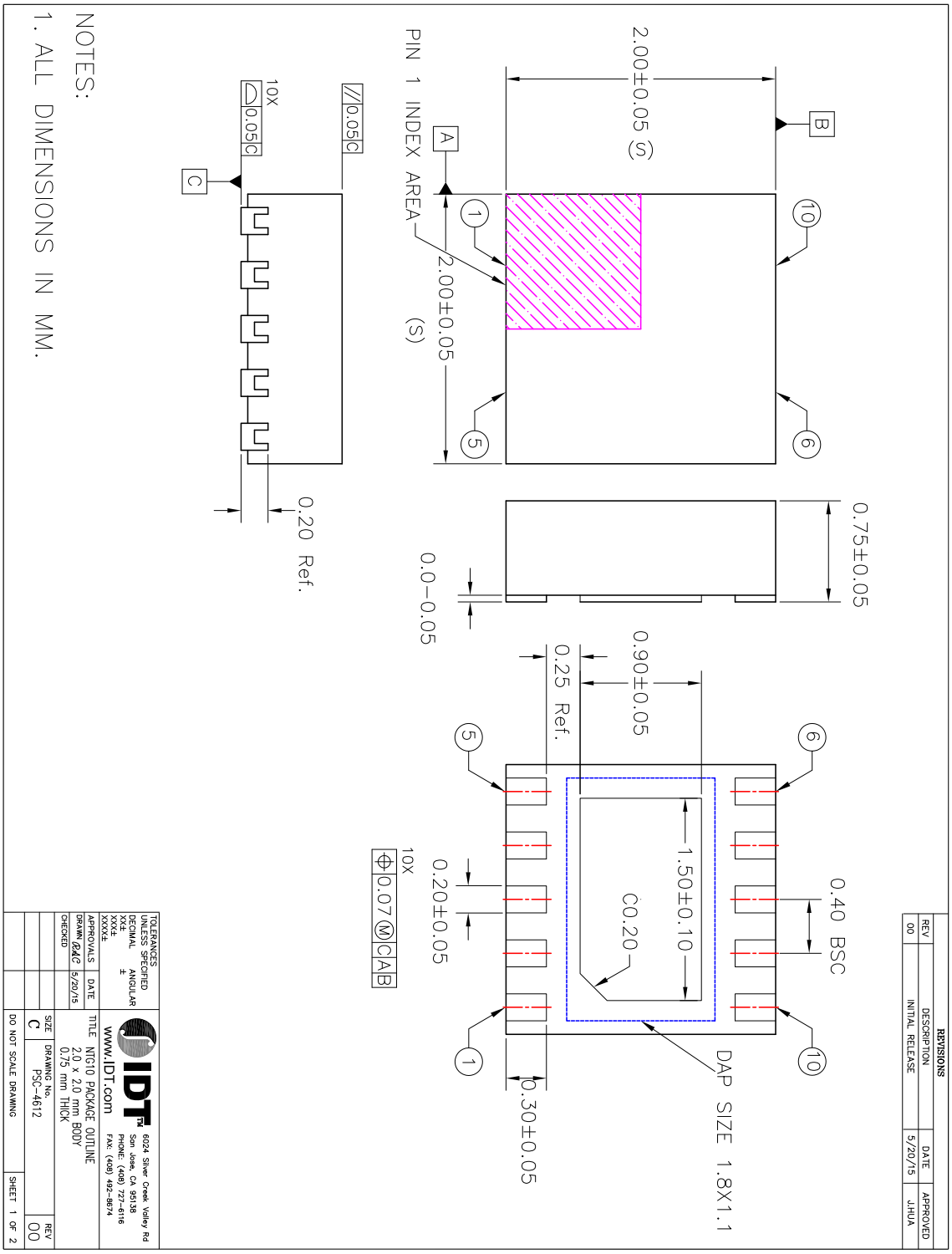


10-pin DFN

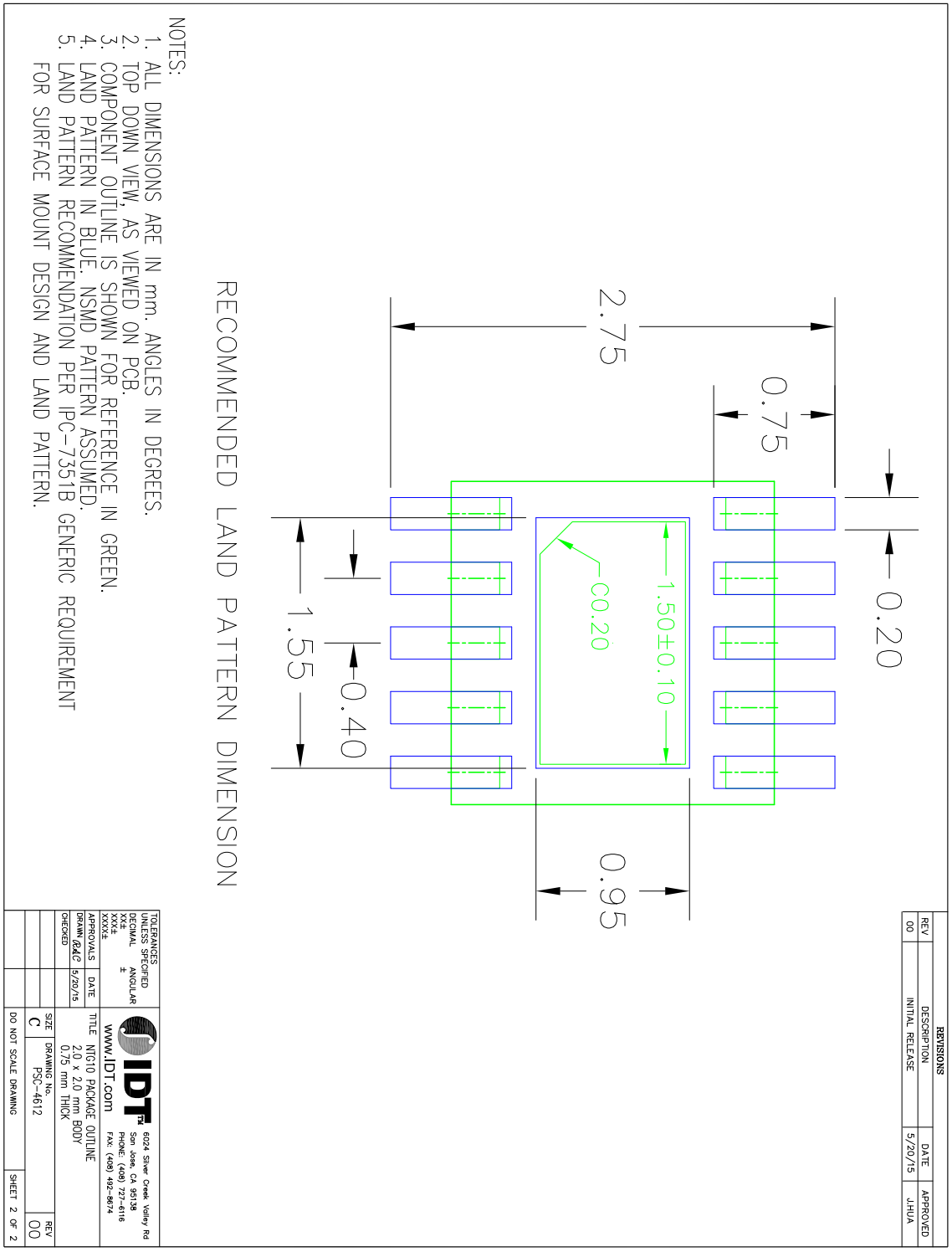
Notes:

1. "**" is the lot number.
2. "YYWW" or "YW" are the last digits of the year and week that the part was assembled.
3 "G" denotes RoHS compliant package.
4. "$" denotes mark code.
5. "K" denotes extended temperature range device.

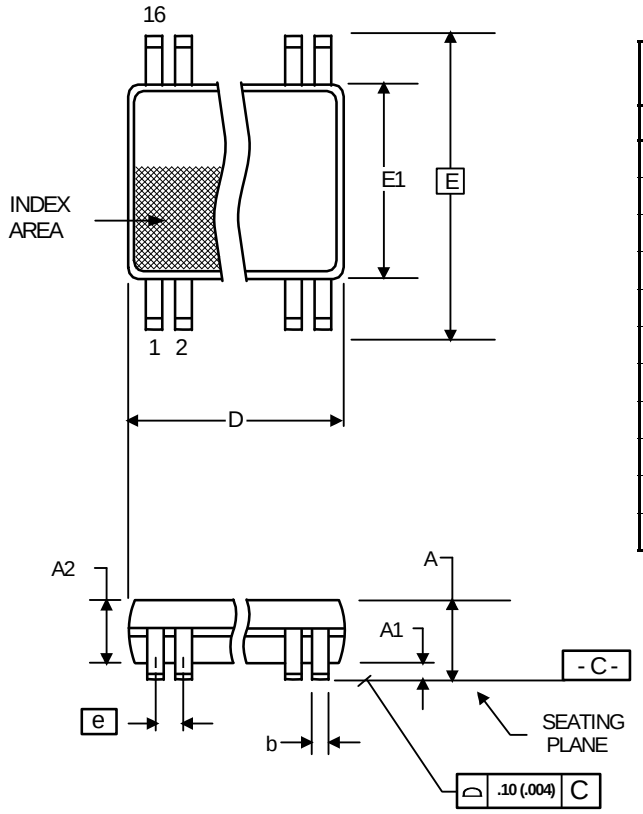
Package Outline and Package Dimensions (10-pin DFN, 2x2mm)



Package Outline and Package Dimensions (10-pin DFN, 2x2mm), cont.



Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Body)



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	1.20	—	.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V2305SPGGK	see page 6	Tubes	16-pin TSSOP	-40° to +105°C
5V2305SPGGK8		Tape and Reel	16-pin TSSOP	-40° to +105°C
5V2305SNTGK		Cut Tape	10-pin DFN	-40° to +105°C
5V2305SNTGK8		Tape and Reel	10-pin DFN	-40° to +105°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Date	Originator	Description of Change
August 1, 2016	H.G.	Updated typical values for propagation delay and output to output skew.
July 11, 2016	H.G.	Release to final.

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