FAIRCHILD SEMICONDUCTOR®

October 2013

FQD13N06L / FQU13N06L

N-Channel QFET® MOSFET

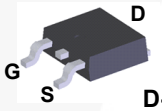
60 V, 11 A, 115 mΩ

Description

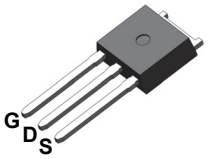
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

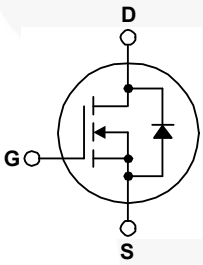
- 11 A, 60 V, $R_{DS(on)}$ = 115 mΩ (Max) @ V_{GS} = 10 V, I_D = 5.5 A
- Low Gate Charge (Typ. 4.8 nC)
- Low Crss (Typ. 17 pF)
- 100% Avalanche Tested
- Low Level Gate Drive Requirements Allowing Direct Operation form Logic Drivers



D-PAK



I-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQD13N06LTM / FQU13N06LTU FQU13N06LTU_WS	Unit
V_{DSS}	Drain-Source Voltage		60	V
I_D	Drain Current - Continuous (T_C = 25°C)		11	A
	- Continuous (T_C = 100°C)		7	A
I_{DM}	Drain Current - Pulsed	(Note 1)	44	A
V_{GSS}	Gate-Source Voltage		± 20	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	90	mJ
I_{AR}	Avalanche Current	(Note 1)	11	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		28	W
	- Derate above 25°C		0.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQD13N06LTM FQU13N06LTU FQU13N06LTU_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2-oz Copper), Max.	50	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD13N06LTM	FQD13N06L	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU13N06LTU	FQU13N06L	I-PAK	Tube	N/A	N/A	70 units
FQU13N06LTU_WS	FQU13N06LS	I-PAK	Tube	N/A	N/A	75 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.05	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 48 V, T_C = 150°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5.5 A	--	0.092	0.115	Ω
		V_{GS} = 5 V, I_D = 5.5 A	--	0.115	0.145	
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 5.5 A	--	6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	270	350	pF
C_{oss}	Output Capacitance		--	95	125	pF
C_{rss}	Reverse Transfer Capacitance		--	17	23	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 6.8 A, R_G = 25 Ω (Note 4)	--	8	25	ns
t_r	Turn-On Rise Time		--	90	190	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 13.6 A, V_{GS} = 5 V (Note 4)	--	4.8	6.4	nC
Q_{gs}	Gate-Source Charge		--	1.6	--	nC
Q_{gd}	Gate-Drain Charge		--	2.7	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	44	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 11 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 13.6 A, dI_F / dt = 100 A/μs	--	45	--	ns
Q_{rr}	Reverse Recovery Charge		--	45	--	nC

Notes:
1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 870 μH, I_{AS} = 11 A, V_{DD} = 25 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 13.6 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

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Typical Characteristics

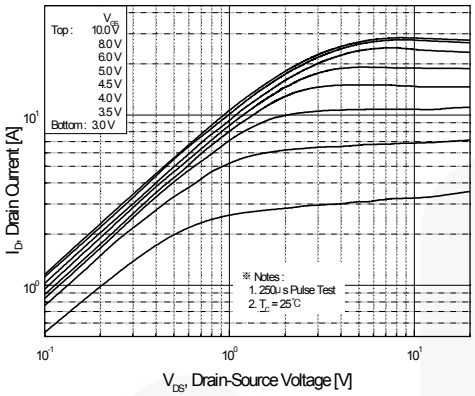


Figure 1. On-Region Characteristics

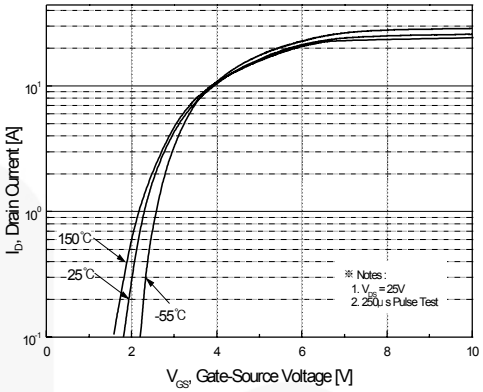


Figure 2. Transfer Characteristics

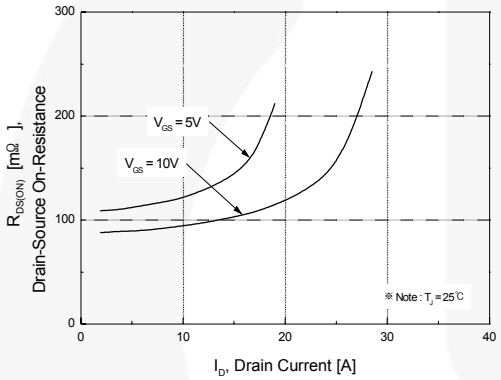


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

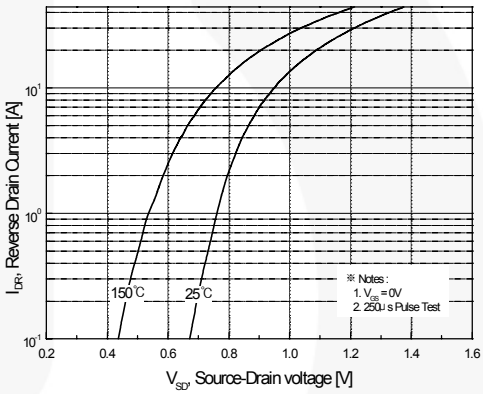


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

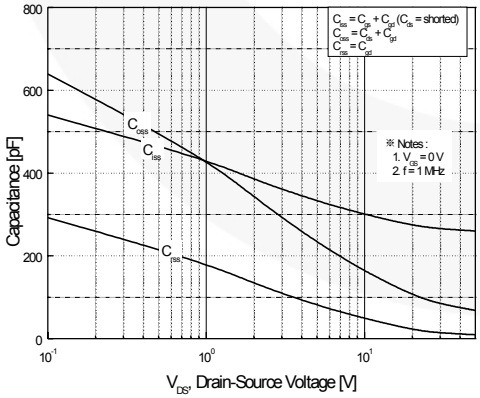


Figure 5. Capacitance Characteristics

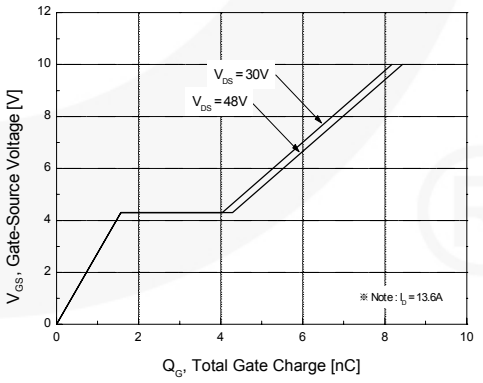


Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

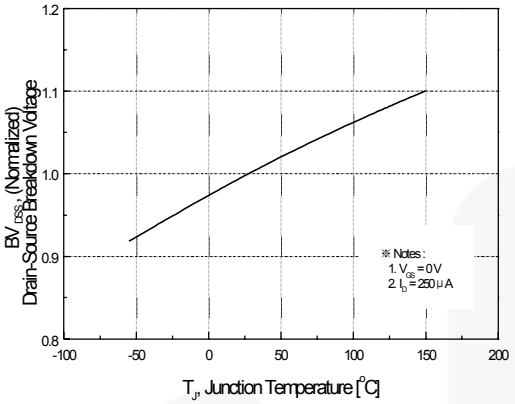


Figure 7. Breakdown Voltage Variation vs. Temperature

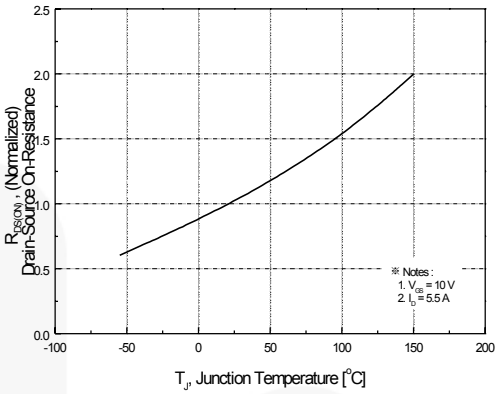


Figure 8. On-Resistance Variation vs. Temperature

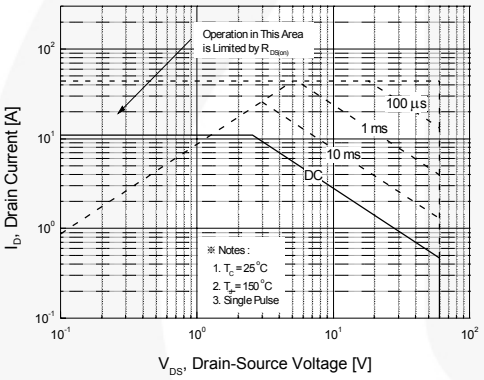


Figure 9. Maximum Safe Operating Area

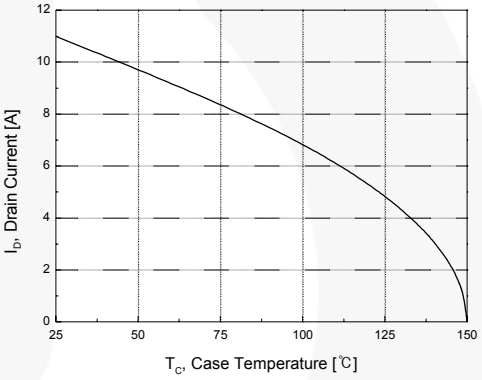


Figure 10. Maximum Drain Current vs. Case Temperature

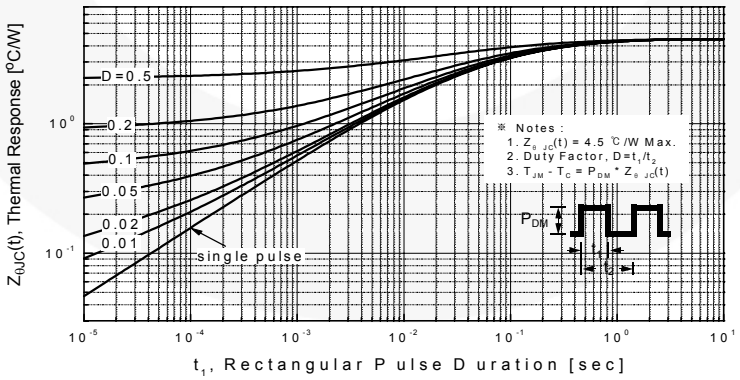


Figure 11. Transient Thermal Response Curve

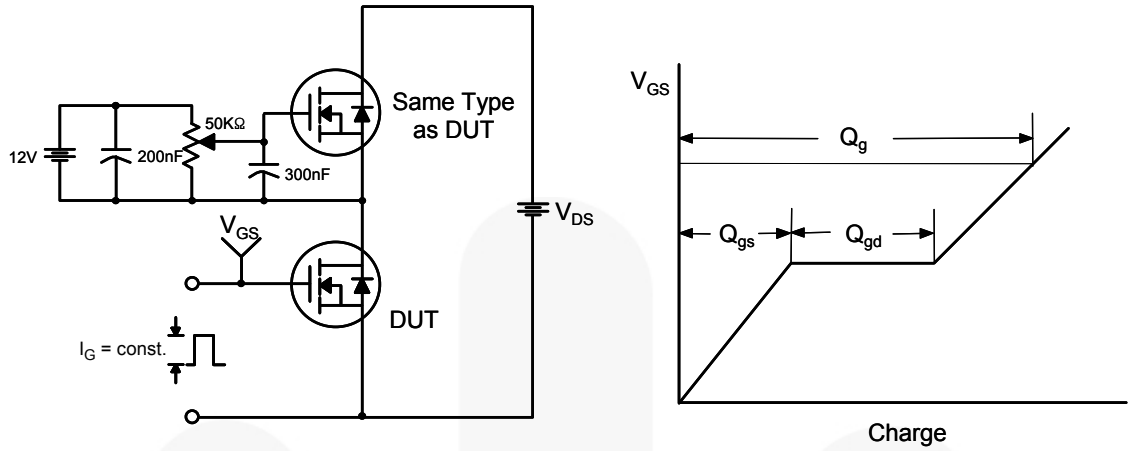


Figure 12. Gate Charge Test Circuit & Waveform

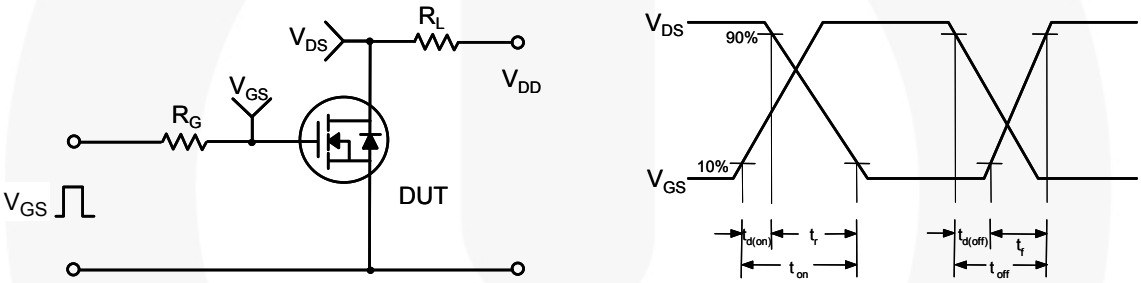


Figure 13. Resistive Switching Test Circuit & Waveforms

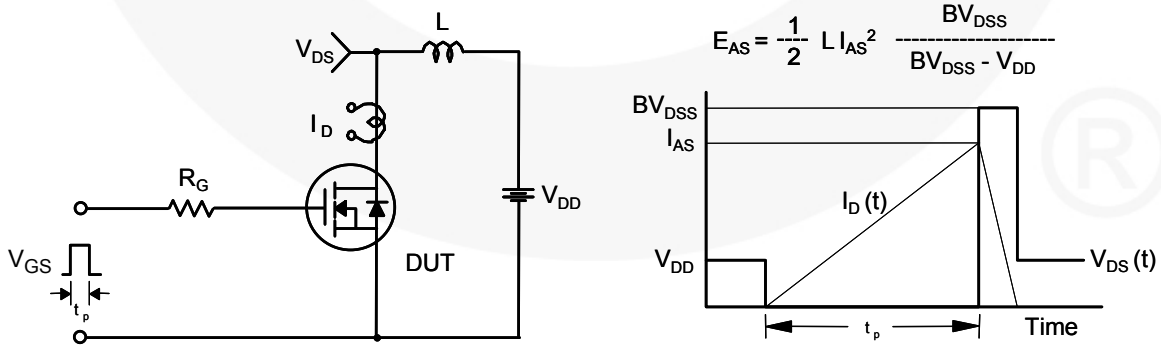


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

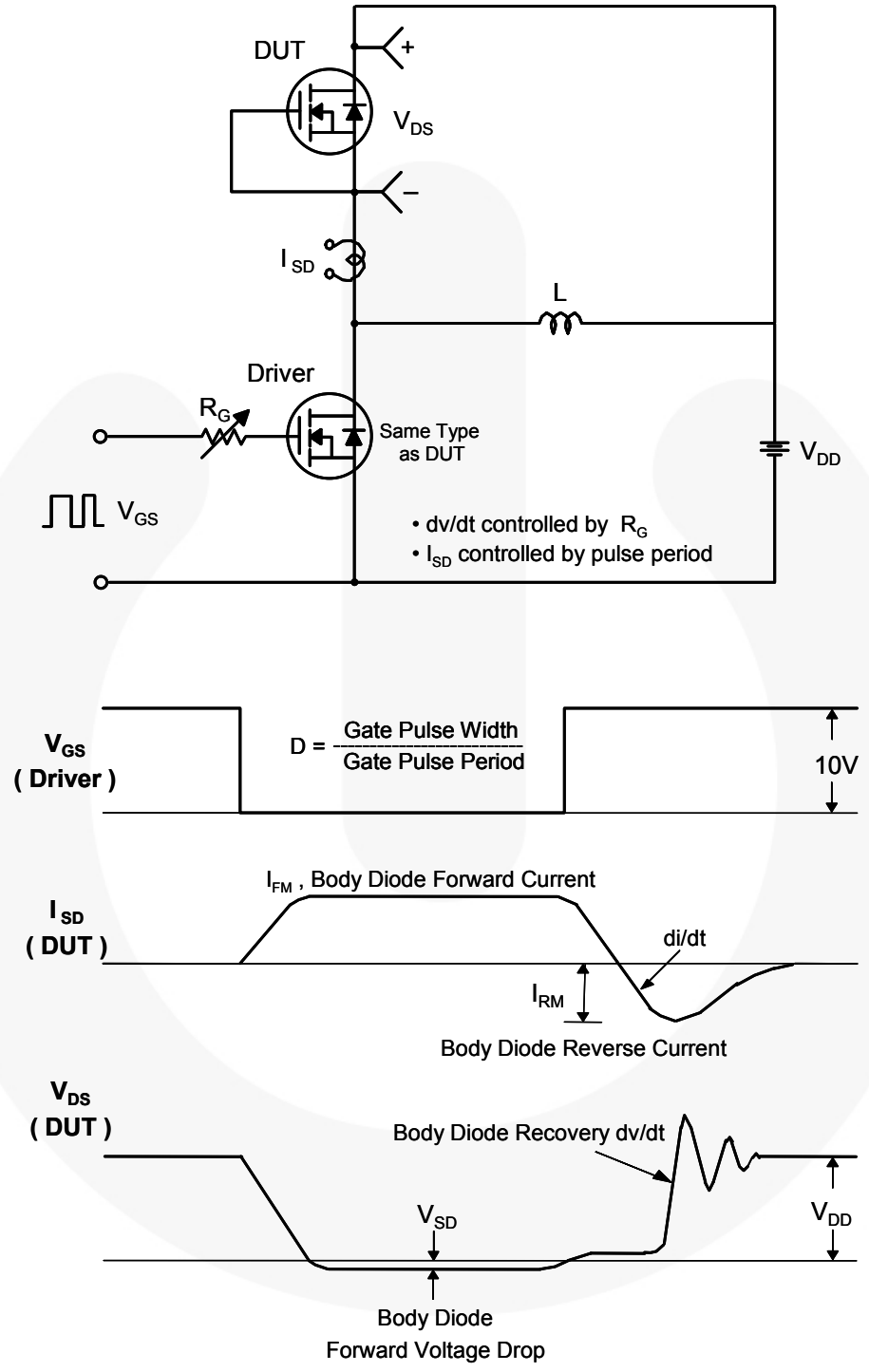
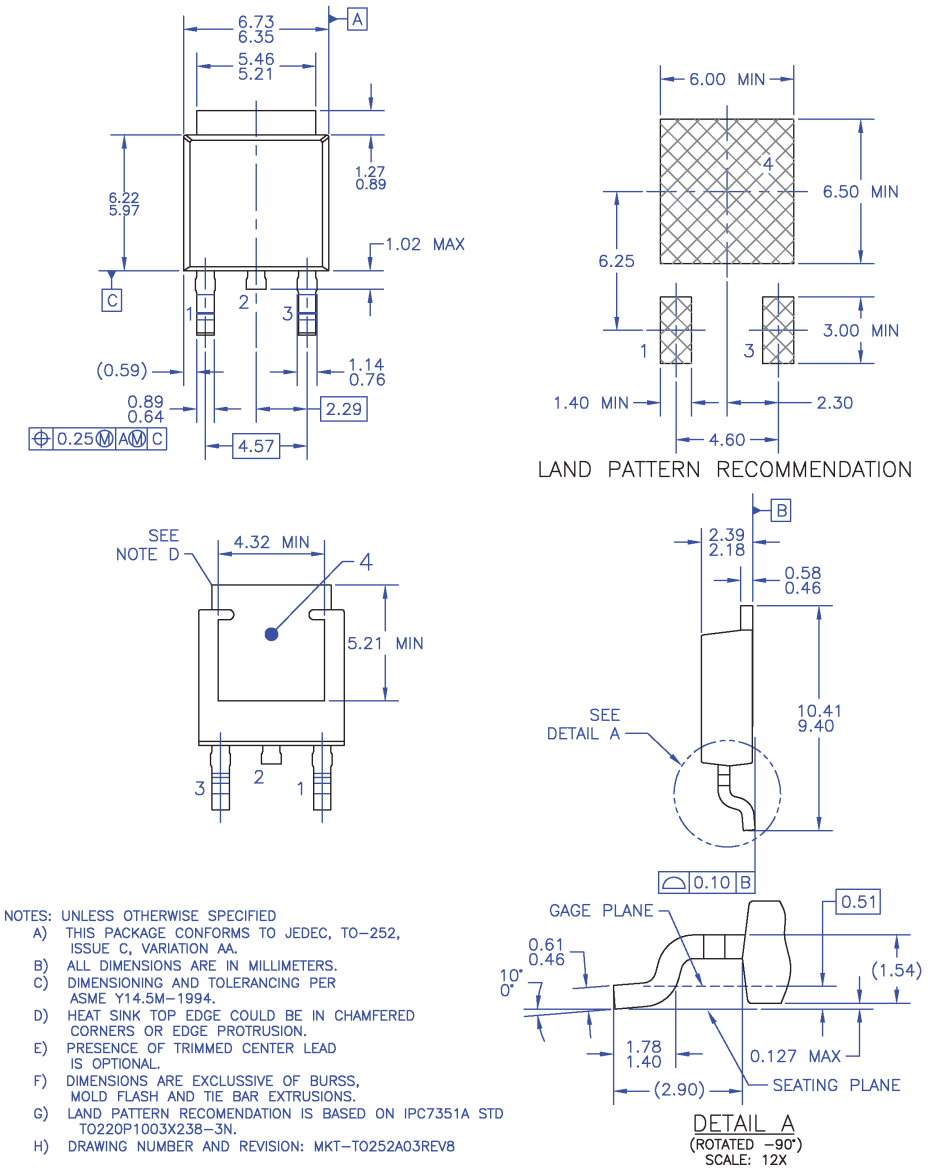


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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Mechanical Dimensions

FQU13N06LTU

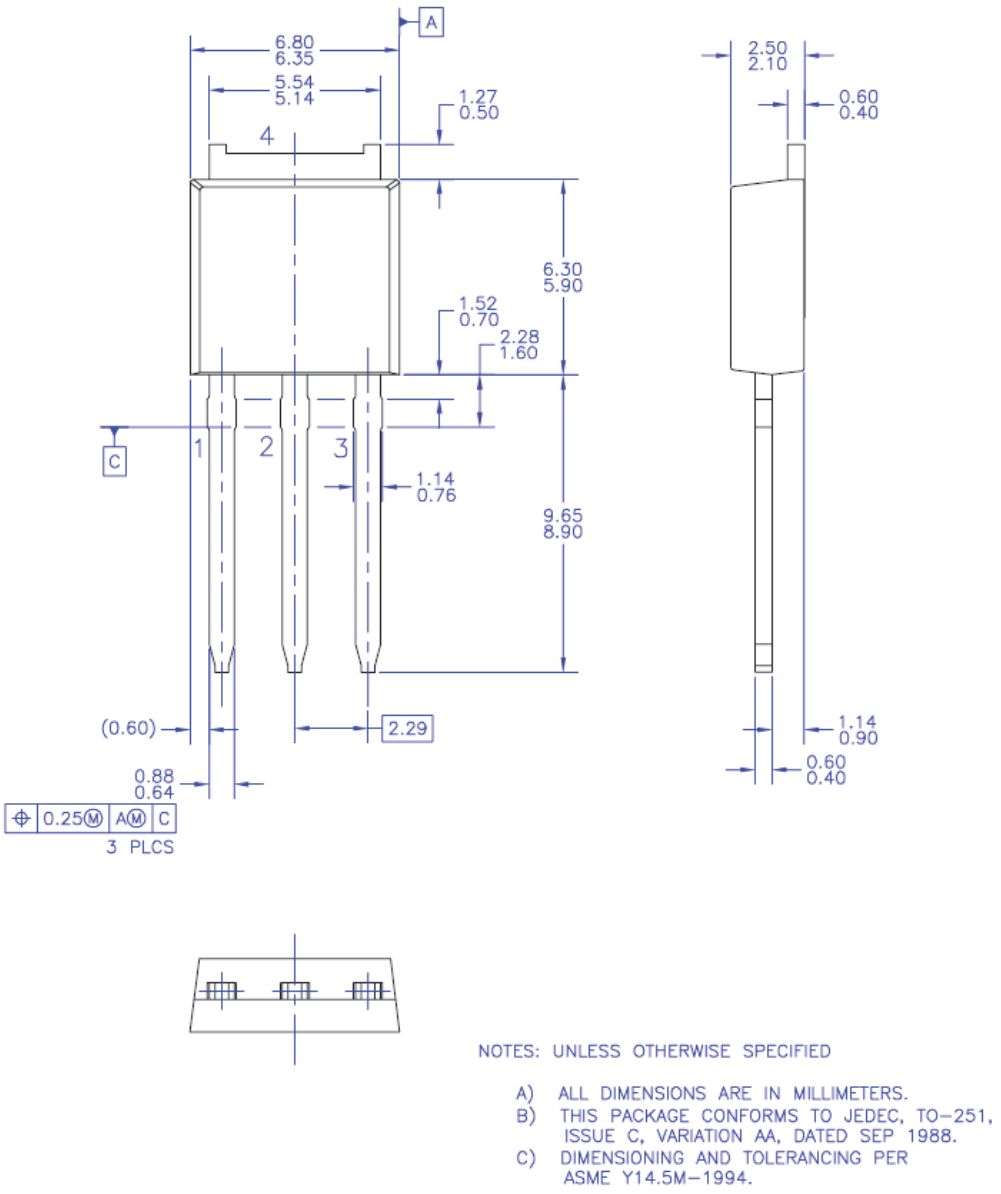


Figure 17. TO251 (I-PAK), Molded, 3-Lead

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Mechanical Dimensions

FQU13N06LTU_WS

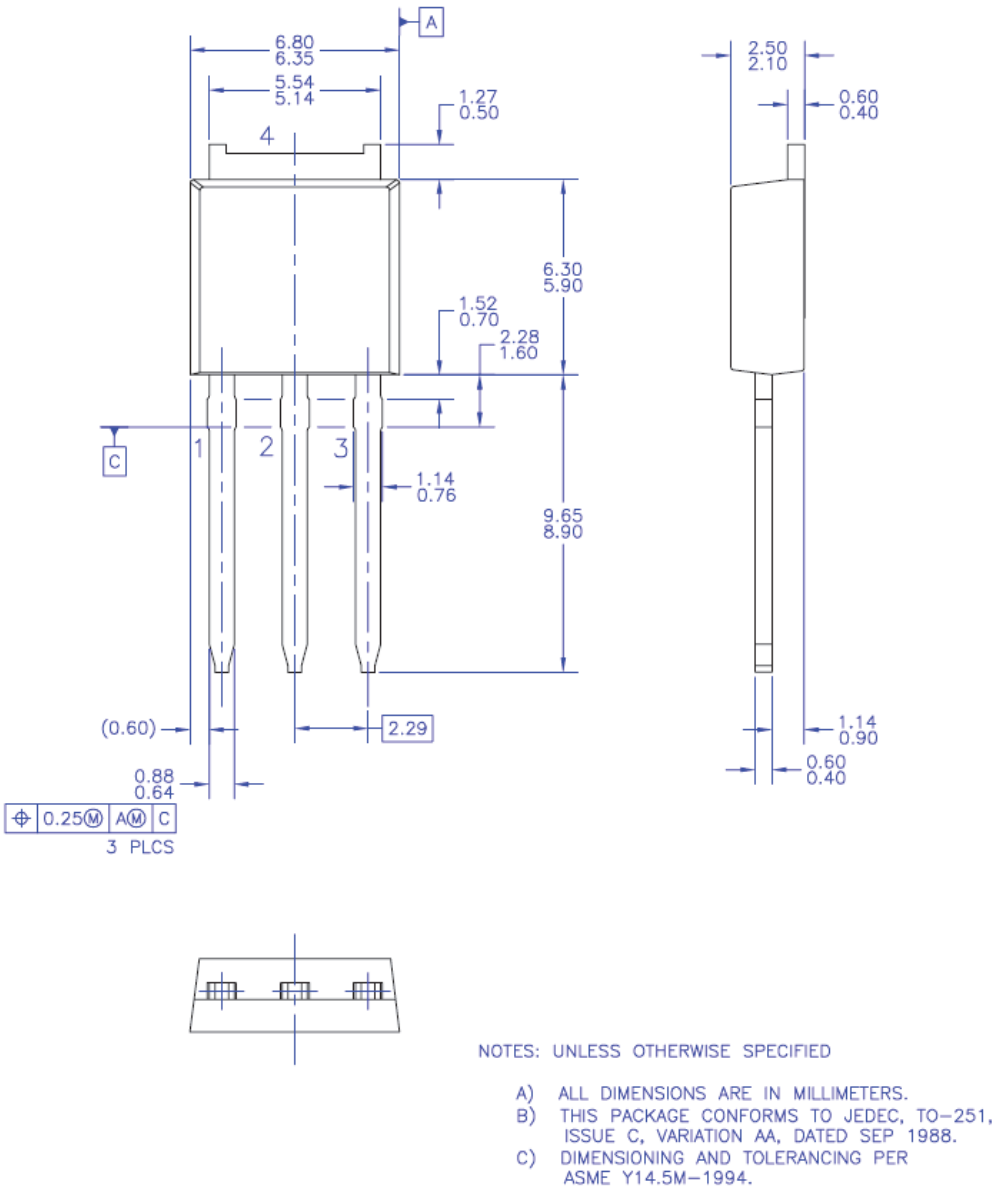


Figure 18. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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