

BSS84L, BVSS84L

Power MOSFET Single P-Channel SOT-23 -50 V, 10 Ω

- SOT-23 Surface Mount Package Saves Board Space
- AEC Q101 Qualified and PPAP Capable – BVSS84L
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	50	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Drain Current Continuous @ $T_A = 25^\circ\text{C}$ Pulsed Drain Current ($t_p \leq 10 \mu\text{s}$)	I_D I_{DM}	130 520	mA
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	$^\circ\text{C}$

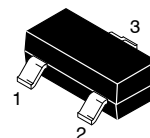
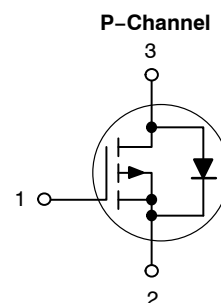
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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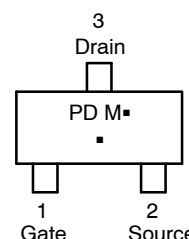
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$
-50 V	10 Ω @ 10 V



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM & PIN ASSIGNMENT



PD = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BSS84LT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
BVSS84LT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = -250\text{ }\mu\text{Adc}$)	$V_{(BR)DSS}$	-50	-	-	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = -25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = -50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = -50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	- - -	- - -	-0.1 -15 -60	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	± 10	nAdc

ON CHARACTERISTICS (Note 1)

Gate-Source Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$)	$V_{GS(th)}$	-0.9	-	-2.0	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = -5.0\text{ Vdc}$, $I_D = -100\text{ mAdc}$)	$R_{DS(on)}$	-	4.7	10	Ω
Transfer Admittance ($V_{DS} = -25\text{ Vdc}$, $I_D = -100\text{ mAdc}$, $f = 1.0\text{ kHz}$)	$ Y_{fs} $	50	-	-	mS

DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 5.0\text{ Vdc}$	C_{iss}	-	36	-	pF
Output Capacitance	$V_{DS} = 5.0\text{ Vdc}$	C_{oss}	-	17	-	
Transfer Capacitance	$V_{DG} = 5.0\text{ Vdc}$	C_{rss}	-	6.5	-	

SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	$V_{DD} = -15\text{ Vdc}$, $I_D = -2.5\text{ Adc}$, $R_L = 50\text{ }\Omega$	$t_{d(on)}$	-	3.6	-	ns
Rise Time		t_r	-	9.7	-	
Turn-Off Delay Time		$t_{d(off)}$	-	12	-	
Fall Time		t_f	-	1.7	-	
Gate Charge	$V_{DD} = -40\text{ Vdc}$, $I_D = -0.5\text{ A}$, $V_{GS} = -10\text{ V}$	Q_T	-	2.2	-	nC

SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Current		I_S	-	-	-0.130	A
Pulsed Current		I_{SM}	-	-	-0.520	
Forward Voltage (Note 2)	$V_{GS} = 0\text{ V}$, $I_S = -130\text{ mA}$	V_{SD}	-	-	-2.2	V

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
2. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

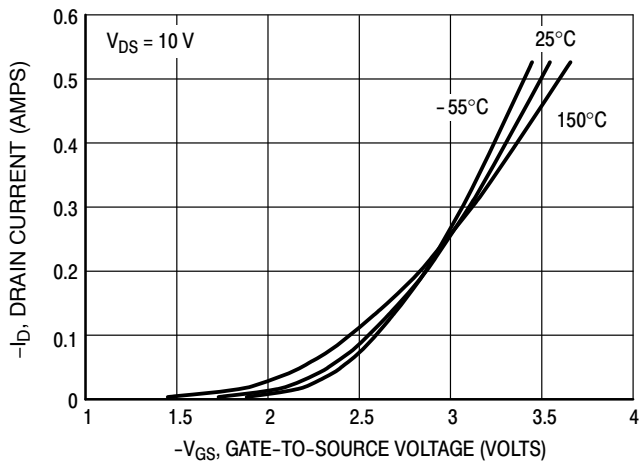


Figure 1. Transfer Characteristics

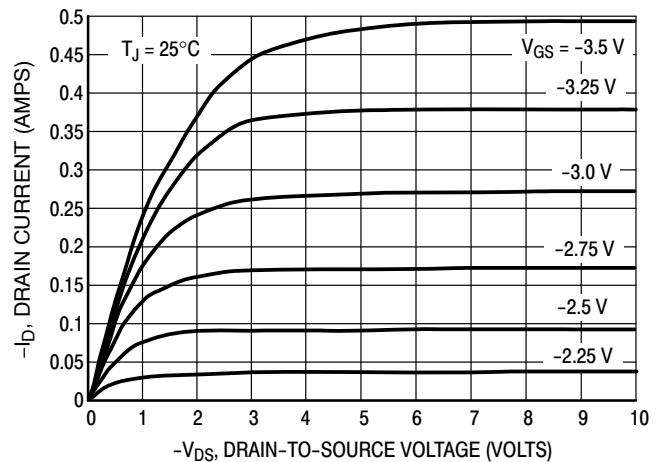


Figure 2. On-Region Characteristics

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TYPICAL ELECTRICAL CHARACTERISTICS

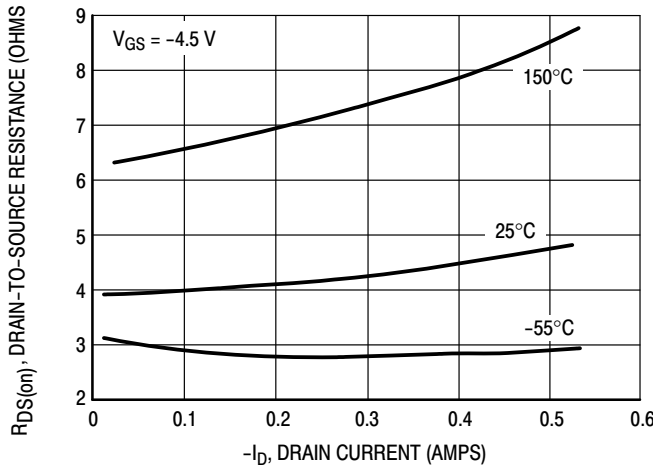


Figure 3. On-Resistance versus Drain Current

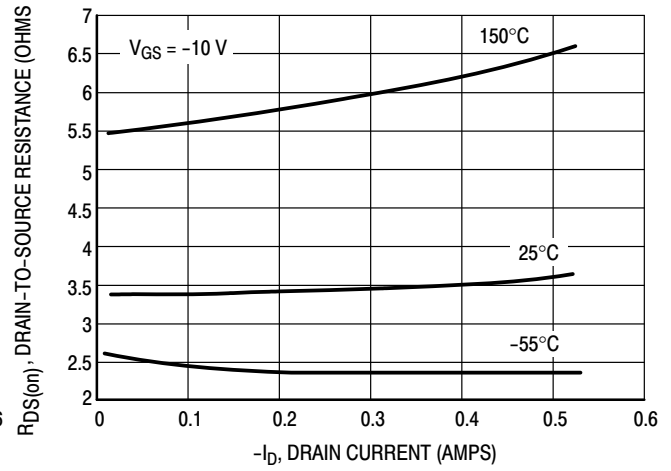


Figure 4. On-Resistance versus Drain Current

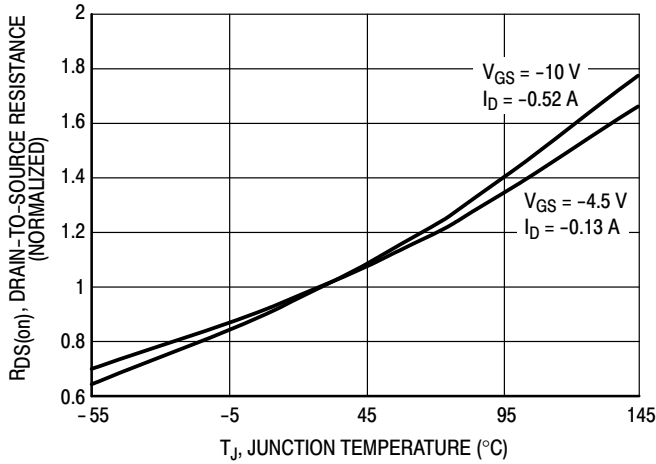


Figure 5. On-Resistance Variation with Temperature

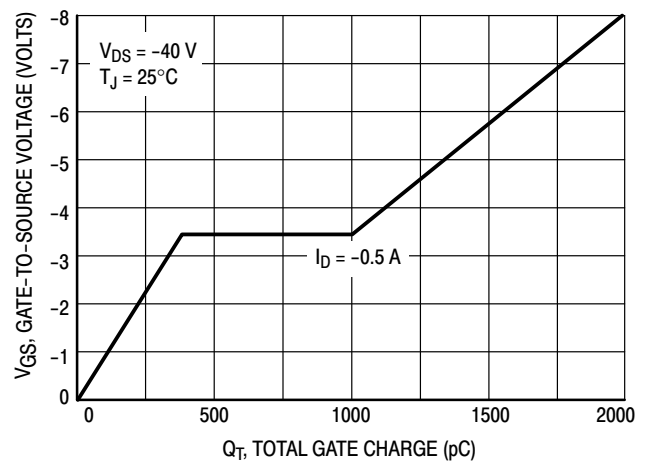


Figure 6. Gate Charge

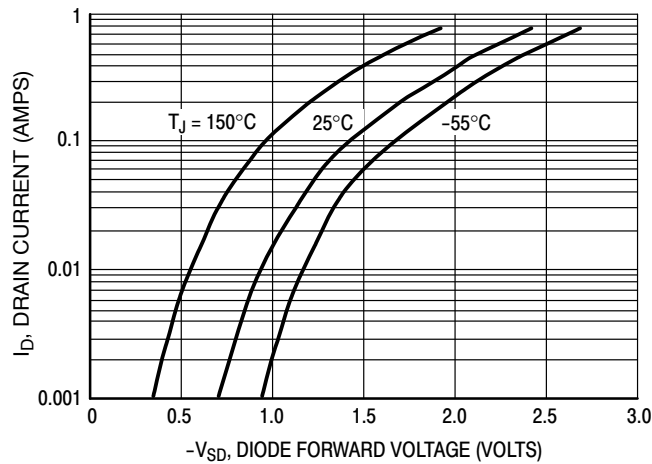
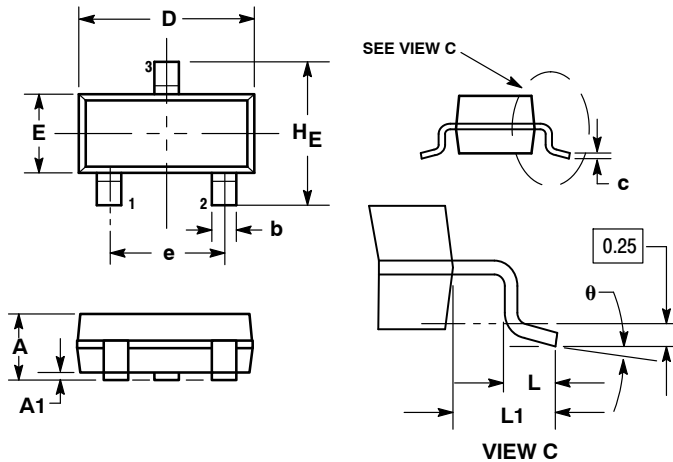


Figure 7. Body Diode Forward Voltage

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PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AP

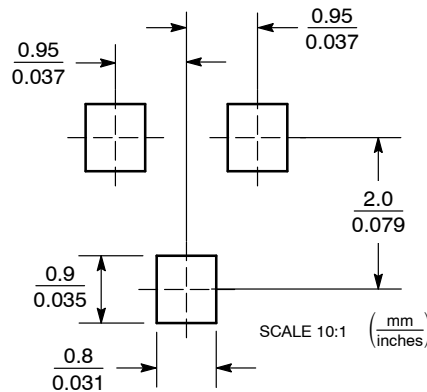


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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