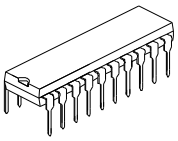
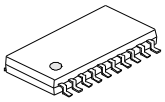
2-CH OUTPUT STEREO AUDIO PROCESSOR

DESCRIPTION

The SC7315 is a volume, tone (bass and treble), balance (left/ right) and fader processor for quality audio applications in car radio and Hi-Fi systems. Selectable input gain and external loudness function are provided. Control is accomplished by serial I^2C bus microprocessor interface. The AC signal settings is obtained by resistor networks and switches combined with operational amplifiers. Due to the Used CMOS technology, low distortion, low noise and low DC stepping are obtained.



DIP-20-300-2.54



SOP-20-375-1.27

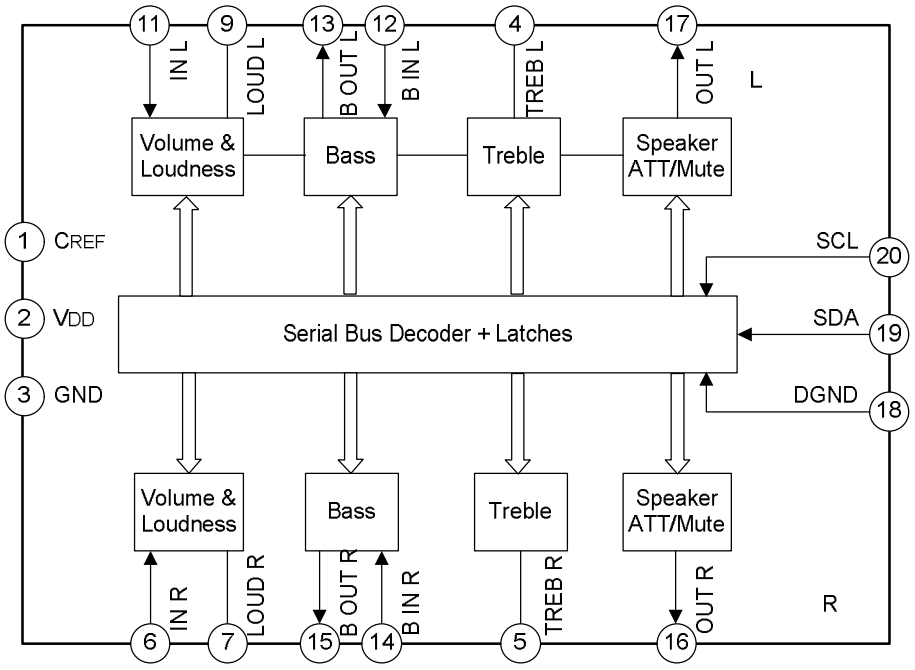
FEATURES

* 2 stereo inputs
* Two speaker attenuators:
  --2 independent speakers control in 1.25dB steps for balance and fader facilities
  --Independent mute function
* All functions programmable via serial I^2C Bus
* Loudness function
* Volume control in 1.25dB steps
* Treble and bass control
* Input and output for external equalizer ornoise reduction system

ORDERING INFORMATION

Device	Package
SC7315	DIP-20-300-2.54
SC7315S	SOP-20-375-1.27

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Characteristics	Symbol	Ratings	Unit
Supply Voltage	V_S	10.2	V
Operating Temperature	T_{amb}	-40 ~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

QUICK REFERENCE DATA

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_S	6	9	10	V
Maximum Input Signal Handling	V_{CL}	2			V_{rms}
Total Harmonic Distortion ,V=1Vrms, f=1kHz	THD		0.01	0.1	%
Signal to Noise Ratio	S/N		106		dB
Channel Separation, f=1kHz	SC		103		dB
Volume Control, 1.25dB Step		-78.75		0	dB
Bass and Treble Control, 2dB step		-14		+14	dB
Fader and Balance Control, 1.25dB step		-38.75		0	dB
Input Gain, 3.75dB Step		0		11.25	dB
Mute Attenuation			100		dB

ELECTRICAL CHARACTERISTICS (Refer to the test circuit)

(Tamb=25°C, VS=9.0V,RL=10kΩ，RG=600Ω，all controls flat(G=0), f=1kHz,Unless otherwise specified)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
Operating Supply Voltage	V_S		6	9	10.0	V
Operating Supply Current	I_S			20.0	35.0	mA
Ripple Rejection of Supply Voltage	S_{VR}		60	80		dB
VOLUME CONTROL						
Input Resistance	R_{IV}		20	33	50	kΩ
Control Range	C_{range}		70	75	80	dB
Minimum Attenuation	$A_{V(min)}$		-1	0	1	dB
Maximum Attenuation	$A_{V(max)}$		70	75	80	dB
Step Resolution	A_{STEP}		0.5	1.25	1.75	dB
Attenuation Set Error	EA	A_V=0 to –20dB	-1.25	0	1.25	dB
		A_V=-20 to –60dB	-3		2	
Tracking Error	ET				2	dB
DC Steps	V_{DC}	Adjacent attenuation steps		0	3	mV
		From 0dB to AV max		0.5	7.5	mV
SPEAKER ATTENUATORS						
Control Range	C_{range}		35	37.5	40	dB

(To be continued)

(Continued)

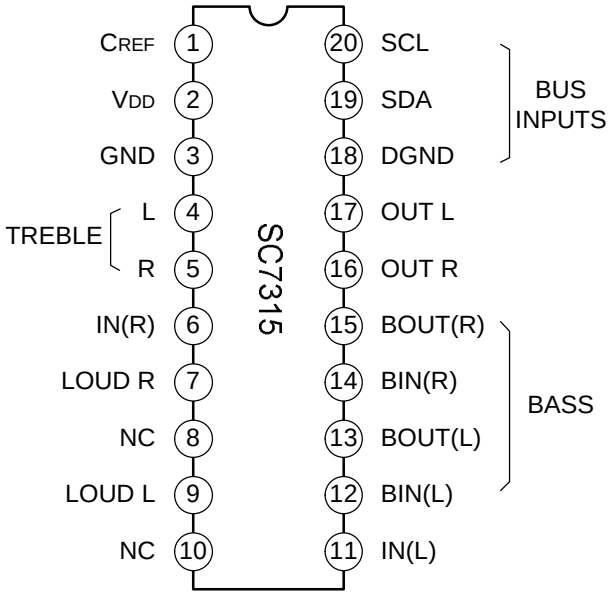
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Step Resolution	S_{STEP}		0.5	1.25	1.75	dB
Attenuation Set Error	EA				1.5	dB
Output Mute Attenuation	A_{MUTE}		80	100		dB
DC Steps	V_{DC}	Adjacent attenuation steps		0	3	mV
		From 0dB to MUTE		1	10	mV
BASS CONTROL (note 1)						
Control Range	GB	Maximum boost/cut	±12	±14	±16	dB
Step Resolution	B_{STEP}		1	2	3	dB
Internal Feedback Resistance	RB		34	44	58	kΩ
TREBLE CONTROL (note 1)						
Control Range	Gt	Maximum boost/cut	±13	±14	±15	dB
Step Resolution	TSTEP		1	2	3	dB
AUDIO OUTPUTS						
Clipping Level	V_{OCL}	THD=0.3%	2	2.5		Vrms
Output Load Resistance	R_L		4			kΩ
Output Load Capacitance	C_L				10	nF
Output Resistance	R_{OUT}		30	75	120	Ω
DC Voltage Level	V_{OUT}		4.2	4.5	4.8	V
GENERAL						
Output Noise	e_{NO}	BW=20 ~20kHz,flat output muted		2.5		μV
		BW=20 ~20kHz,flat All gains=0dB		5	15	μV
		A curve, all gains =0 dB		3		μV
Signal to Noise Ratio	S/N	All gains=0dB; Vo=1V_{rms}		106		dB
Distortion	d	A_V=0,V_{IN}=10mV		0.01	0.1	%
		A_V=-20dB, V_{IN}=1V_{rms}		0.09	0.3	%
		A_V=-20dB,V_{IN}=0.3V_{rms}		0.04		%
Channel Separation Left/Right	S_C		80	103		dB
Total Tracking Error		A_V=0 to –20 dB		0	1	dB
		A_V=-20 to –60 dB		0	2	dB
BUS INPUTS						
Input Low Voltage	V_{IL}				1	V
Input High Voltage	V_{IH}		3			V
Input Current	I_{IN}		-5		+5	μA
Output Voltage SDA Acknowledge	V_O	I_O=1.6mA			0.4	V

NOTES:

(1) Bass and treble response see Figure 16. The center frequency and quality of the response behavior can be chosen by the external circuitry. A standard first order bass response can realized by a standard feedback network.

(2) The input is grounded through the 2.2μF capacitor.

PIN CONFIGURATIONS



TYPICAL CHARACTERISTICS PERFORMANCE

Fig.1 Loudness vs. Volume Attention

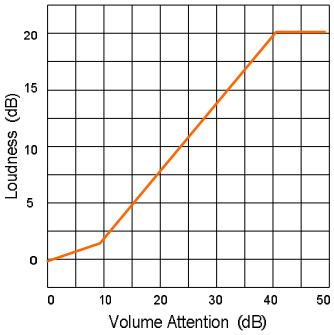


Fig.2 Loudness vs. Frequency vs. volume Attenuation

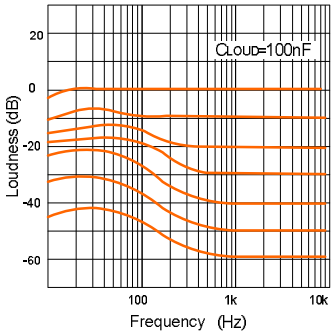


Fig.3 Loudness vs. External Capacitors

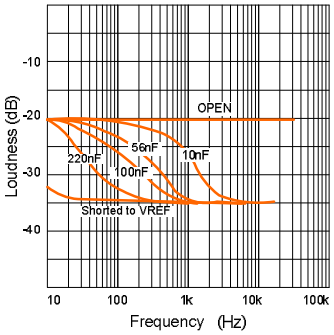


Fig.4 Noise vs. Volume/Gain settings

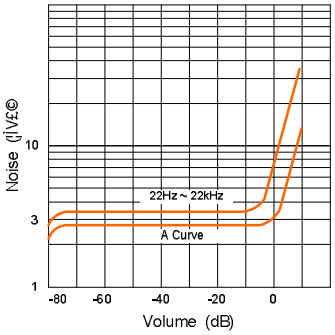


Fig.5 Signal to Noise Ratio vs.Volume settings

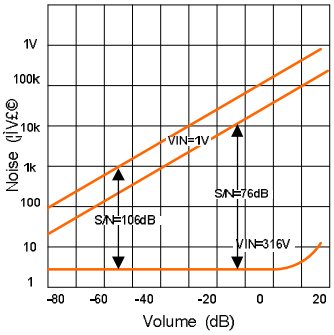


Fig.6 Distortion & Noise vs. Frequency

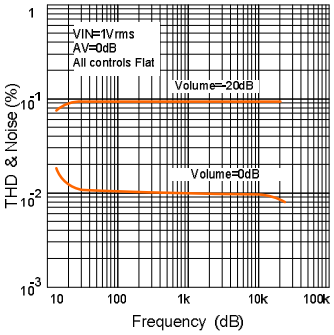


Fig.7 Distortion & Noise vs. Frequency

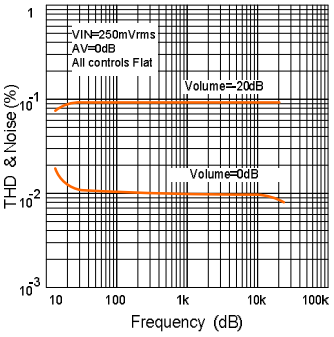


Fig.8 Distortion vs. Load Resistance

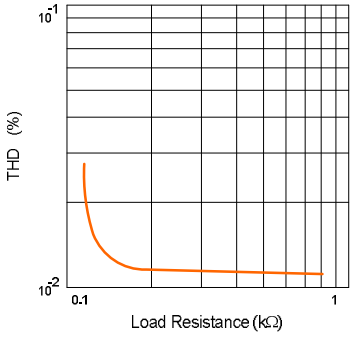
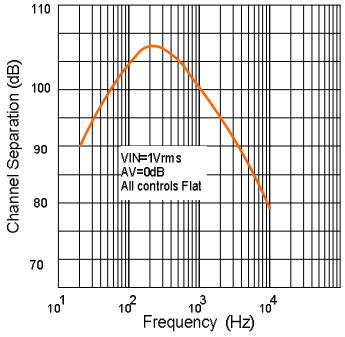


Fig.9 Channel Separation(L¡úR) vs. Frequency



TYPICAL CHARACTERISTICS PERFORMANCE (continued)

Fig.10 Input Separation vs. Frequency

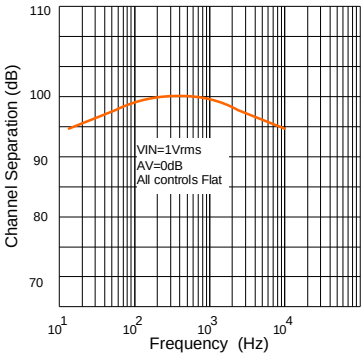


Fig.11 Supply Voltage Rejection vs. Frequency

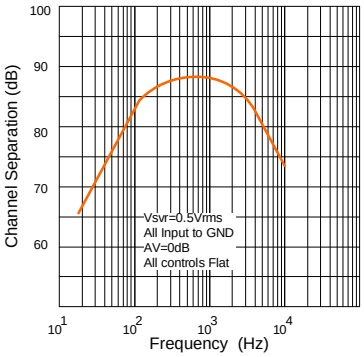


Fig.12 Output Clipping Level vs. Supply Voltage

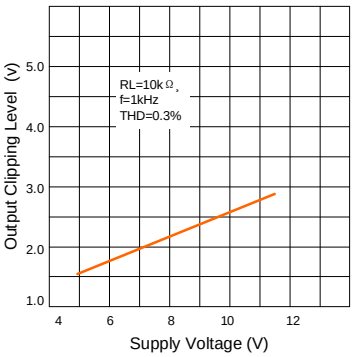


Fig.13 Quiescent current vs. Supply Voltage

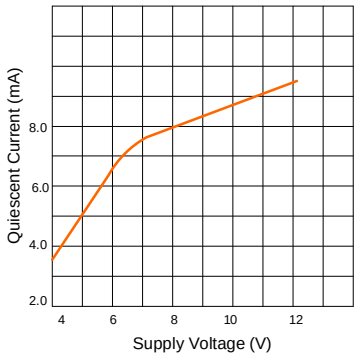


Fig.14 Supply current vs. Temperature

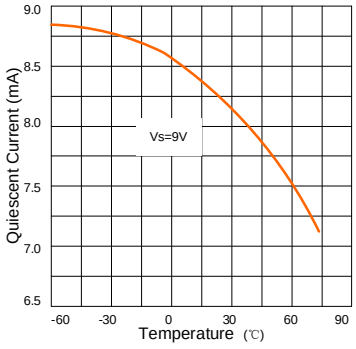


Fig.15 Bass resistance vs. Temperature

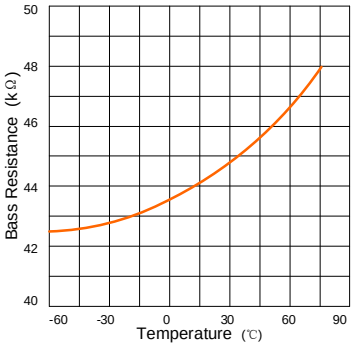
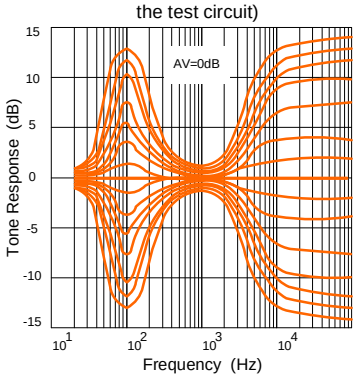


Fig.16 Typical Tone Response (with the Ext components indicated the test circuit)



APPLICATION NOTES

1. I²C BUS INTERFACE

Data transmission from microprocessor to the SC7315 and viceversa takes place through the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL(pull-up resistors to positive supply voltage must be connected).

2. DATA VALIDITY

As shown in Figure 17, the data of the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the dtat line can only change when the clock signal on the SCL line is LOW.

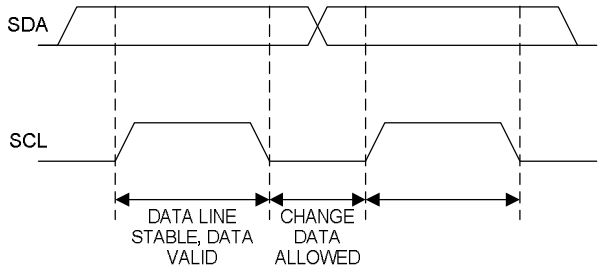


Fig. 17 Data Validity on the I^2C BUS

3. START AND STOP CONDITIONS

As shown in Figure 18, a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

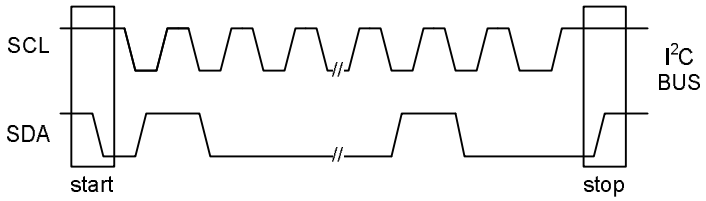


Fig. 18 Timing diagram of I2C BUS

4. BYTE FORMAT

Every byte transferred on the SDA line must obtain 8 bits. Each byte must be followed by the an acknowledge bit. The MSB is transferred first.

5. ACKNOWLEDGE

The master(microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse(see Figure 19). The peripheral(audioprocessor) that acknowledges has to pull-down(LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte , otherwise the SDA line remain at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

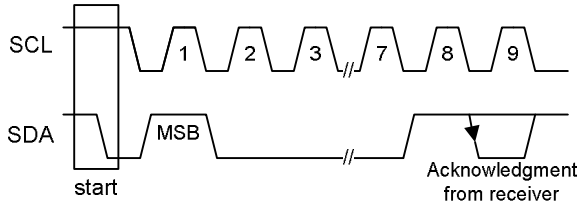


Fig. 19 Acknowledge on the I^2C BUS

6. Transmission without acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the microprocessor can use a simpler transmission: simply it waits one clock without checking the slave acknowledgig, and sends the new data.

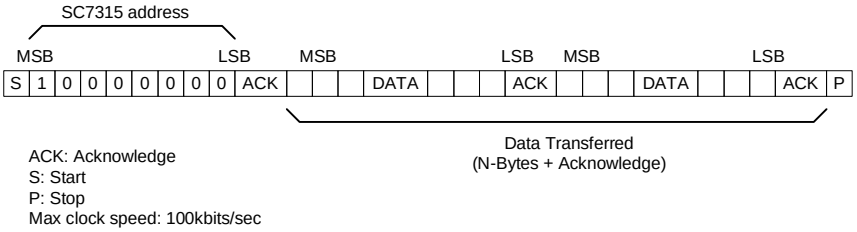
This approach of course is less protected from mis-working and decreases the noise immunity.

SOFTWARE SPECIFICATION

1. Interface protocol

The interface protocol comprises:

- A start conditions
- A chip address byte, containing the SC7315 address(the 8th bit of the bytes must be 0). The SC7315 must always acknowledge at the end of each transmitted byte.
- A sequence of data(N-bytes + acknowledge)
- A stop condition (P)



2. Chips address

1 (MSB)	0	0	0	0	0	0	0 (LSB)

3. Data bytes

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	*	*	L	*	*	Loudness control
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Note: Ax=1.25dB steps;Bx=10dB steps;Cx=2dB steps;Gx=3.75dB steps;*=no effect.

DETAILED DESCRIPTION OF DATA BYTES

1. Volume

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example, a volume of –45dB is given by: 00100100

2. Speaker attenuators

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	MUTE

For example, attenuation of 25dB on speaker R is given by: 10110100

3.Loudness function

MSB							LSB	Function
0	1	0	*	*	L	*	*	Loudness control
					0			Loudness ON
					1			Loudness OFF

Note:*=no effect

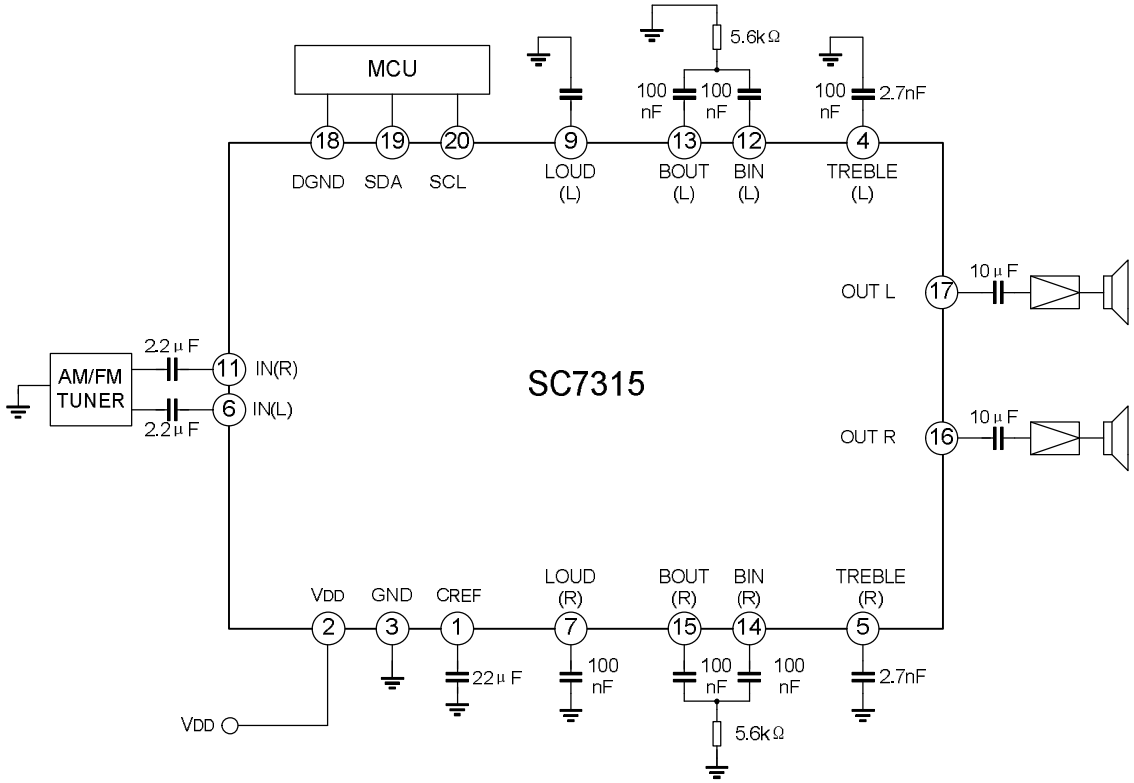
4.Bass and treble

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Terble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

C3=Sign

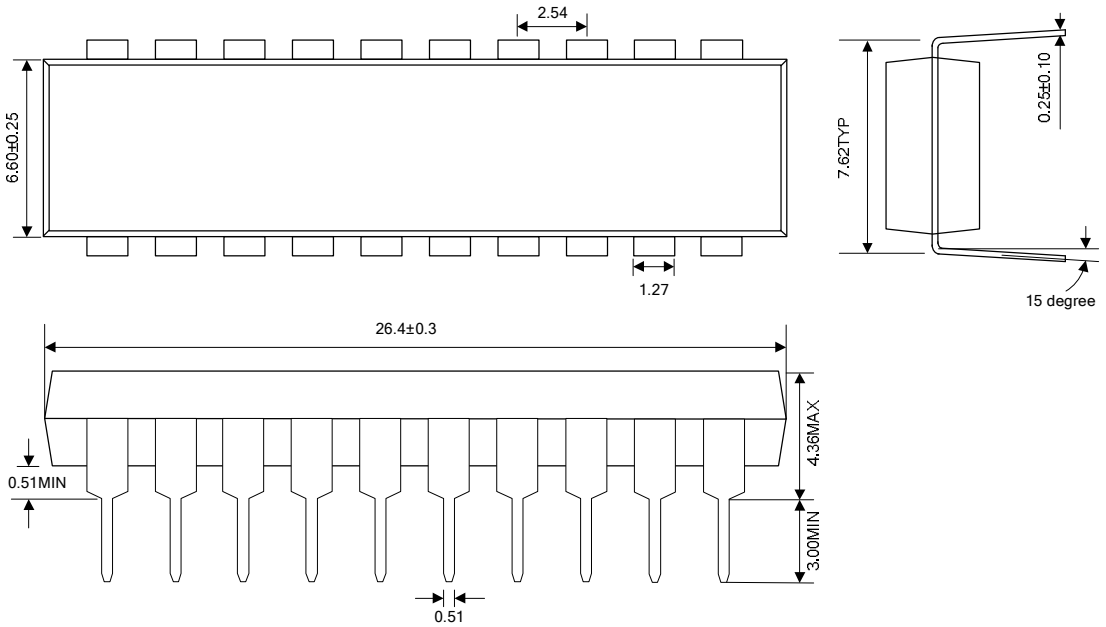
For Example, bass at –10dB is obtained by the following 8 bit string is: 01100010.

TEST AND TYPICAL APPLICATION CIRCUIT

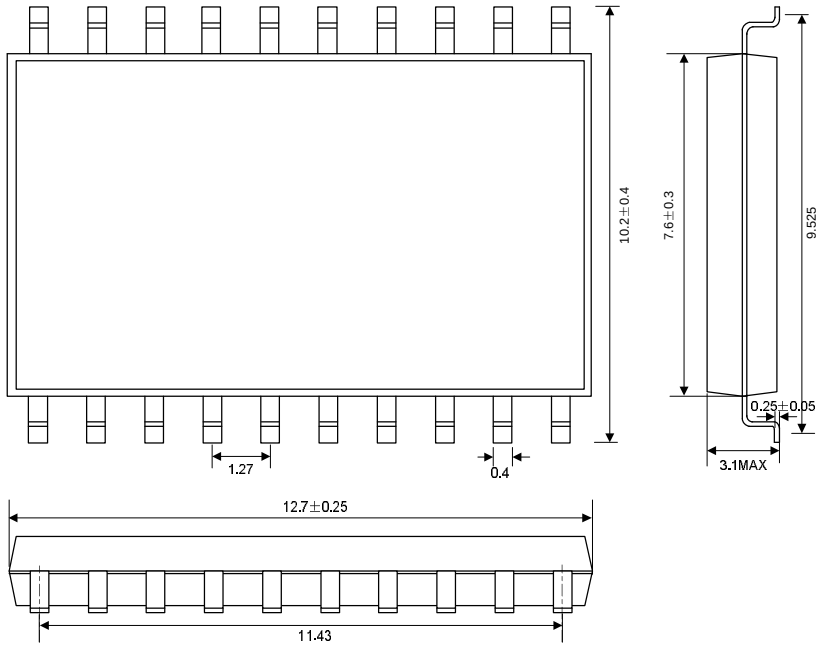


PACKAGE OUTLINE

DIP-20-300-2.54 UNIT: mm



SOP-20-375-1.27 UNIT: mm





HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.