

ASX1436 Data Sheet

Ku Band Power Amplifier MMIC

1. Product Overview

1.1 General Description

ASX1436 is a three-stage internally matched MMIC Power Amplifier which operates between 13.75 GHz and 14.50 GHz frequency range. This product is well suited for VSAT applications.

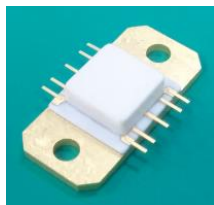
1.2 Features

- Frequency Range: 13.75 – 14.50 GHz
- Saturated Output Power: 35 dBm
- Power Added Efficiency: 28 %
- Small Signal Gain: 31.5 dB
- Output Third Order Intercept Point: 41.5 dBm
- Bias: VDD = +7 V, IDD = 1300 mA, VGG = -0.8 V (Typical)
- 100% DC and RF tested

1.3 Applications

- Ku Band VSAT
- Point to Point Radio

1.4 Package Profile & RoHS Compliance



10-lead Flange Package



RoHS-compliant

2. Summary on Product Performances

2.1 Typical Performance

Test conditions : T = +25 °C, VDD = +7 V, CW, Z₀ = 50 Ω.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	f = 13.75 - 14.50 GHz		-0.8	-0.5	V
Output Power at Psat ¹⁾	f = 13.75 - 14.50 GHz	34	35		dBm
Power Gain at Psat ¹⁾	f = 13.75 - 14.50 GHz	27	29		dB
Drain Current at Psat ¹⁾	f = 13.75 - 14.50 GHz		1550	1700	mA
Power Added Efficiency at Psat ¹⁾	f = 13.75 - 14.50 GHz		28		%
Gain Flatness	f = 13.75 - 14.50 GHz		1.5	2.0	dB
Input Return Loss	f = 13.75 - 14.50 GHz		-10	-6	dB
Output Return Loss	f = 13.75 - 14.50 GHz		-15	-8	dB
Output TOI ²⁾	Δ f = 10 MHz 2-Tone Test Output power / Tone = +26 dBm		41.5		dBm
Supply Current	VDD = +7 V		1300		mA

1) Psat: Saturated output power

2) TOI: Third order intercept point

2.2 Product Specification

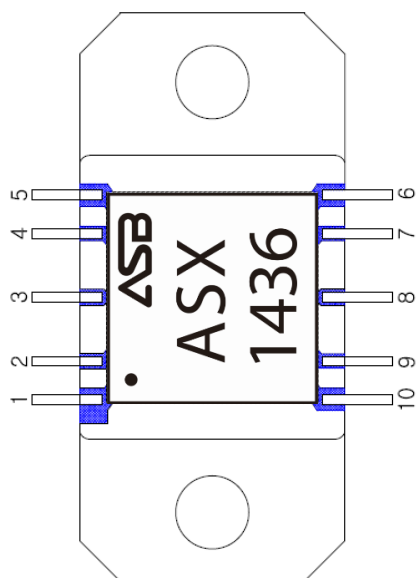
Test conditions : T = +25 °C, VDD = +7 V, CW, VGG = -0.8 V typical, Z₀ = 50 Ω.

Parameter	Min	Typ	Max	Unit
Frequency	13.75		14.50	GHz
Small Signal Gain	29.5	31.5		dB
Input Return Loss		-10	-6	dB
Output Return Loss		-15	-8	dB
Supply Current		1300		mA

2.3 Absolute Maximum Ratings

Parameters	Max. Ratings
Operating Case Temperature (T _c)	-40 to +85 °C
Storage Temperature (T _{stg})	-55 to +125 °C
Drain Voltage (VDD)	+9 V
Gate Voltage (VGG)	-1.5 to -0.5 V
Input RF Power (P _{in})	+18 dBm

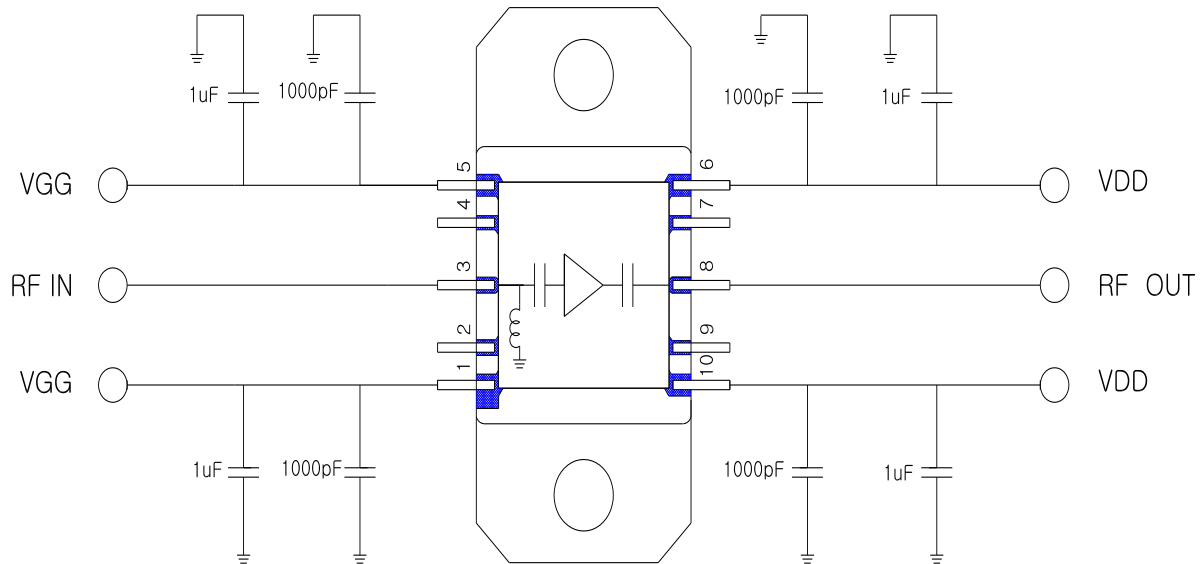
2.4 Pin Descriptions



Pin	Pin Name	Description
1,5	Vg	Gate voltage
3	RF IN	Input, matched to 50 ohms
6,10	Vd	Drain voltage
8	RF OUT	Output, matched to 50 ohms
2,4,7,9	NC	No internal connection (open or connected to GND)

3. Application 1: 13.75 – 14.50 GHz, VDD = +7V, IDD = 1300mA

3.1 Application Circuit



Note 1: The capacitors are recommended on the bias supply line, close to the package, in order to prevent video oscillations which could damage the module.

3.2 Biasing Procedure

- Make sure no RF power is applied to the device before continuing.
- Pinch off device by setting VGG to -1.5 V.
- Raise VDD to +7 V while monitoring drain current.
- Raise VGG until drain current reaches 1300 mA. VGG should be between -1.5 and -0.5 V.
- Apply RF power.
- To improve the thermal and RF performance, ASB recommends a heat sinker attached to the bottom of the package with an Indium alloy preform.

3.3 Performance Table

Test conditions : T = +25 °C, VDD = +7 V, CW, Z₀ = 50 Ω.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	f = 13.75 - 14.50 GHz		-0.8	-0.5	V
Output Power at Psat ¹⁾	f = 13.75 - 14.50 GHz	34	35		dBm
Power Gain at Psat ¹⁾	f = 13.75 - 14.50 GHz	27	29		dB
Drain Current at Psat ¹⁾	f = 13.75 - 14.50 GHz		1550	1700	mA
Power Added Efficiency at Psat ¹⁾	f = 13.75 - 14.50 GHz		28		%
Gain Flatness	f = 13.75 - 14.50 GHz		1.5	2.0	dB
Input Return Loss	f = 13.75 - 14.50 GHz		-10	-6	dB
Output Return Loss	f = 13.75 - 14.50 GHz		-15	-8	dB
Output TOI ²⁾	Δ f = 10 MHz 2-Tone Test Output power / Tone = +26 dBm		41.5		dBm
Supply Current	VDD = +7 V		1300		mA

1) Psat: Saturated output power

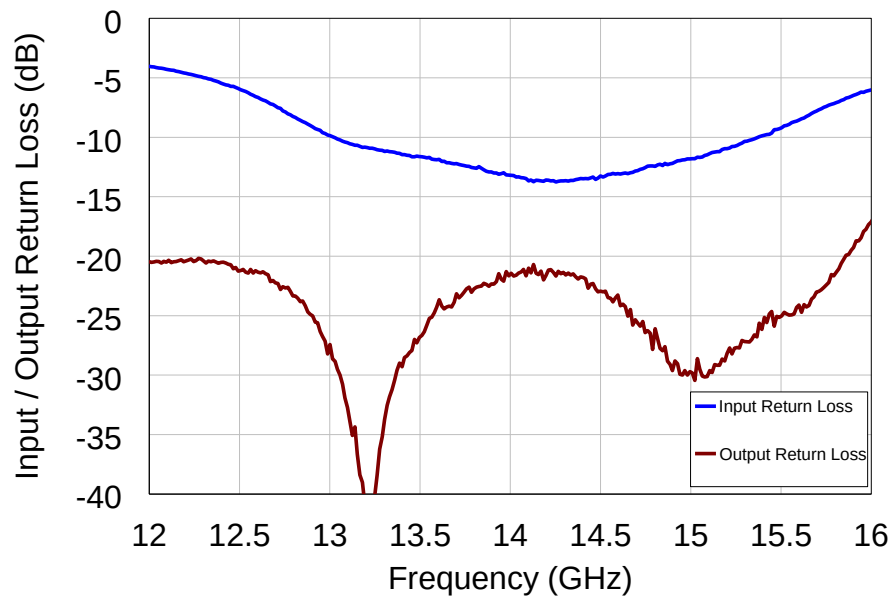
2) TOI: Third order intercept point

3.4 Plots of Performances

S-parameter

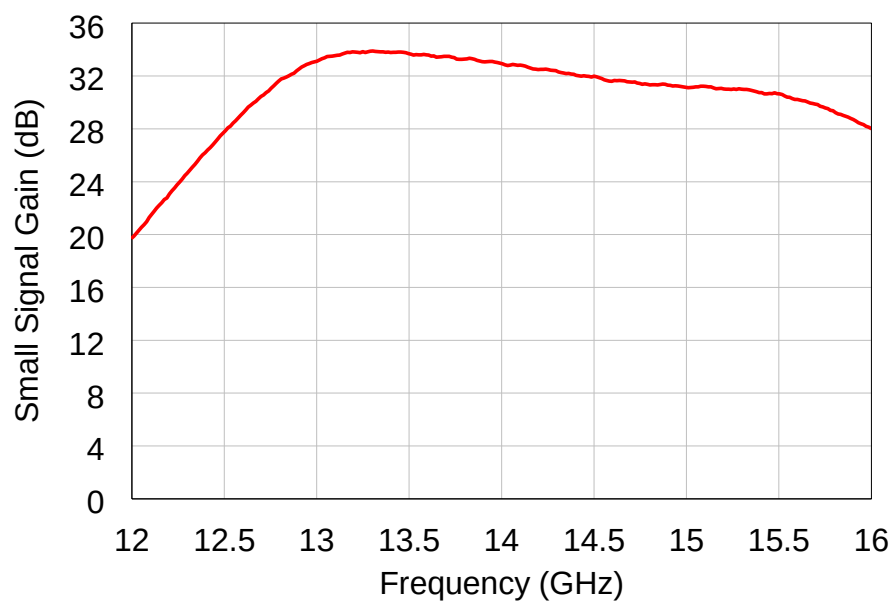
Input / Output Return Loss vs. Frequency

VDD = +7 V, IDD = 1300 mA, Pin = -20 dBm



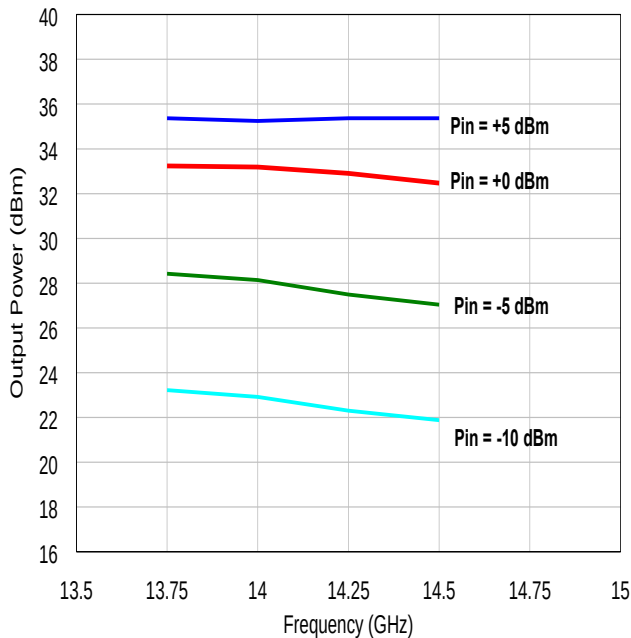
Small Signal Gain vs. Frequency

VDD = +7 V, IDD = 1300 mA, Pin = -20 dBm



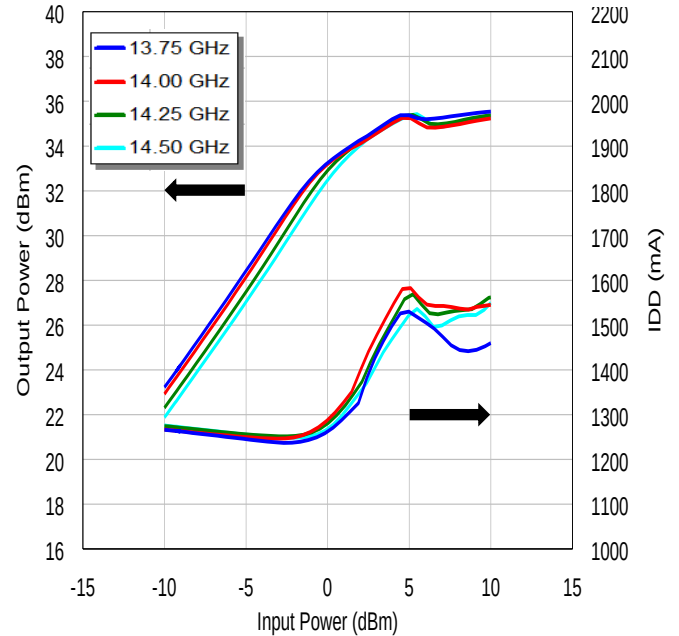
Output Power vs. Frequency

VDD = +7 V, IDD = 1300 mA



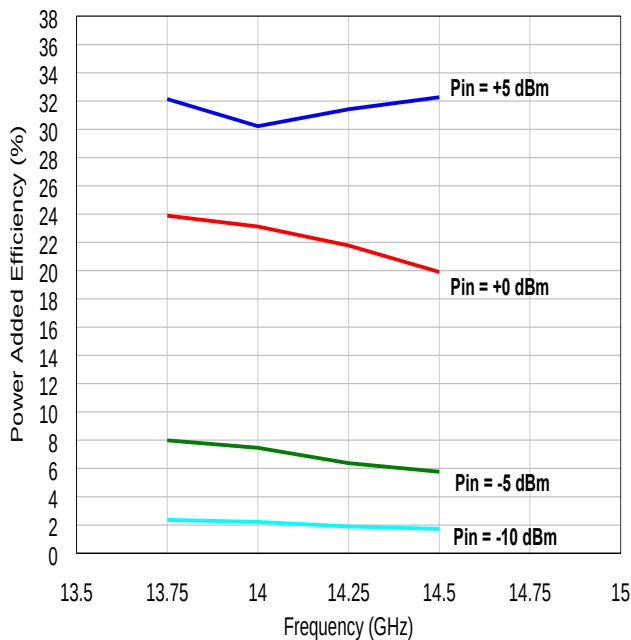
Output Power, IDD vs. Input Power

VDD = +7 V, IDD = 1300 mA



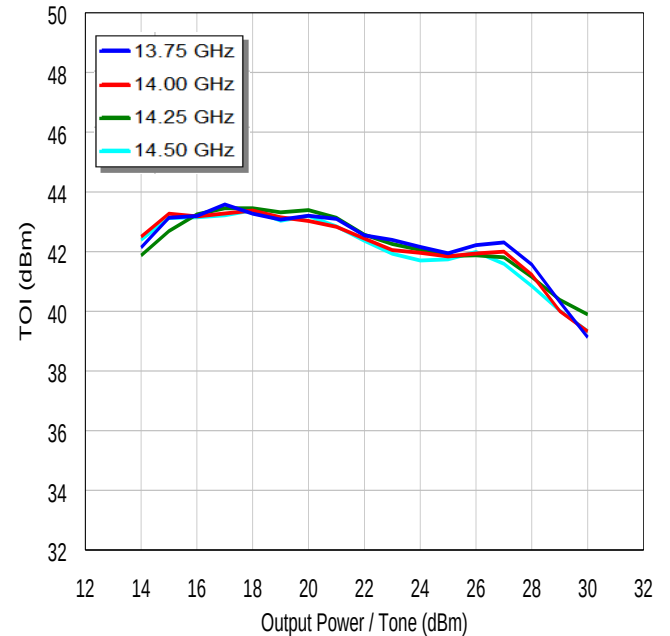
Power Added Efficiency vs. Frequency

VDD = +7 V, IDD = 1300 mA



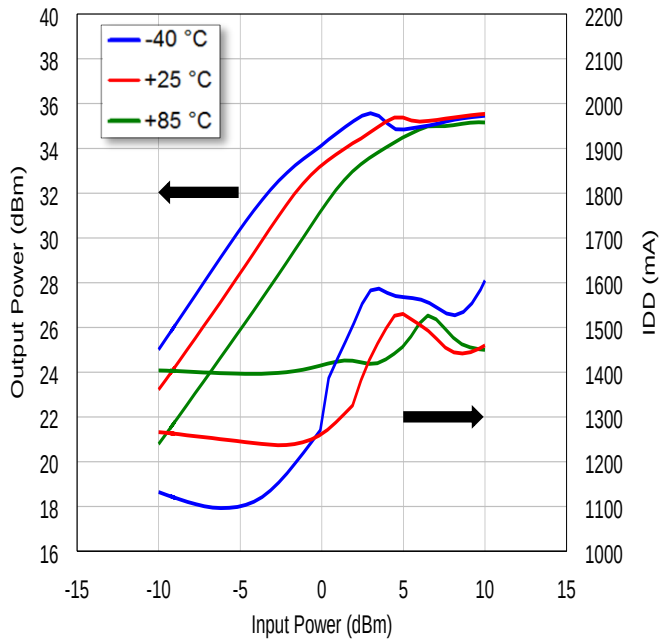
Output TOI vs. Output Power / Tone

VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

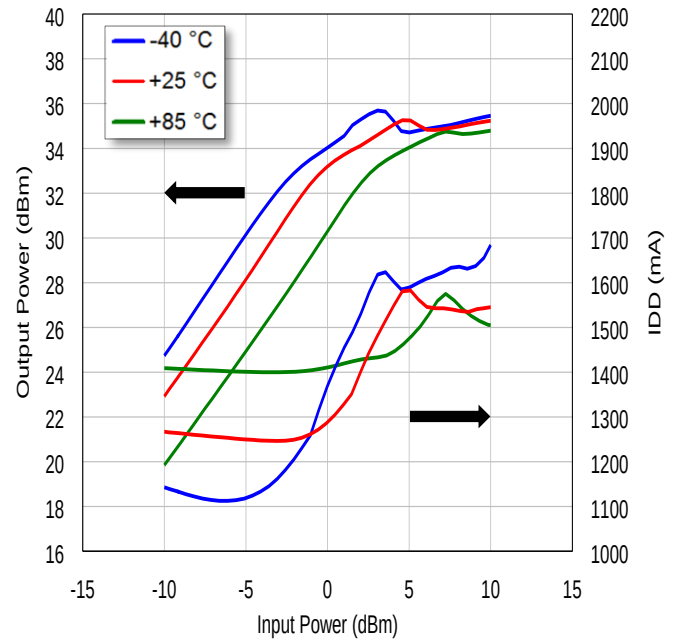


Output Power, Drain Current vs. Input Power by Temperature

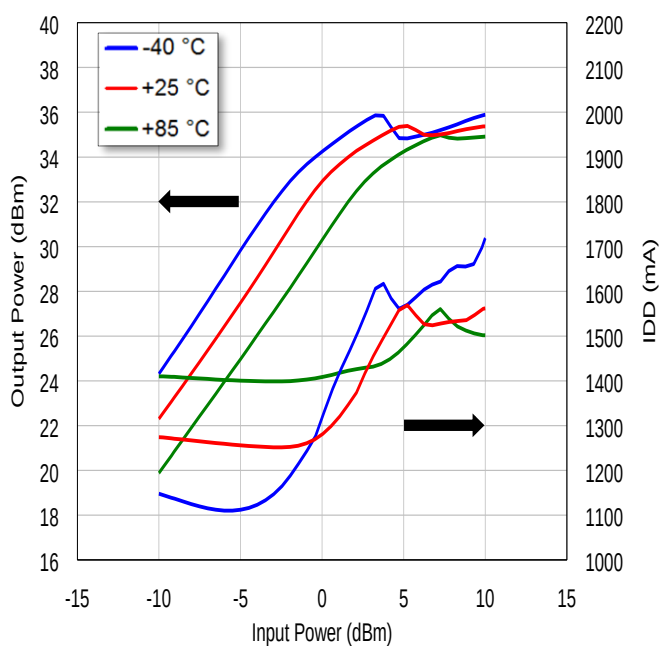
VDD = +7 V, IDD = 1300 mA @ 13.75 GHz



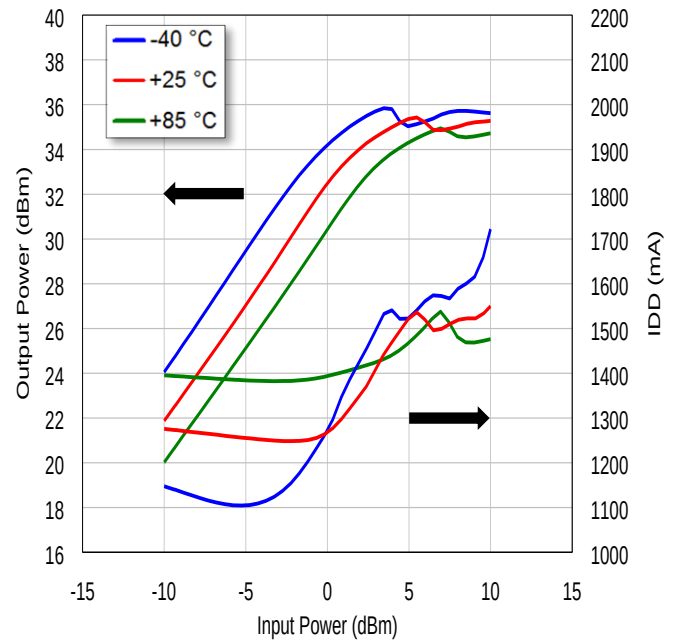
VDD = +7 V, IDD = 1300 mA @ 14.00 GHz



VDD = +7 V, IDD = 1300 mA @ 14.25 GHz



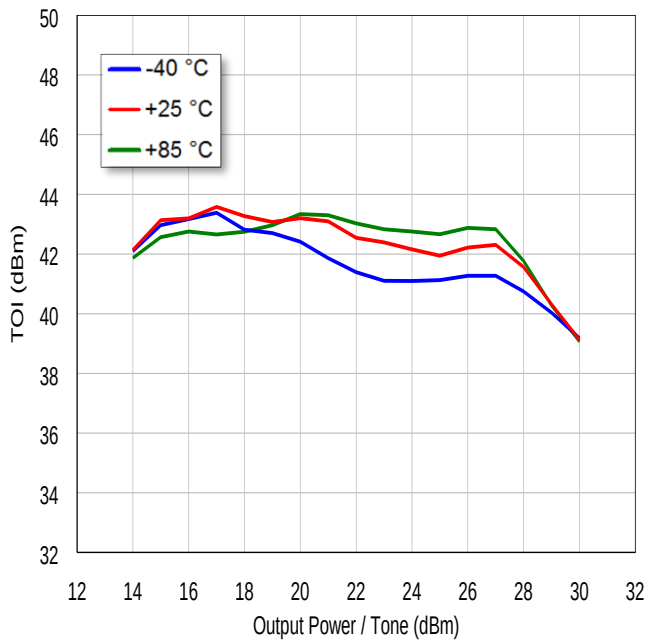
VDD = +7 V, IDD = 1300 mA @ 14.50 GHz



Output TOI vs. Output Power / Tone by Temperature

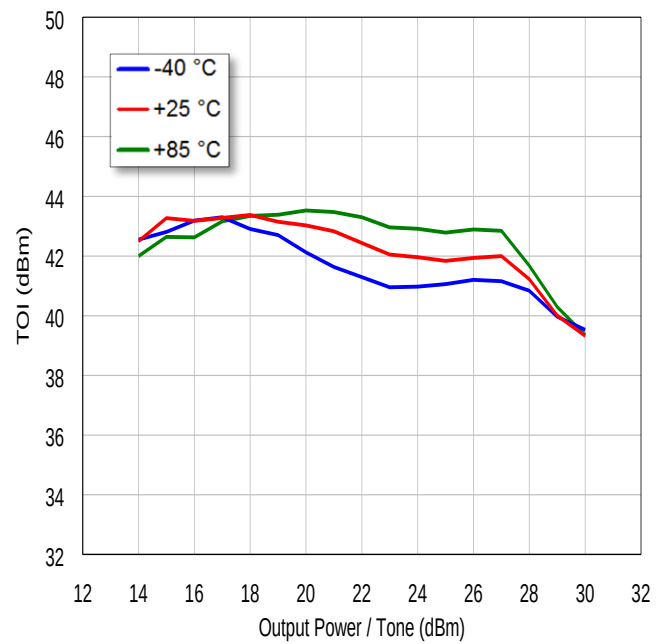
VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

@ 13.75 GHz



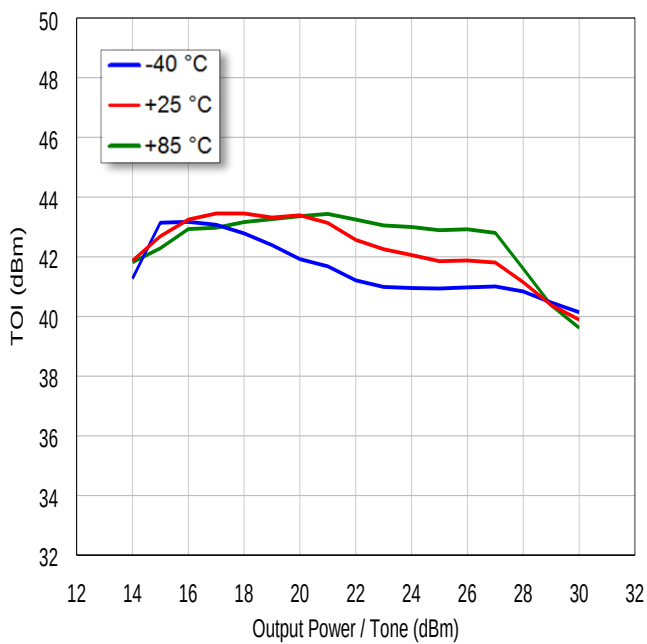
VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

@ 14.00 GHz



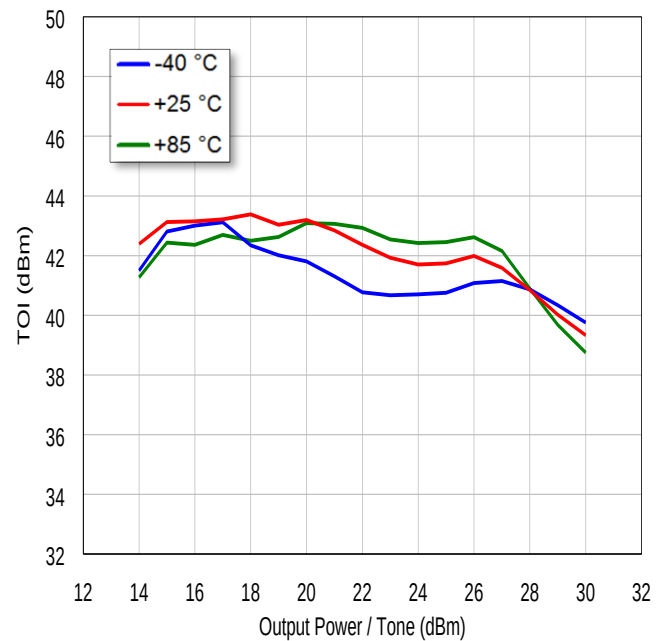
VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

@ 14.25 GHz



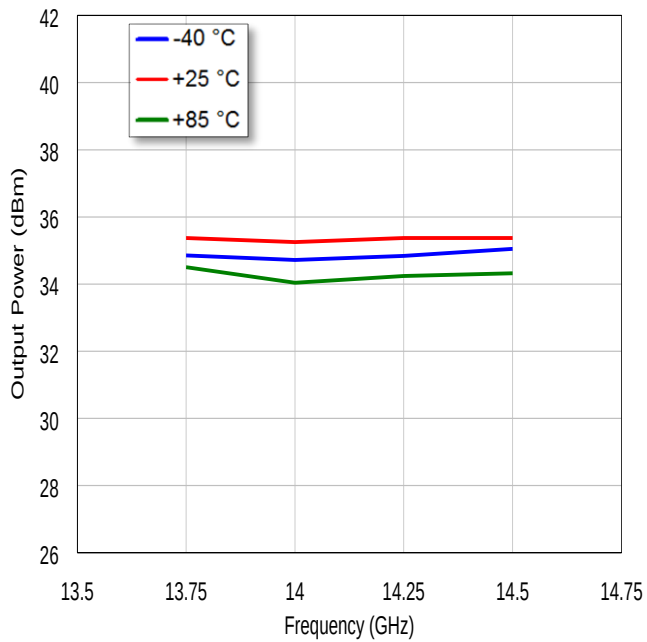
VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

@ 14.50 GHz



Output Power vs. Frequency

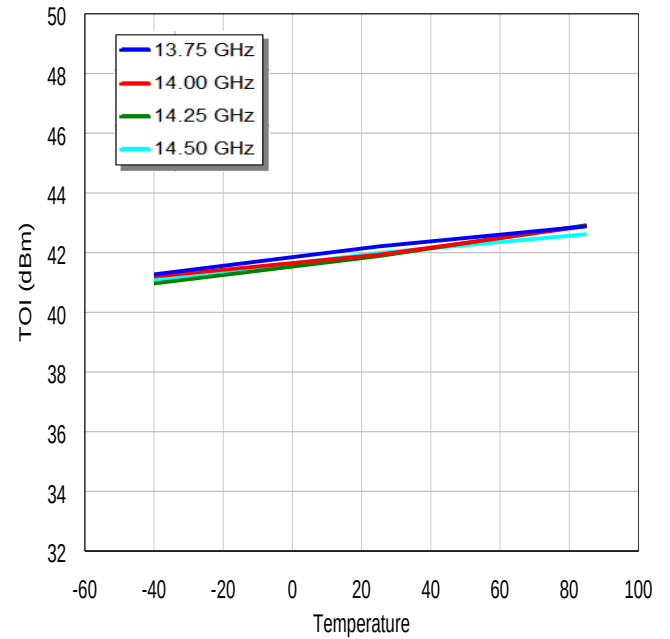
VDD = +7 V, IDD = 1300 mA, Pin = +5 dBm, CW



Output TOI vs. Temperature

VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz

Output power / Tone = +26 dBm

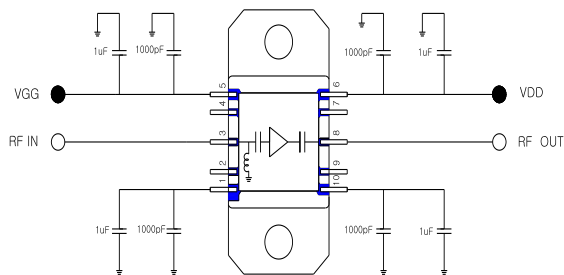


4. Application 2: 13.75 – 14.50 GHz, VDD = +7V, IDD = 1300mA

4.1 Application Circuit

- In case of one VGG and one VDD bias applied.

Case 1



4.3 Performance Table

Test conditions : T = +25 °C, VDD = +7 V, CW, Z₀ = 50 Ω.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	f = 13.75 - 14.50 GHz		-0.8	-0.5	V
Output Power at Psat ¹⁾	f = 13.75 - 14.50 GHz	33	34		dBm
Power Gain at Psat ¹⁾	f = 13.75 - 14.50 GHz	27	29		dB
Drain Current at Psat ¹⁾	f = 13.75 - 14.50 GHz		1400	1600	mA
Power Added Efficiency at Psat ¹⁾	f = 13.75 - 14.50 GHz		25		%
Gain Flatness	f = 13.75 - 14.50 GHz		1.5	2.0	dB
Input Return Loss	f = 13.75 - 14.50 GHz		-10	-6	dB
Output Return Loss	f = 13.75 - 14.50 GHz		-12	-8	dB
Output TOI ²⁾	Δ f = 10 MHz 2-Tone Test Output power / Tone = +26 dBm		42		dBm
Supply Current	VDD = +7 V		1300		mA

1) Psat: Saturated output power

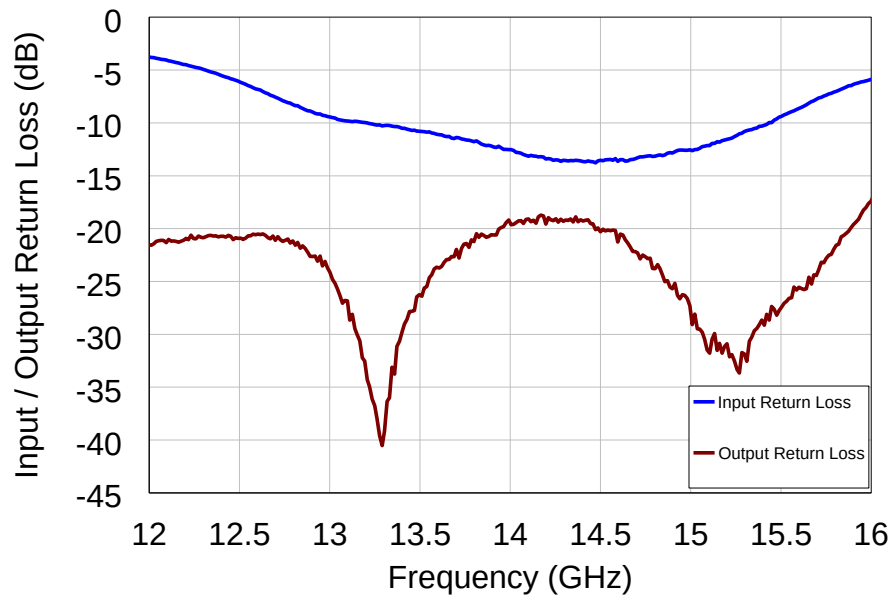
2) TOI: Third order intercept point

4.4 Plots of Performances

S-parameter

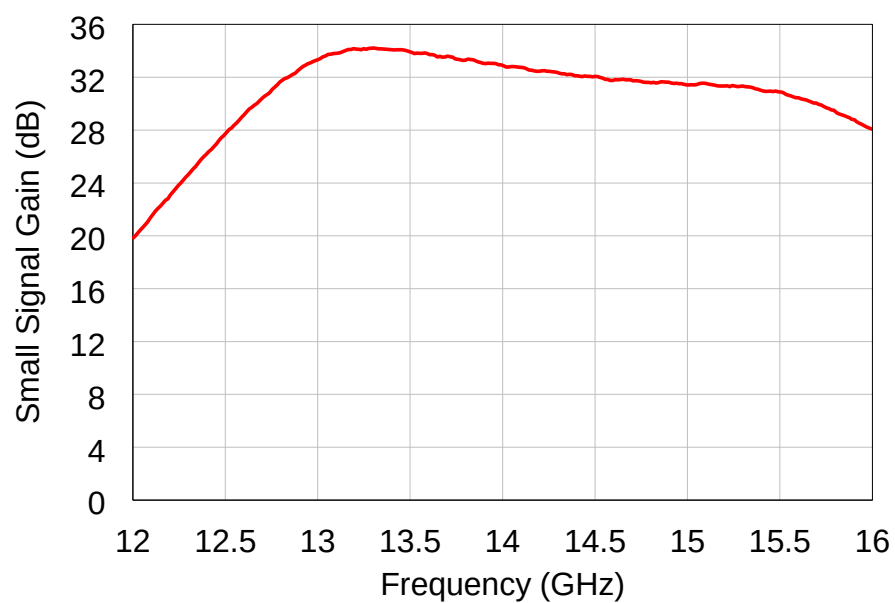
Input / Output Return Loss vs. Frequency

VDD = +7 V, IDD = 1300 mA, Pin = -20 dBm



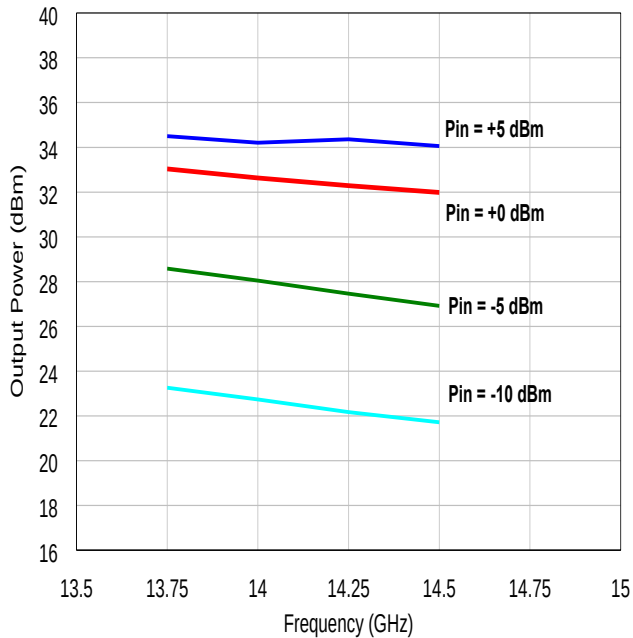
Small Signal Gain vs. Frequency

VDD = +7 V, IDD = 1300 mA, Pin = -20 dBm



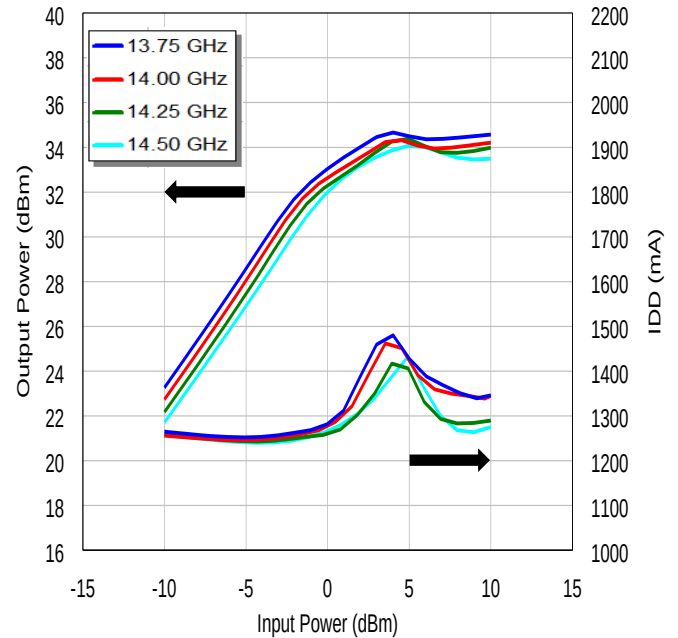
Output Power vs. Frequency

VDD = +7 V, IDD = 1300 mA



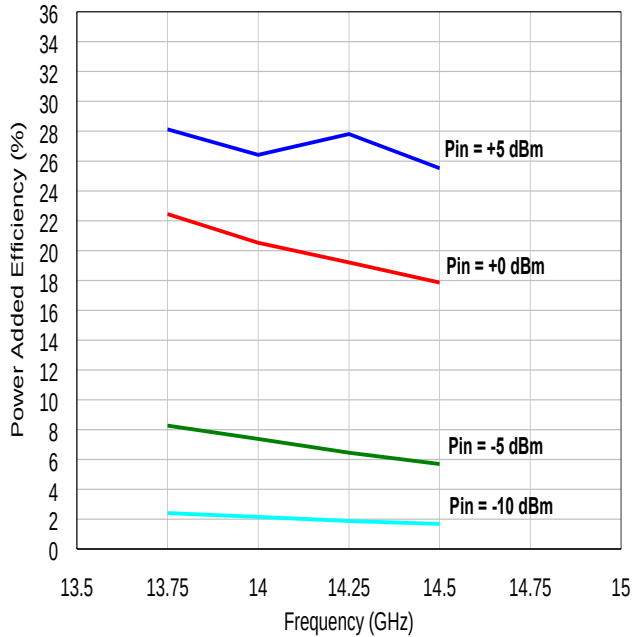
Output Power, IDD vs. Input Power

VDD = +7 V, IDD = 1300 mA



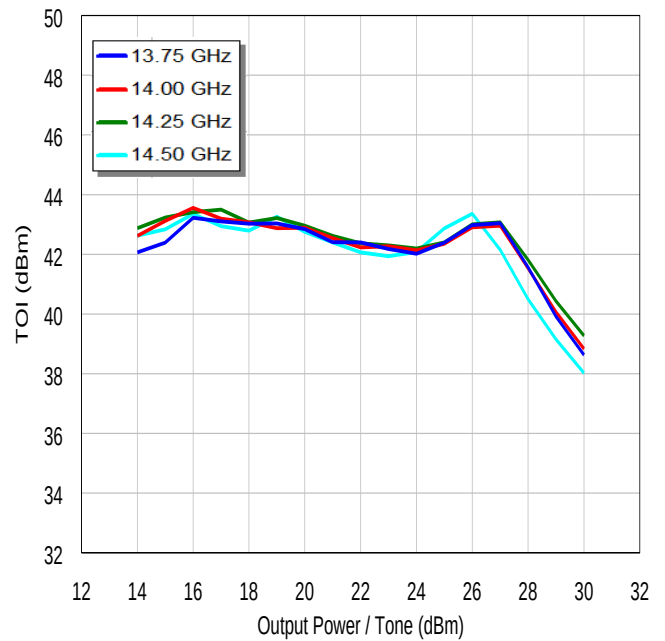
Power Added Efficiency vs. Frequency

VDD = +7 V, IDD = 1300 mA



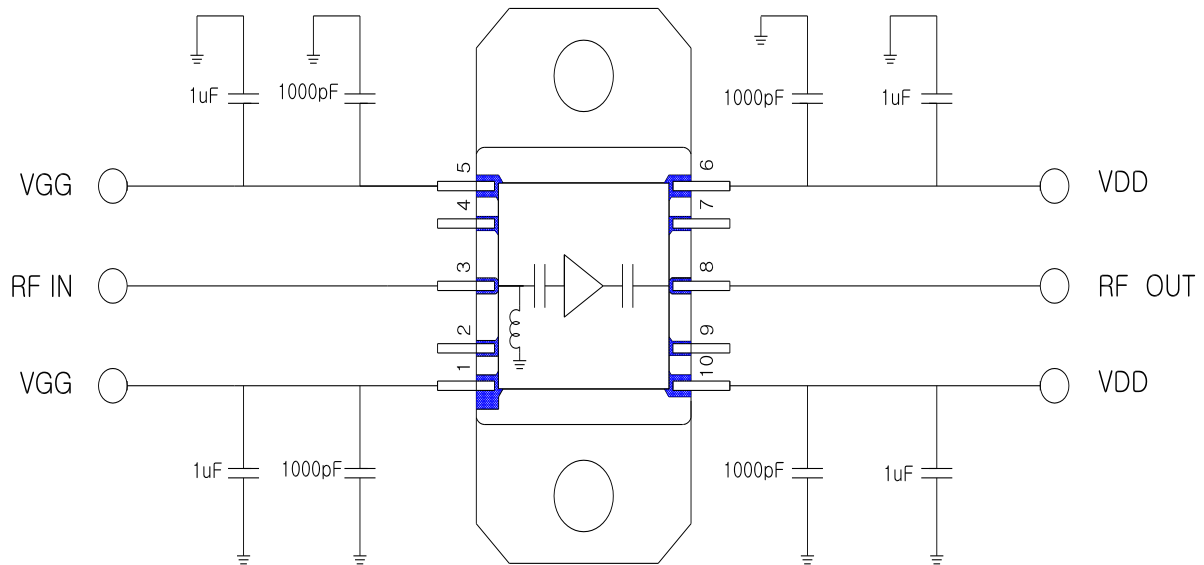
Output TOI vs. Output Power / Tone

VDD = +7 V, IDD = 1300 mA, $\Delta f = 10$ MHz



5. Application 3: 13.75 – 14.50 GHz, VDD = +5V, IDD = 1300mA

5.1 Application Circuit



Note 1: The capacitors are recommended on the bias supply line, close to the package, in order to prevent video oscillations which could damage the module.

5.2 Biasing Procedure

- Make sure no RF power is applied to the device before continuing.
- Pinch off device by setting VGG to -1.5 V.
- Raise VDD to +5 V while monitoring drain current.
- Raise VGG until drain current reaches 1300 mA. VGG should be between -1.5 and -0.5 V.
- Apply RF power.
- To improve the thermal and RF performance, ASB recommends a heat sinker attached to the bottom of the package with an Indium alloy preform.

5.3 Performance Table

Test conditions : T = +25 °C, VDD = +5 V, CW, Z₀ = 50 Ω.

Parameters	Test Conditions	Min	Typ	Max	Units
Gate Bias Voltage	f = 13.75 - 14.50 GHz		-0.8	-0.5	V
Output Power at Psat ¹⁾	f = 13.75 - 14.50 GHz	30	31		dBm
Power Gain at Psat ¹⁾	f = 13.75 - 14.50 GHz	24	26		dB
Drain Current at Psat ¹⁾	f = 13.75 - 14.50 GHz		1250	1400	mA
Power Added Efficiency at Psat ¹⁾	f = 13.75 - 14.50 GHz		23		%
Gain Flatness	f = 13.75 - 14.50 GHz		0.5	1.0	dB
Input Return Loss	f = 13.75 - 14.50 GHz		-8	-6	dB
Output Return Loss	f = 13.75 - 14.50 GHz		-10	-8	dB
Output TOI ²⁾	Δ f = 10 MHz 2-Tone Test Output power / Tone = +22 dBm		40		dBm
Supply Current	VDD = +5 V		1300		mA

1) Psat: Saturated output power

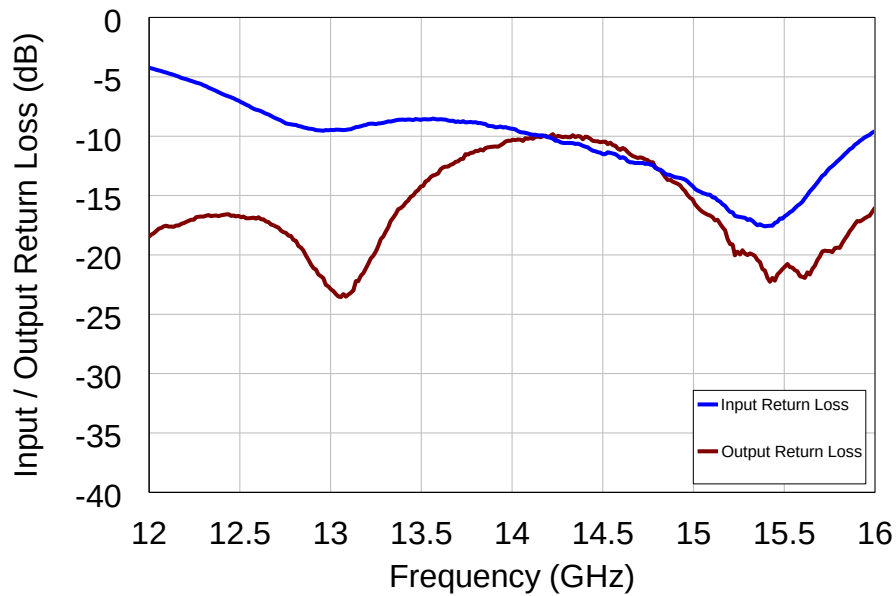
2) TOI: Third order intercept point

5.4 Plots of Performances

S-parameter

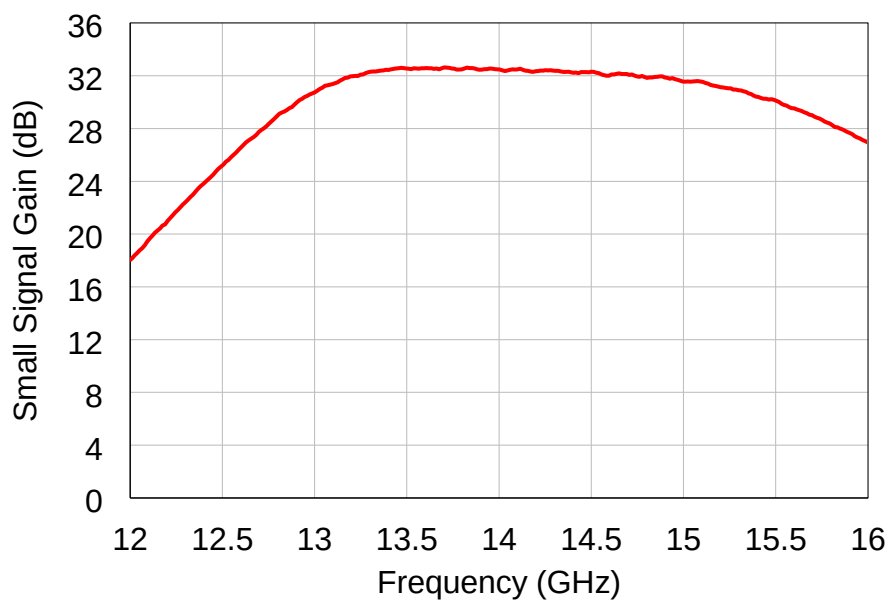
Input / Output Return Loss vs. Frequency

VDD = +5 V, IDD = 1300 mA, Pin = -20 dBm



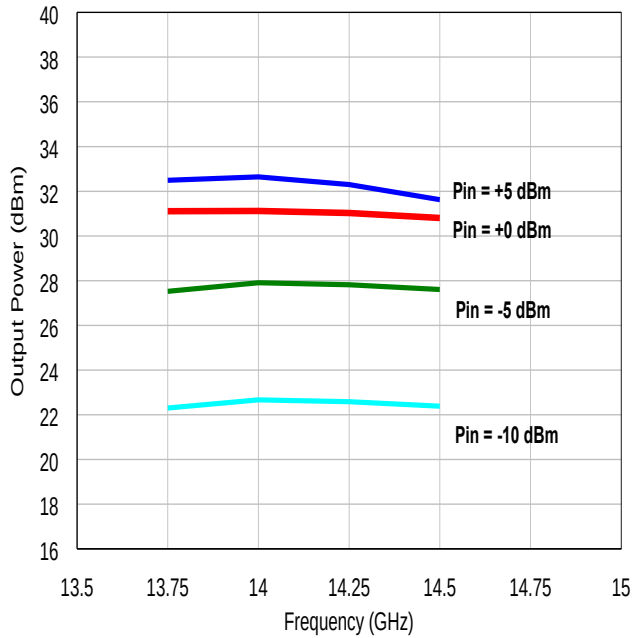
Small Signal Gain vs. Frequency

VDD = +5 V, IDD = 1300 mA, Pin = -20 dBm



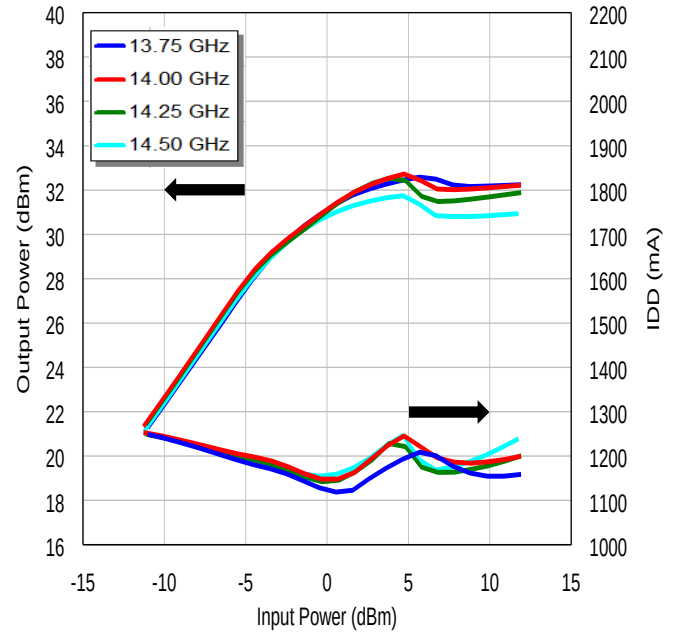
Output Power vs. Frequency

VDD = +5 V, IDD = 1300 mA



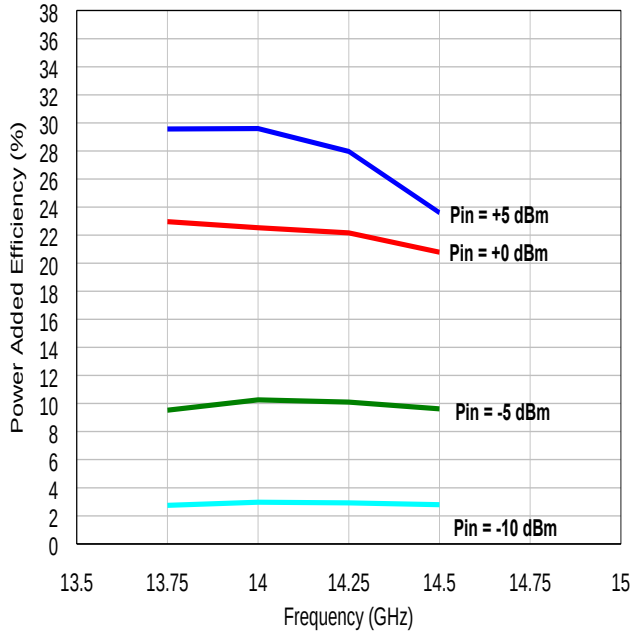
Output Power, IDD vs. Input Power

VDD = +5 V, IDD = 1300 mA



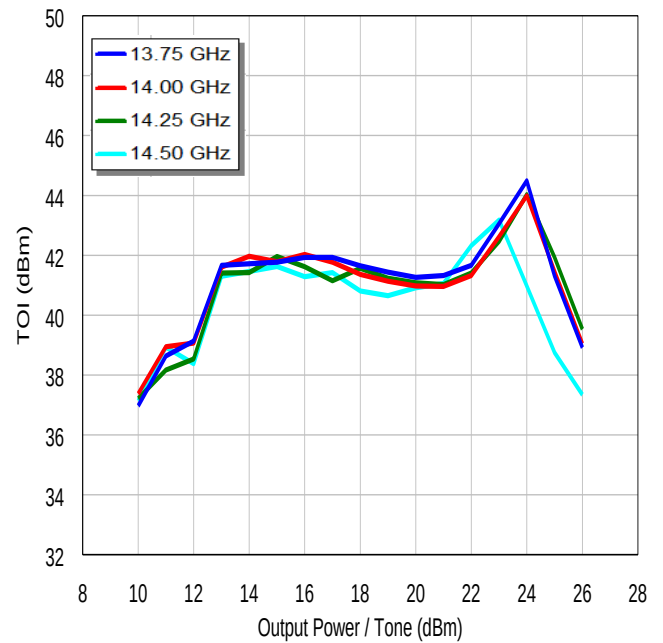
Power Added Efficiency vs. Frequency

VDD = +5 V, IDD = 1300 mA



Output TOI vs. Output Power / Tone

VDD = +5 V, IDD = 1300 mA, $\Delta f = 10$ MHz



6. Mounting Instructions for Flange Package

6.1 Screw Mounting

6.1.1 The flange of package should be attached using screws. Torque conditions are shown in table 1.

Table 1. Recommended and Maximum Torque for Screw Mounting

Package	Recommended Screw	Recommended Torque	Maximum Torque
Flange	M2.0	10 N-cm (0.9 lb-in)	15 N-cm (1.3 lb-in)

6.1.2 First, tighten the screws with a torque driver set to 5 N-cm

6.1.3 The surface finish of the heat sinker should be better than 0.8 μm and the surface flatness must be better than 10 μm .

6.1.4 Silicon based heat sink compounds should not be used for the thermal conductive grease. It causes the poor grounding of the source flange, contamination, and long term degradation of thermal resistance between the package and heat sinker.

6.2. Solder Mounting

6.2.1 Recommended solder is lead-free solder (Sn-3.0Ag-0.5Cu) or equivalent.

6.2.2 After soldering, the flux residue should be removed by appropriate cleaning methods.

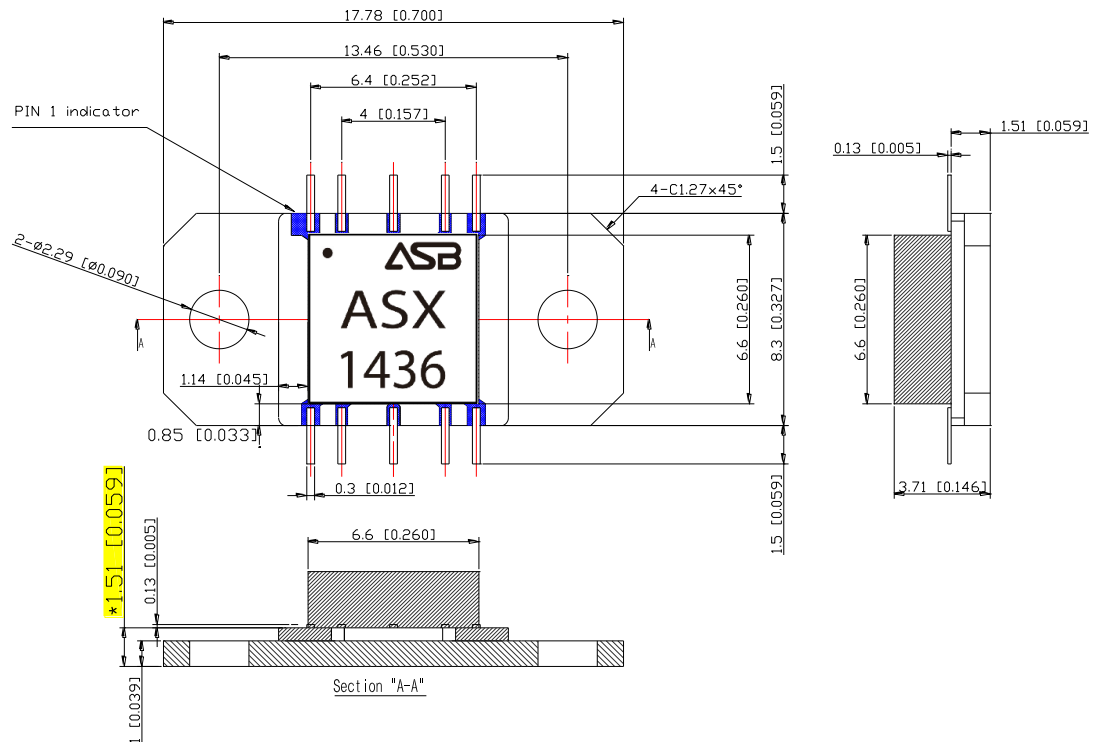
6.2.3 The recommended soldering conditions are as follows:

Partial heating method: Soldering iron, spot laser/air

Product terminal temperature: 260°C, max. 10 sec/terminal or 400°C, max. 3 sec/terminal

7. Package Outline

Units: mm [in]



* Please note the 1.51 mm of the height of the lead from the bottom of the metal base when it is to be mounted.

(End of Datasheet)

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