Low Threshold N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low ON-resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-Channel devices

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Medical ultrasound pulsers
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

The Supertex TN2425 is a low threshold enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)
	TO-243AA (SOT-89)				
TN2425	TN2425N8	TN2425N8-G	250V	3.5Ω	1.5A

-G indicates package is RoHS compliant ('Green')

Product marking for TO-243AA:

TN4C✳

where ✳ = 2-week alpha date code

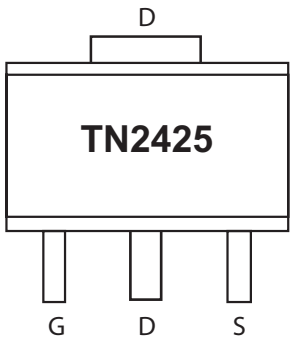
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Gate to source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature[1]	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

***Note 1**. Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



TO-243AA (SOT-89)
(Top View)

Electrical Characteristics (T_A=25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	250	-	-	V	V_{GS} = 0V, I_D = 250µA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	$V_{GS(th)}$ change with temperature	-	-	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current	0.8	-	-	A	V_{GS} = 4.5V, V_{DS} = 25V
		1.5	-	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	6.0	Ω	V_{GS} = 3.0V, I_D = 150mA
		-	-	5.0		V_{GS} = 4.5V, I_D = 250mA
		-	-	3.5		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward transconductance	500	-	-	mmho	V_{DS} = 25V, I_D = 250mA
C_{ISS}	Input capacitance	-	105	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common source output capacitance	-	25	100		
C_{RSS}	Reverse transfer capacitance	-	7	40		
$t_{d(ON)}$	Turn-ON delay time	-	5	15	ns	V_{DD} = 25V, I_D = 500mA, R_{GEN} = 25Ω
t_r	Rise time	-	10	25		
$t_{d(OFF)}$	Turn-OFF delay time	-	25	35		
t_f	Fall time	-	5	15		
V_{SD}	Diode forward voltage drop	-	-	1.5	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 500mA

Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

Thermal Characteristics

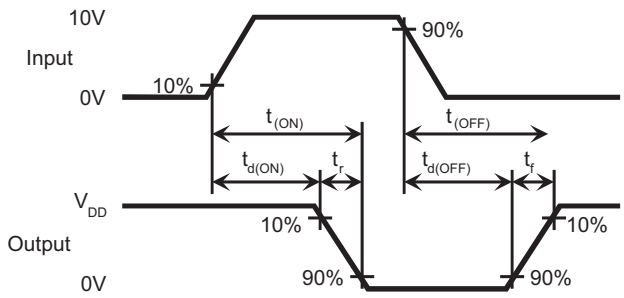
Package	I_D (continuous)†	ID (pulsed)	Power Dissipation @T_A = 25°C	θ_{JC} (°C/W)	θ_{JA} (°C/W)	I_{DR}†	I_{DRM}
TO-243AA	480mA	1.9A	1.6W‡	15	78‡	480mA	1.9A

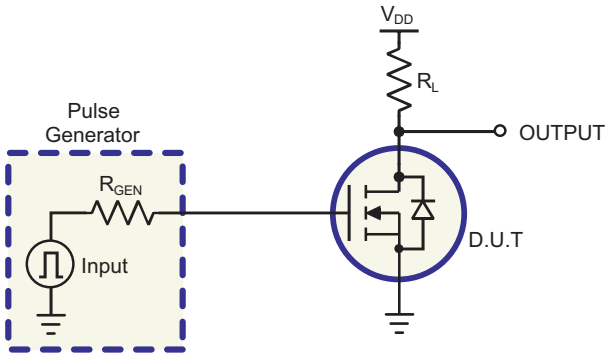
Notes:

† ID (continuous) is limited by max rated T_J.

‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant PD increase possible on ceramic substrate.

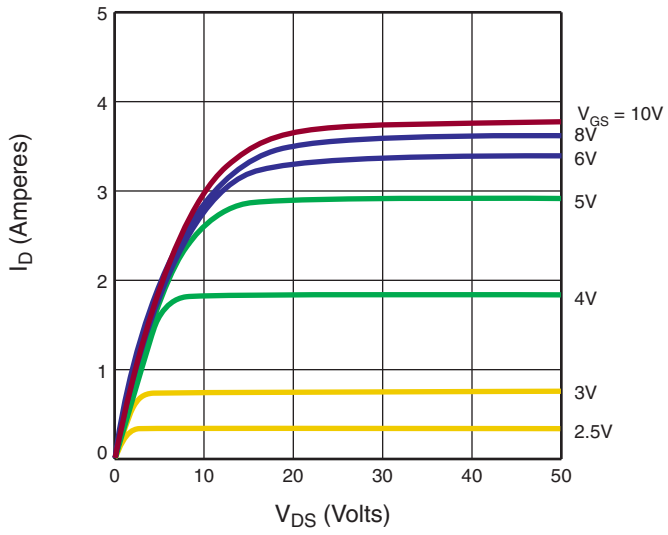
Switching Waveforms and Test Circuit



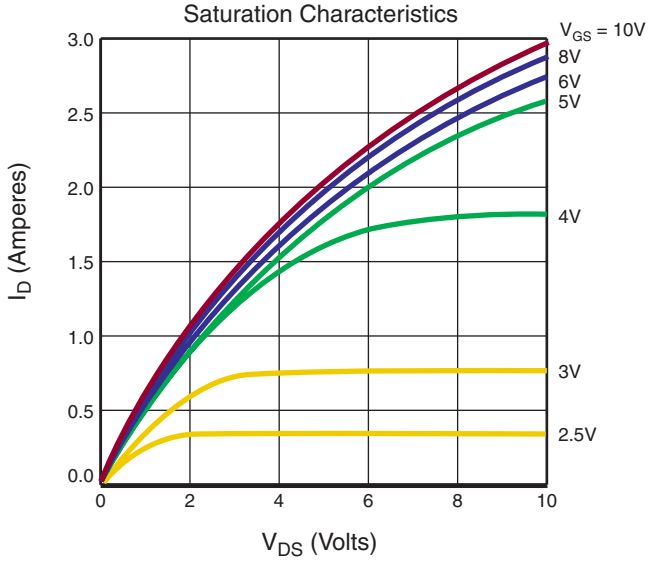


Typical Performance Curves

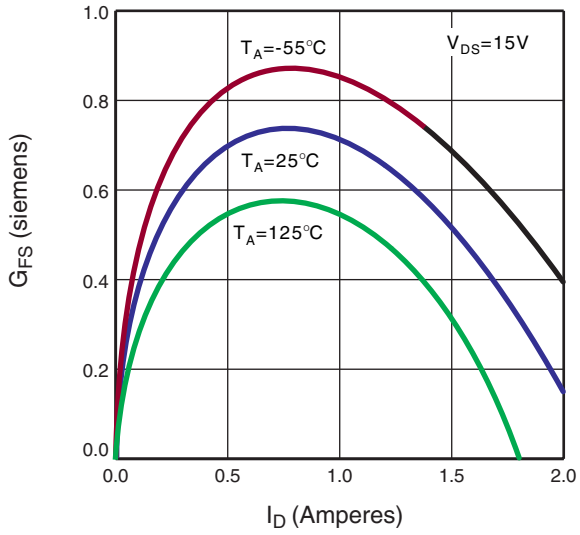
Output Characteristics



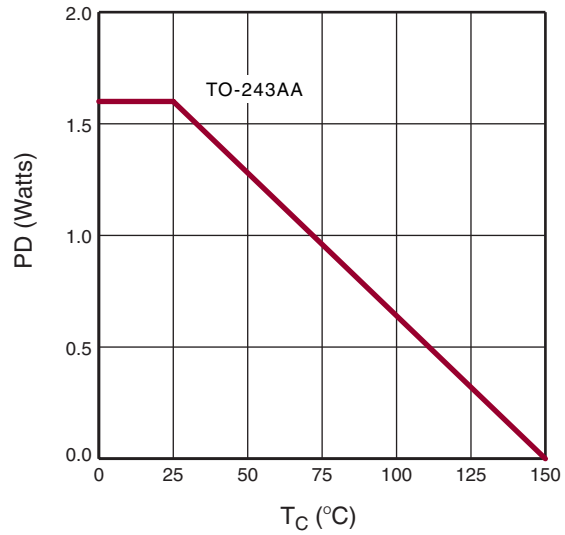
Saturation Characteristics



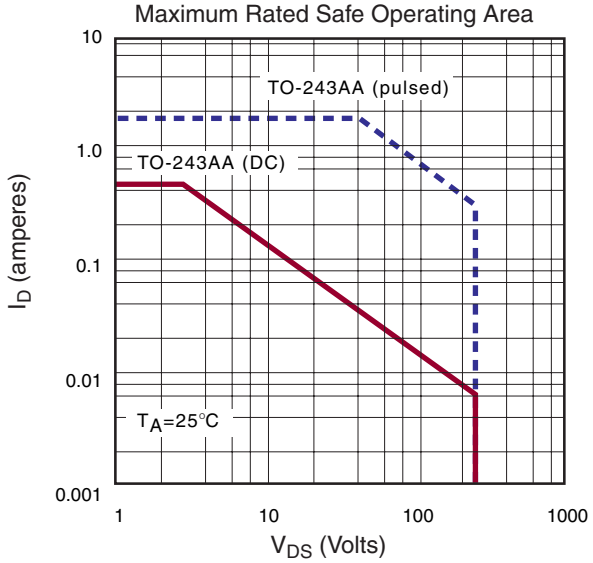
Transconductance vs. Drain Current



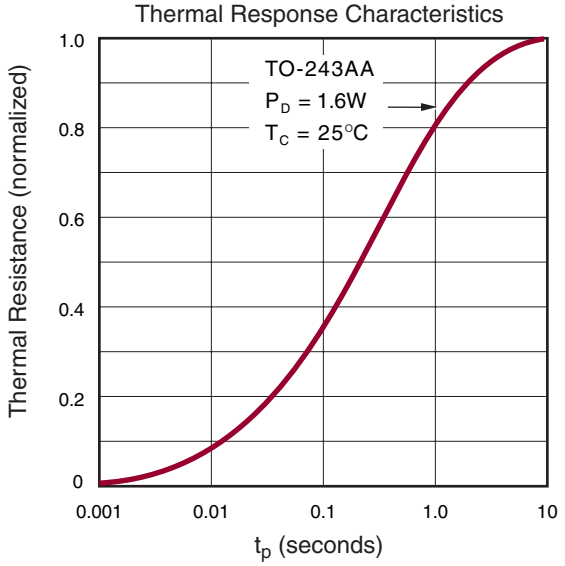
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

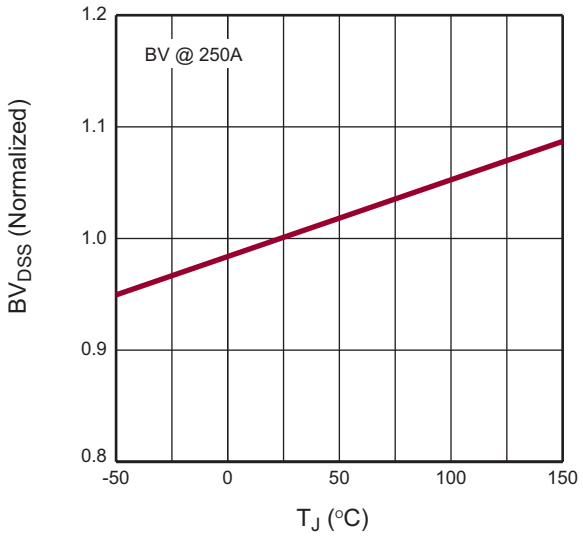


Thermal Response Characteristics

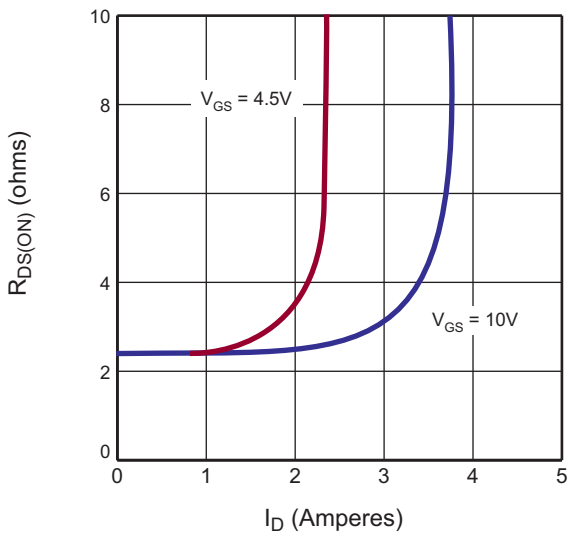


Typical Performance Curves *(cont.)*

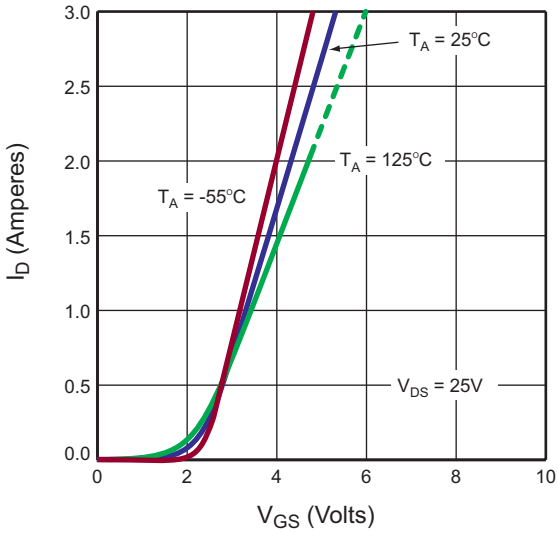
BV_{DSS} Variation with Temperature



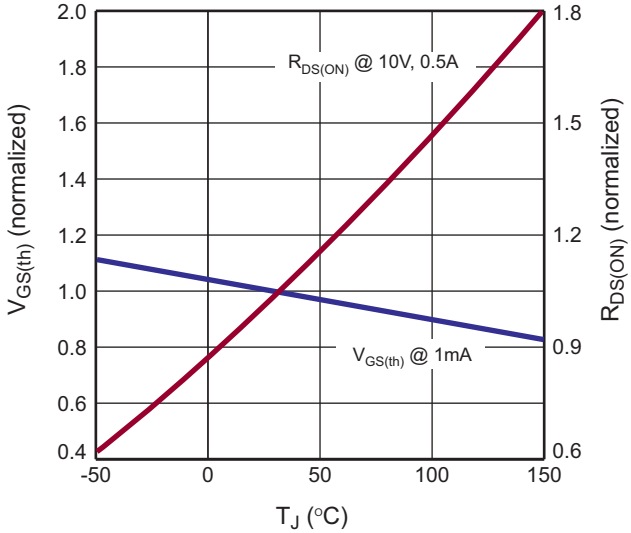
On Resistance vs. Drain Current



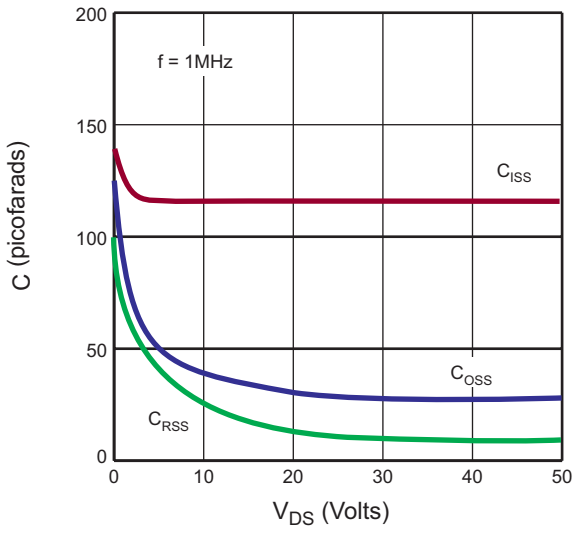
Transfer Characteristics



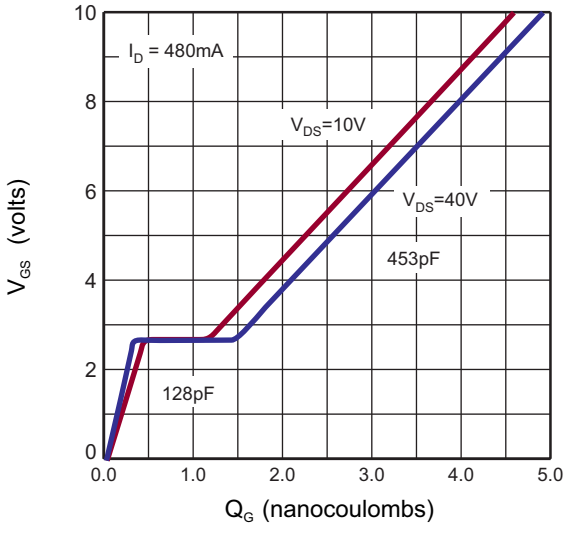
$V_{GS(TH)}$ and $R_{DS(ON)}$ w/ Temperature



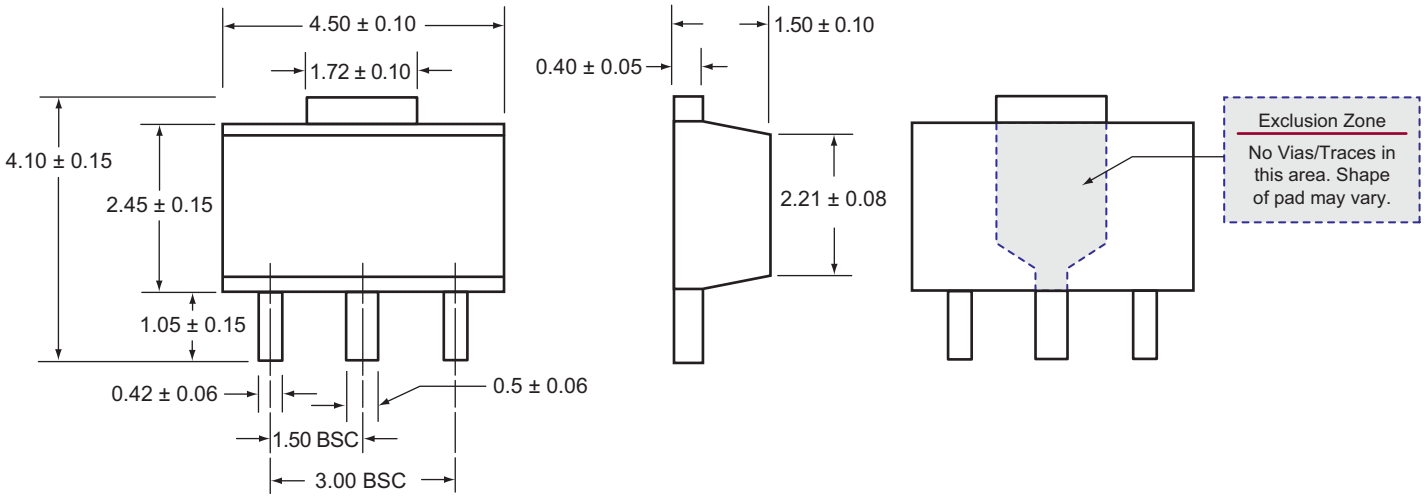
Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



TO-243AA (SOT-89) Package Outline (N8)



Top View **Side View** **Bottom View**

Notes:

1. All dimensions are in millimeters; all angles in degrees.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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