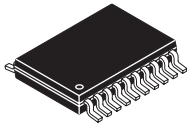
Low Voltage 1:5 Differential LVDS Clock Fanout Buffer

MC100ES8014

The MC100ES8014 is a HSTL differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8014 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

The MC100ES8014 is designed for low skew clock distribution systems and supports clock frequencies up to 400MHz. The device accepts two clock sources. The CLK0 input accepts HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 5 identical, differential HSTL compatible outputs.

1:5 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER



DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E

Features

- 1:5 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 400 MHz operation
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Supports industrial temperature range
- Standard 20 lead TSSOP package

ORDERING INFORMATION

Device	Package
MC100ES8014DT	TSSOP-20
MC100ES8014DTR2	TSSOP-20

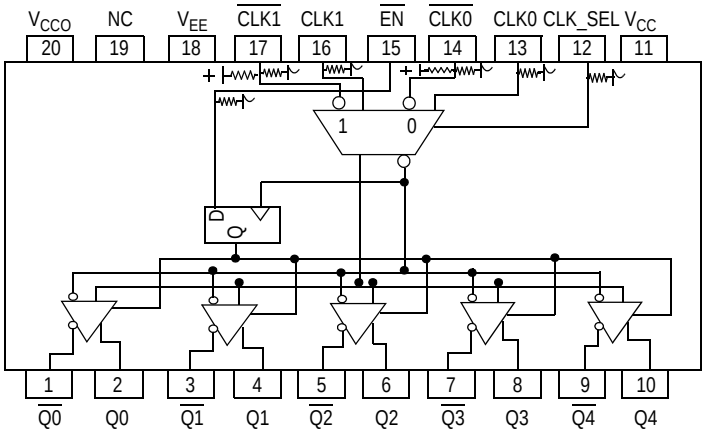


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

Table 1. Pin Description

Pin	Function
CLK0, $\overline{\text{CLK0}}$	HSTL Data Inputs
CLK1, $\overline{\text{CLK1}}$	PECL Data Inputs
Q[0:4], $\overline{\text{Q[0:4]}}$	HSTL Data Outputs
CLK_SEL	LVCMOS Active Clock Select Input
$\overline{\text{EN}}$	LVCMOS Sync Enable
V_{CC}	Positive Supply of device core (3.3V)
V_{CCO}	Positive power supply of the HSTL outputs. All VCCO pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation.
V_{EE}	Negative Supply
nc	no connect

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{EN}}$	0	Q[0:4], $\overline{\text{Q[0:4]}}$ are active. Deassertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0:4] = L, $\overline{\text{Q[0:4]}}$ = H (outputs disabled). Assertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential input voltage[2]	0.2			V	
$V_{X, IN}$	Differential cross point voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input high voltage	V_X + 0.1			V	
V_{IL}	Input low voltage			V_X – 0.1	V	
I_{IN}	Input current			±150	mA	V_{IN} = V_X ± 0.1V
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential input voltage[4]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential cross point voltage[5]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input high voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input low voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input current			±150	mA	V_{IN} = V_{IH} or V_{IN}
LVCMOS control inputs $\overline{EN}$, CLK_SEL						
V_{IL}	Input low voltage			0.8	V	
V_{IH}	Input high voltage	2.0			V	
I_{IN}	Input current			±150	mA	V_{IN} = V_{IH} or V_{IN}
HSTL clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output high voltage	1			V	
V_{OL}	Ouput low voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)
I_{CCO}	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pin (outputs)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential input voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential cross point voltage[4]	0.68		0.9	V	
f_{CLK}	Input Frequency		0 – 400	TBD	MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential input voltage (peak-to-peak)[5]	0.2		1.0	V	
V_{CMR}	Differential cross point voltage[6]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency		0 – 400		MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
HSTL clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output high voltage	1			V	
V_{OL}	Ouput low voltage			0.5	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-output skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%
t_{PDL}	Output disable time[7]	2.5*T +t_{PD}		3.5*T +t_{PD}	ns	T = CLK period
t_{PLD}	Output enable time[8]	3*T +t_{PD}		4*T +t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to $V_{TT.}$
3. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{EN}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{EN}$ assertion to output enabled (active).

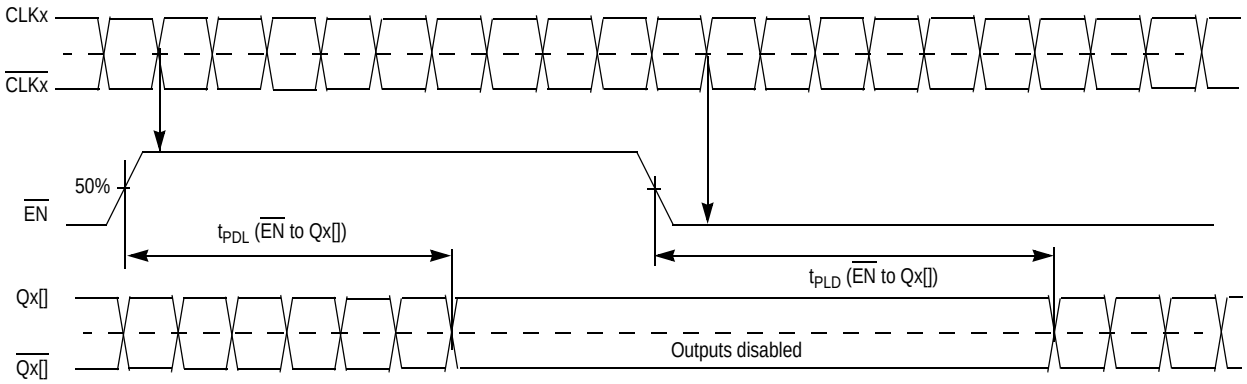


Figure 2. MC100ES8014 AC Test Reference

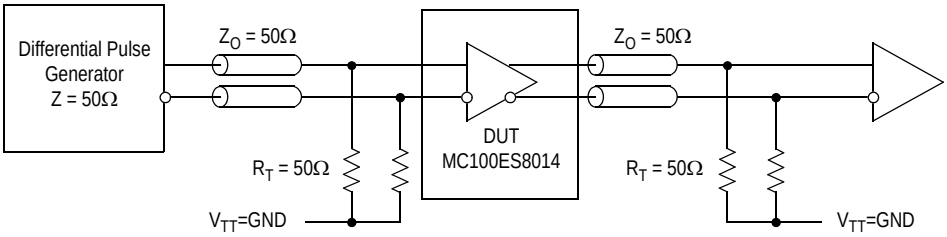


Figure 3. MC100ES8014 AC Test Reference

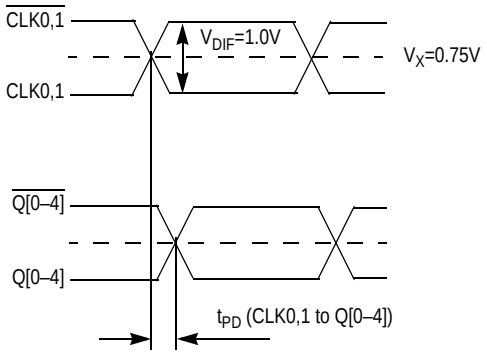


Figure 4. MC100ES8014 AC Reference Measurement Waveform (HSTL Input)

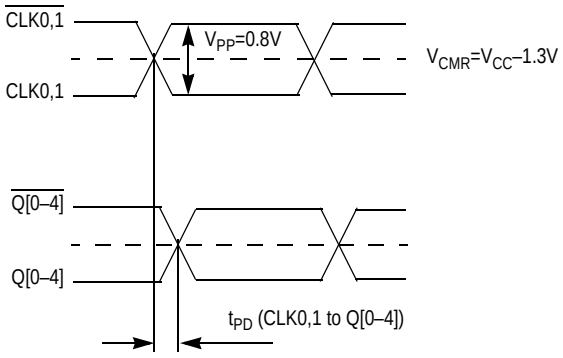
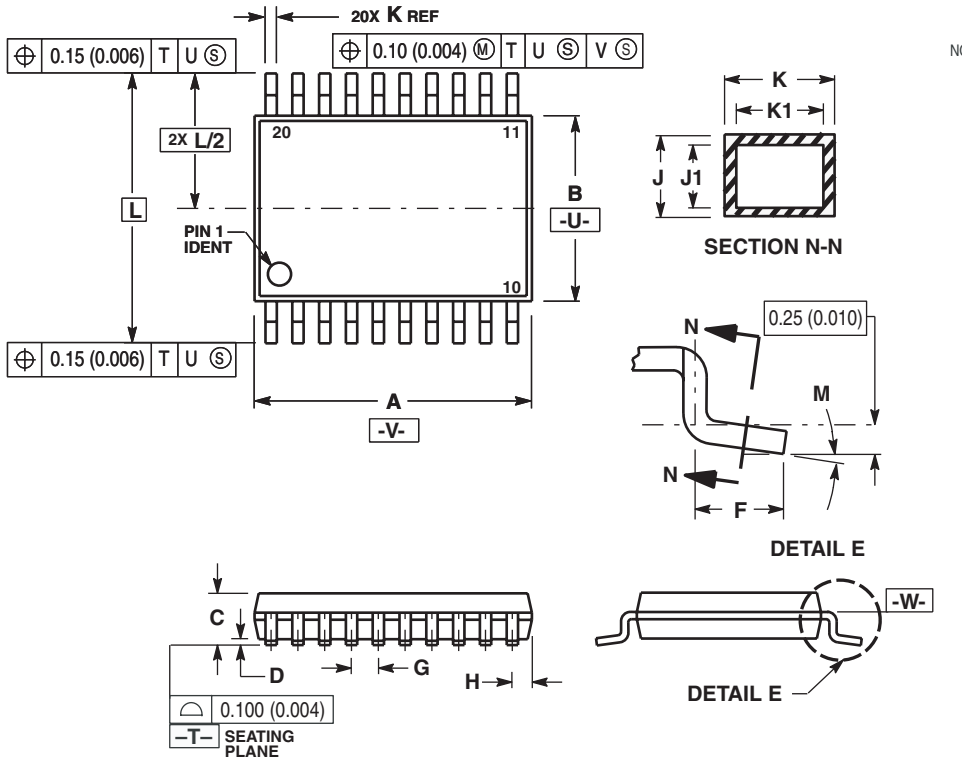


Figure 5. MC100ES8014 AC Reference Measurement Waveform (PECL Input)

PACKAGE DIMENSIONS

DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND BE ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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Printed in USA

XX-XXXX-XXXXX