Spread Spectrum System FTG for SMP Systems

Features

- **Maximized EMI suppression using Cypress's spread spectrum technology (0.5% down spread)**
- **Seven skew-controlled copies of CPU and 16.667-MHz synchronous APIC output**
- **Two copies of fixed-frequency 33-MHz outputs**
- **Four copies of 66-MHz fixed-frequency outputs**
- **Two copies of CPU/2 outputs for synchronous memory reference**
- **One copy of 48-MHz USB output**
- **Two copies of 14.31818-MHz reference clock**
- **Programmable to 133- or 100-MHz operation**
- **Power management control pins for clock stop and shut down**
- **Available in 56-pin SSOP**

Key Specifications

Supply Voltages: ..... V_{DDQ3} = 3.3V±5%
V_{DDQ2} = 2.5V±5%

CPU Output Jitter: ..... 150 ps

CPUdiv2, 3V33, APIC Output Jitter: ..... 250 ps

CPU, 3V33 Output Edge Rate: ..... ≥1 V/ns

48-MHz, 3V66, REF Output Jitter: ..... 500 ps

CPU0:6, CPUdiv2_0:1 Output Skew: ..... 175 ps

3V66, APIC0:6, 3V33 Output Skew: ..... 250 ps

CPU to 3V66 Output Offset: ..... 0.0 to 1.5 ns (CPU leads)

3V66 to 3V33 Output Offset: ..... 1.5 to 3.0 ns (3V66 leads)

CPU to APIC Output Offset: ..... 1 to 3.0 ns (CPU Leads)

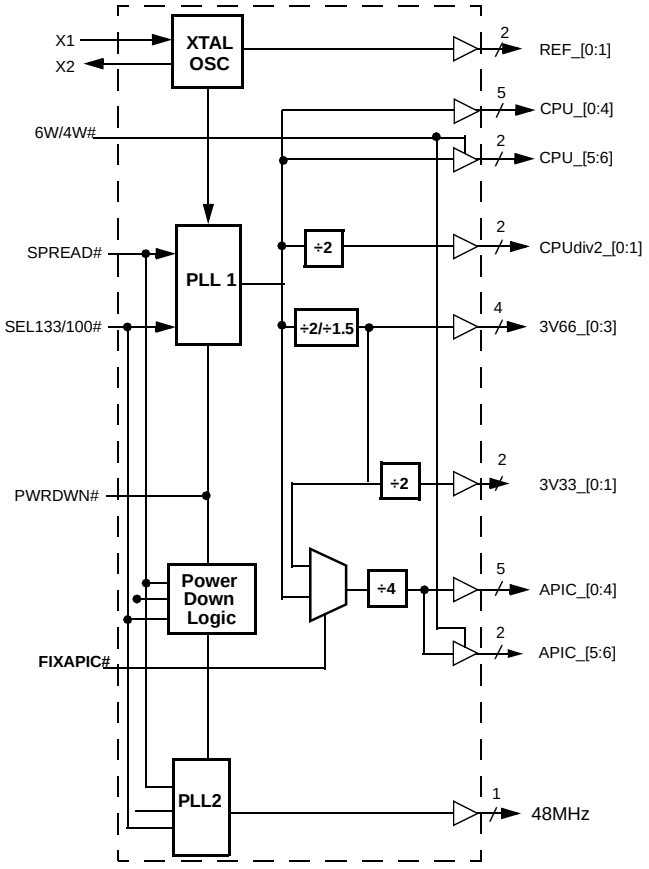
CPU to 3V33 Output Offsets: ..... 1.5 to 4.0 ns (CPU Leads)

Logic inputs, except SEL133/100#, have 250-kΩ pull-up resistors.

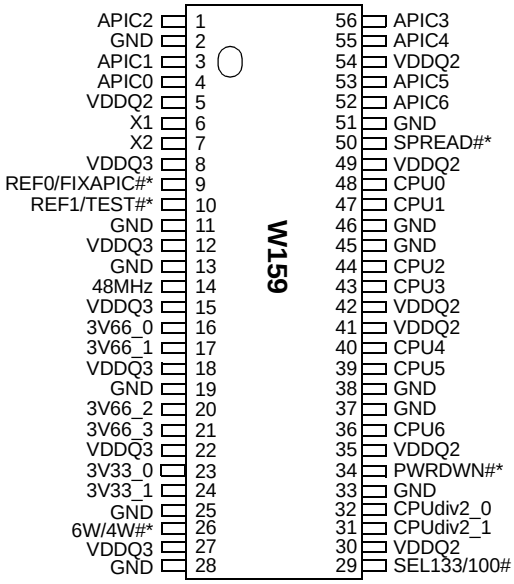
Table 1. Pin Selectable Frequency

SEL133/100#	CPU0:6 (MHz)	PCI
1	133 MHz	33.3 MHz
0	100 MHz	33.3 MHz

Block Diagram



Pin Configuration[1]



Note:

1. Pins denoted by * have a 250 kΩ pull-up resistor. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:6	48, 47, 44, 43, 40, 39, 36	O	***CPU Clock Outputs 0 through 6:*** These seven CPU clocks run at a frequency set by SEL133/100#. Output voltage swing is set by the voltage applied to VDDQ2. For 4-way SMP systems that do not require more than 5 CPU outputs, CPU5 and CPU6 can be disabled by asserting 6W/4W# during power-up.
CPUdiv2_ 0:1	32, 31	O	***Synchronous Memory Reference Clock Output 0 through 1:*** Reference clock for Direct RDRAM clock generators running at 1/2 CPU clock frequency. Output voltage swing is set by the voltage applied to VDDQ2. For systems using SDRAM, CPUdiv2_0:1 output can be disabled by tying VDDQ2 on pin 35 to GND.
3V33_0:1	23, 24	O	***33-MHz Fixed-Frequency Output:*** These are fixed-frequency outputs that can be used to drive PCI devices.
REF0/ FIXAPIC#*	9	I/O	***14.318-MHz Reference Clock Output/APIC Speed Select:*** During normal operations, this is a 3.3V 14.318-MHz reference output. During power-up, it is sampled to determine the operating frequency of APIC. If the sample is a “1,” APIC will be set at CPU/4. If it is a “0,” APIC will be fixed at 16.667 MHz.
REF1/TEST#*	10	I/O	***14.318-MHz Reference Clock Output/Test Mode:*** During normal operations, this is a 3.3V 14.318-MHz reference output. The input is sampled at power-up to determine if the device should initialize for normal operations or test mode.
APIC0:6	4, 3, 1, 56, 55 53, 52	O	***Synchronous I/OAPIC Clock Outputs:*** APIC output frequency is determined by FIXAPIC# strapping. For 4-way SMP systems that do not require more than 5 APIC outputs, APIC5 and APIC6 can be disabled by asserting 4W/6W# during power up.
48MHz	14	O	***48-MHz Output:*** Fixed 48-MHz USB output. Output voltage swing is controlled by voltage applied to VDDQ3.
3V66_0:3	16, 17, 20, 21	O	***66-MHz Output 0 through 3:*** Fixed 66-MHz outputs.
SEL133/100#	29	I	***Frequency Selection Input:*** 3.3V LVTTL-compatible input that selects CPU output frequency as shown in *Table 1*.
X1	6	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318-MHz crystal or other reference signal.
X2	7	O	***Crystal Connection:*** An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
6W/4W#*	26	I	***4-way/6-way Output Select:*** This input can be changed after initialization and has an internal pull-up resistor. If left unconnected during power-up, the outputs are configured so that all CPU and APIC outputs are active. If it is pulled down during power-up, CPU5:6 and APIC5:6 will be disabled.
SPREAD#	50	I	***Active LOW Spread Spectrum Enable:*** 3.3V LVTTL-compatible input that enables spread spectrum mode when held LOW.
PWRDWN#	34	I	***Active LOW Power Down Input:*** 3.3V LVTTL-compatible asynchronous input that requests the device to enter power down mode.
GND	2, 11, 13, 19, 25, 28, 33, 37, 38, 45, 46, 51	G	***Ground Connection***
VDDQ3	8, 12, 15, 18, 22, 27	P	***Power Connection:*** Power supply for 3V33, 3V66, 48MHz, and REF output buffers, core circuitry and PLL circuitry. Connect to 3.3V supply.
VDDQ2	5, 30, 35, 41, 42, 49, 54	P	***Power Connection:*** Power supply for APIC and CPU, CPUdiv2 output buffers. Connect to 2.5V supply.

Overview

The W159 is designed to provide the essential frequency sources to work with advanced multiprocessing Intel® architecture platforms. Split voltage supply signaling provides 2.5V and 3.3V clock frequencies operating up to 133 MHz.

From a low-cost 14.31818-MHz reference crystal oscillator, the W159 generates 2.5V clock outputs to support CPUs, core logic chip set, and Direct RDRAM clock generators. It also provides skew-controlled PCI and IOAPIC clocks synchronous to CPU clock, 48-MHz Universal Serial Bus (USB) clock, and replicates the 14.31818-MHz reference clock.

All CPU, PCI, and IOAPIC clocks can be synchronously modulated for spread spectrum operations. Cypress employs proprietary techniques that provide the maximum EMI reduction while minimizing the clock skews that could reduce system timing margins. The use of spread spectrum modulation is controlled by an external signal input.

The W159 also includes power management control inputs. By using these inputs, system logic can stop CPU and/or PCI clocks or power down the entire device to conserve system power.

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$

Where P is the percentage of deviation and F is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is –0.5% downspread. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for the SPREAD# input pin.

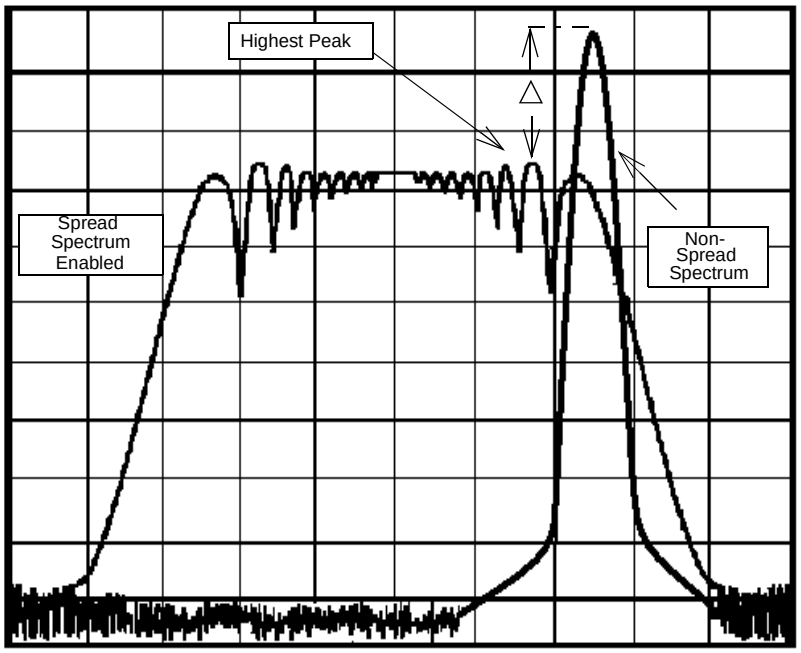


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

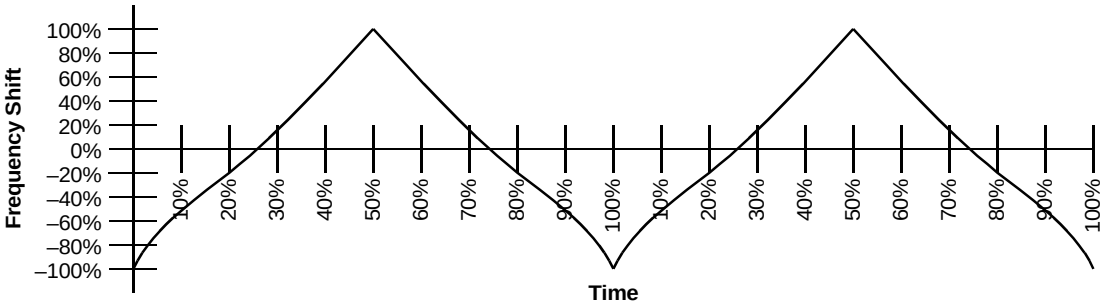


Figure 2. Modulation Waveform Profile

Maximum Allowed Current

Table 2. Maximum Allowed Current

Condition	Max. 2.5V supply consumption Max. discrete cap loads, V_{DDQ2}=2.625V All static inputs=V_{DDQ3} or V_{SS}	Max. 3.3V supply consumption Max. discrete cap loads, V_{DDQ3}=3.465V All static inputs=V_{DDQ3} or V_{SS}
Power-down Mode (PWRDWN#=0)	300 µA	500 µA
Full Active 100 MHz SEL133/100#=0	120 mA	160 mA
Full Active 133 MHz SEL133/100#=1	120 mA	160 mA

Table 3. Clock Enable Configuration[2, 3, 4]

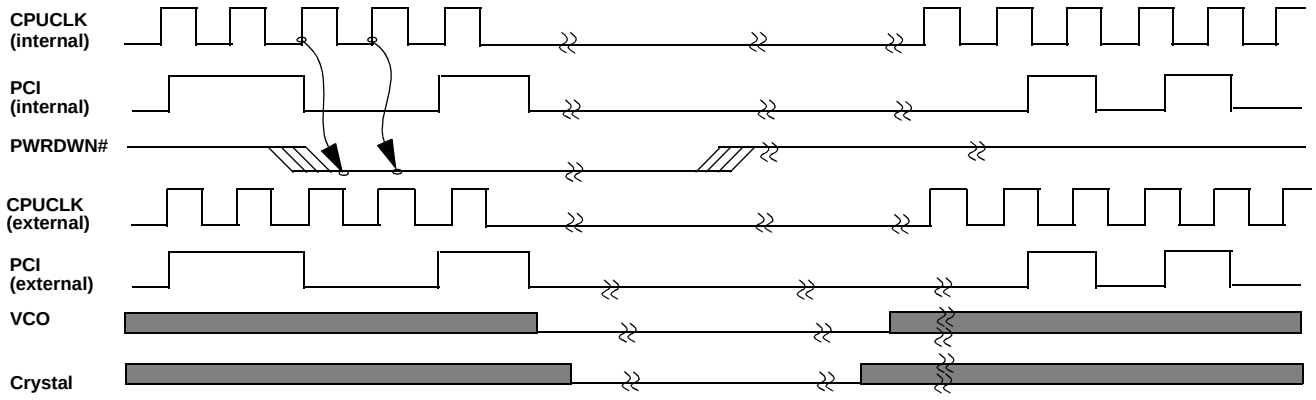
PWRDWN#	CPUCLK	CPUdiv2	APIC	3V66	3V33	48MHz	REF	OSC.	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Table 4. Power Management State Transition

Signal	Signal State	Latency[5]
PWRDWN#	1 (normal operation)	3 ms
	0 (power down)	2 PCI clocks (max.)

Timing Diagram

PWRDWN# Timing Diagram[6, 7, 8, 9, 10]



Notes:
2. LOW means outputs held static LOW as per latency requirement below.
3. ON means active.
4. PWRDWN# pulled LOW, impacts all outputs including REF and 48-MHz outputs.
5. Power-up latency is when PWRDWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.
6. All internal timing is referenced to the CPUCLK.
7. The internal label means inside the chip and is a reference only. This, in fact, may not be the way that the control is designed.
8. PWRDWN is an asynchronous input and metastable conditions could exist. This signal is synchronized by the W159 internally.
9. The shaded sections on the VCO and the Crystal signals indicate an active clock.
10. Diagrams shown with respect to 133 MHz. Similar operation when CPUCLK is 100 MHz.

Absolute Maximum Ratings[11]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Supply Current						
$I_{DD-3.3V}$	Combined 3.3V Supply Current	CPU0:3 =133 MHz[12]			160	mA
$I_{DD-2.5}$	Combined 2.5V Supply Current	CPU0:3 =133 MHz[12]			90	mA
Logic Inputs (All referenced to V_{DDQ3} = 3.3V)						
V_{IL}	Input Low Voltage		GND – 0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[13]				–25	µA
I_{IH}	Input High Current[13]				10	µA
I_{IL}	Input Low Current, SEL133/100#[13]				–5	µA
I_{IH}	Input High Current, SEL133/100#[13]				5	µA
Clock Outputs						
CPU, CPUdiv2, IOAPIC (Referenced to V_{DDQ2})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	V_{OL} = 1.25V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.25V	45	65	100	mA
48MHz, REF (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	45	65	100	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	45	65	100	mA
3V33, 3V66 (Referenced to V_{DDQ3})		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	70	100	145	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	65	95	135	mA

Notes:

11. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
12. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
13. W159 logic inputs have internal pull-up devices, except SEL133/100# (pull-ups not CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[14]			1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[15]			18		pF
$C_{IN,X1}$	X1 Input Capacitance[16]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

3.3V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[17]

3V66 Clock Outputs, 3V66_0:3 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency	Note 18		66.6		MHz
t_H	High Time	Duration of clock cycle above 2.4V	4.95			ns
t_L	Low Time	Duration of clock cycle below 0.4V	4.55			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
t_O	CPU to 3V66 Clock Skew	Covers all 3V66 outputs. Measured on rising edge at 1.5V. CPU leads 3V66 outputs.	0		1.5	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

Notes:
14. X1 input threshold voltage (typical) is $V_{DD}/2$.
15. The W159 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
16. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
17. Period, jitter, offset, and skew measured on rising edge at 1.5V.
18. 3V66 is CPU/2 for CPU =133 MHz and (2 x CPU)/3 for CPU = 100 MHz.

3V33 Clock Outputs, 3V33_0:1 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
t_P	Period	Measured on rising edge at 1.5V[19]	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	3V66 to 3V33 Clock Skew	Covers all 3V66 outputs. Measured on rising edge at 1.5V. 3V66 leads 3V33 output.	1.5		3.0	ns
t_q	CPU to 3V33 Clock Skew	Covers all 3V33 outputs. Measured on rising edge at 1.5V. CPU leads 3V33 output.	1.5		4.0	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF Clock Outputs, REF0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

Note:
19. 3V33 clock is CPU/4 for CPU = 133 MHz and CPU/3 for CPU = 100 MHz.

48-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

2.5V AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5%
f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[20]

CPU Clock Outputs, CPU0:6 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	7.5		7.65	10		10.2	ns
t_H	High Time	Duration of clock cycle above 2.0V	1.87			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	1.67			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

Note:
20. Period, Jitter, offset, and skew measured on rising edge at 1.25V.

CPUdiv2 Clock Outputs, CPUdiv2_0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 133 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.3	20		20.4	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.25			7.5			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.05			7.3			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

APIC Clock Outputs, APIC0:2 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min	Typ	Max	Unit
f	Frequency	Note 21		16.67		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

Note:
21. APIC clock is CPU/8 for CPU = 133 MHz and CPU/6 for CPU = 100 MHz.

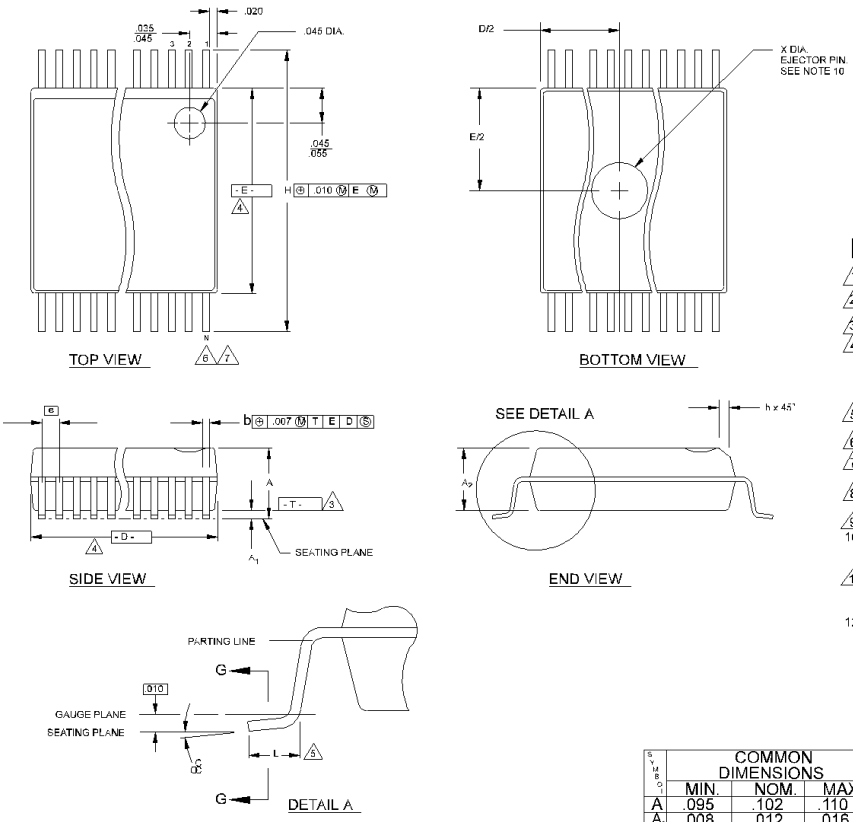
Ordering Information

Ordering Code	Package Name	Package Type
W159	H	56-pin SSOP (300 mils)

Intel is a registered trademark of Intel Corporation.

Package Diagram

56-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			NOTE 6
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110	AA	.620	.625	.630	48
A_1	.008	.012	.016	AB	.720	.725	.730	56
A_2	.088	.090	.092					
b	.008	.010	.0135					
b_1	.008	.010	.012					
c	.005	-	.010					
c_1	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.296	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			NOTE 6
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34					
b	0.203	0.254	0.343					
b_1	0.203	0.254	0.305					
c	0.127	-	0.254					
c_1	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS

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Document Title: W159 Spread Spectrum System FTG for SMP Systems Document Number: 38-07163				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110273	11/11/01	SZV	Change from Spec number: 38-00818 to 38-07163
*A	122804	12/14/02	RBI	Add Power up Requirements to Operating Conditions Information