32MB - 4M x 64 SDRAM UNBUFFERED

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 168 pin DIMM JEDEC

DESCRIPTION

The W3DG644V is a 4M x 64 synchronous DRAM module which consists of four 4M x 16 SDRAM components in TSOP II package and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 pin DIMM multilayer FR4 Substrate.

*This product is under development, is not qualified or characterized and is subject to change without notice.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK
1	V_{SS}	29	DQM1	57	DQ18	85	V_{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	DNU	59	V_{CC}	87	DQ33	115	RAS#	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	NC	90	V_{CC}	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	DNU
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	NC	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V_{CC}	101	DQ45	129	NC	157	V_{CC}
18	V_{CC}	46	DQM2	74	DQ28	102	V_{CC}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	V_{CC}	77	DQ31	105	NC	133	V_{CC}	161	DQ63
22	NC	50	NC	78	V_{SS}	106	NC	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CLK2	107	V_{SS}	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	*WP	109	NC	137	NC	165	**SA0
26	V_{CC}	54	V_{SS}	82	**SDA	110	V_{CC}	138	V_{SS}	166	**SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	V_{CC}	112	DQM4	140	DQ49	168	V_{CC}

PIN NAMES

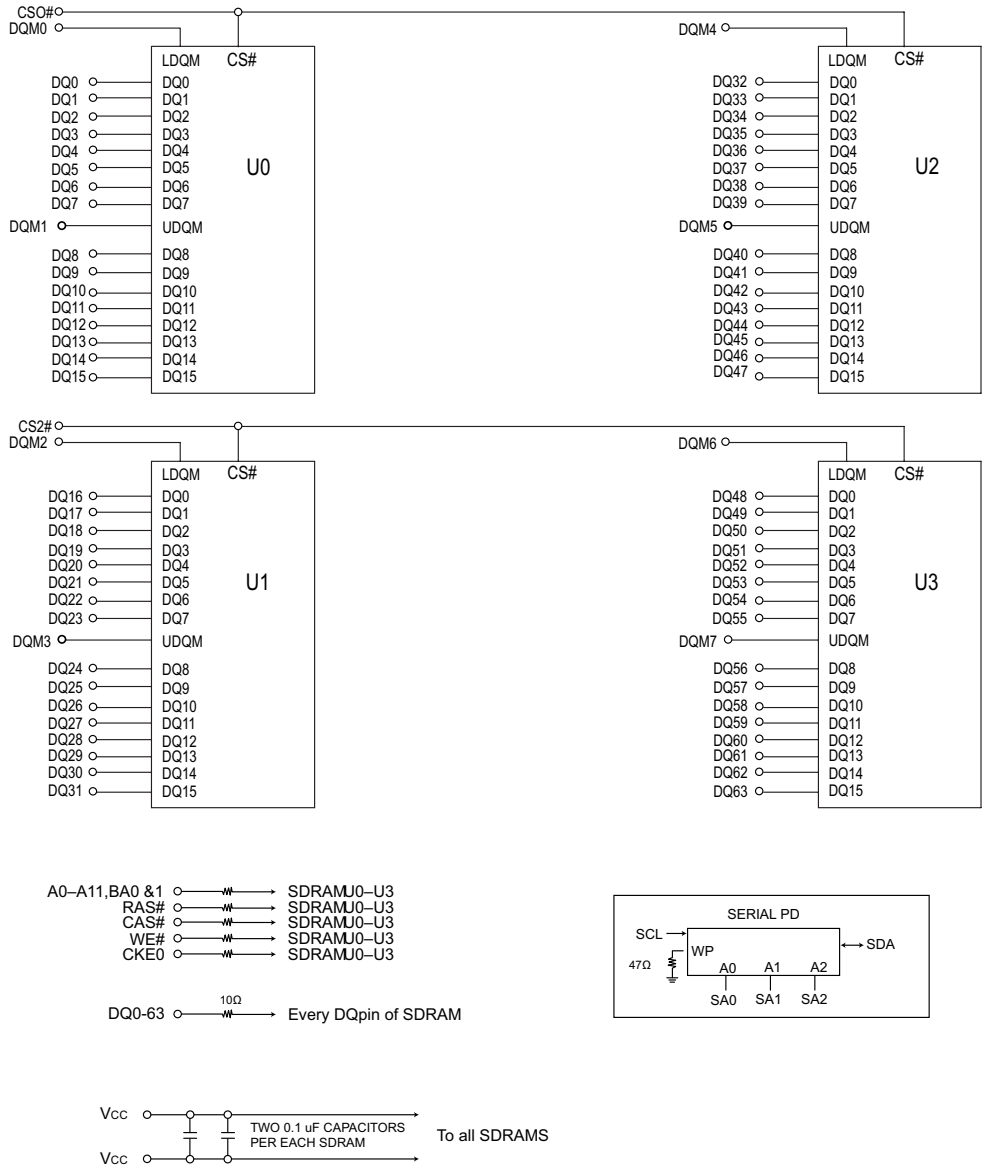
A0 – A11	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0,CLK2	Clock input
CKE0	Clock Enable input
CS0#,CS2#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7#	DQM
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

* WP (write protect) option available on pin 81, see ordering information on page 5.

** These pins should be NC in the system which does not support SPD.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	4	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CCQ}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	A	3

Note:

1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 23°C, f = 1MHz, V_{CC} = 3.3V, V_{REF}=1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	25	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	25	pF
Input Capacitance (CKE0)	C_{IN3}	25	pF
Input Capacitance (CLK0,CLK2)	C_{IN4}	13	pF
Input Capacitance (CS0#,CS2#)	C_{IN5}	15	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	8	pF
Input Capacitance (BA0-BA1)	C_{IN7}	25	pF
Data input/output capacitance (DQ0-DQ63)	C_{OUT}	10	pF

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, 0°C ≤ T_A ≤ 70°C)

Parameters	Symbol	Conditions	Versions		Units	Note
			133	100		
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0mA	300	300	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	4		mA	
	I_{CC2PS}	CKE & CK ≤ V_{IL}(max), t_{CC} = ∞	4		mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} =10ns Input signals are charged one time during 20	48		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CK ≤ V_{IL}(max), t_{CC}= ∞ Input signals are stable	24		mA	
Active standby current in power-down mode	I_{CC3P}	CKE ≥ V_{IL}(max), t_{CC} = 10ns	8		mA	
	I_{CC3PS}	CKE & CK ≤ V_{IL}(max), t_{CC} = ∞	8			
Active standby in current non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 10ns Input signals are charged one time during 20ns	80		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CK ≤ V_{IL}(max), t_{CC} = ∞ input signals are stable	40		mA	
Operating current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CK	460	460	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	360	360	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	4		mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.

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ORDERING INFORMATION

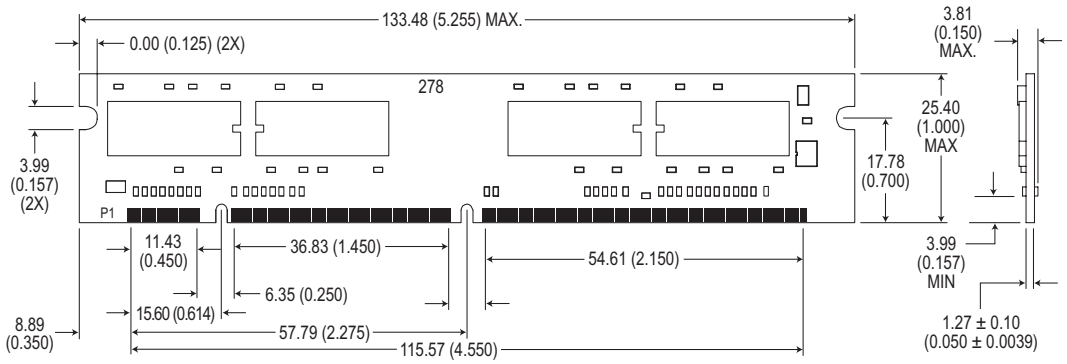
Part Number	Speed	CAS Latency	Height*
W3DG644V10D2	100MHz	CL=2	25.40 (1.00")
W3DG644V7D2	133MHz	CL=2	25.40 (1.00")
W3DG644V75D2	133MHz	CL=3	25.40 (1.00")

Note: Modules are available in industrial temperature - 40°C ≤ T_A ≤ 85°C.
Add an "I" to the end of the part number.

Part Number	Speed	CAS Latency	Height*
W3DG634V10D2	100MHz	CL=2	25.40 (1.00")
W3DG634V7D2	133MHz	CL=2	25.40 (1.00")
W3DG634V75D2	133MHz	CL=3	25.40 (1.00")

Note: Available with WP (write protect) on pin 81.

PACKAGE DIMENSIONS



*** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)**

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 0	0.1 Created 0.2 Updated CAP and I_{DD} specs.	7-2004	Advanced
Rev 1	Moved from Advanced to Preliminary	7-2004	Preliminary