Ordering number : ENA1046

SANYO Semiconductors
DATA SHEET

LV1117N/NV — Bi-CMOS IC Surround Processor ICs for Electronic Volume Control

Overview

The LV1117N/NV are sound processor ICs developed for use in TV sets.
They incorporate the surround processing functions including (AViSS), pseudo stereo function, (L+R) output, and the major functional blocks of an electronic volume control IC.

Features

- Input function SW (4ch stereo inputs [L, R]).
- Line out (through output).
- Input gain control (−6dB, −4dB, 0dB, 4dB, 6dB: 5 positions).
- AViSS (ON/OFF/6-stage level control).
- Tone control (BASS: ±20dB, TREBLE: ±18dB [in 2dB steps]).
- Volume control (0dB to −14dB: 1dB step/−14dB to −80dB: 2dB steps/−∞=−82dB).
- Balance control.
- Through mode/Mute mode.
- Pseudo stereo function (ON/OFF/MONO).
- L+R output with LPF (Mute + 7-stage level control: 8 positions).
- I^2C bus control.
- Parallel output ports (4pin).

* Initial gain of L+R AMP can be controlled by the resistance value of external resistor.

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		10.5	V
Allowable power dissipation 1	Pd max1	Ta ≤ 70°C, DIP	700	mW
Allowable power dissipation 2	Pd max2	Ta ≤ 70°C *, SSOP	700	mW
Operating temperature	Topr		-25 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note *: Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy board

Operating Condtions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		9.0	V
Operating supply voltage 1	V_{CC} opg1	DIP	5.0 to 10.0	V
Operating supply voltage 2	V_{CC} opg2	SSOP	5.0 to 9.0	V
Control data				
"H" level voltage	V_{IH}		2.0 to 5.5	V
"L" level voltage	V_{IL}		0.0 to 1.0	V
Pulse width	tϕw		1.0	μs
Hold time	thold		1.0	μs
Operating frequency	fopg		100	kHz

Electrical Characteristics at Ta = 25°C, V_{CC} = 9.0V, fin = 1kHz, V_{IN} = 300mVrms = 0dB, R_L = 10kΩ

(Input=L/Rch-A, Output=L/R-VROUT)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}			48		mA
Total through (Total through mode, Volume control: 0dB)						
Voltage gain	VG_T		-1.6	-0.6	+0.6	dB
Maximum output voltage	VO_T	THD=1%	2.0	2.6		Vrms
Total harmonic distortion	THD_T	DIN AUDIO		0.03	0.1	%
Output noise voltage	VNO_T	DIN AUDIO		-93	-85	dBV
Cross talk	CT_T	DIN AUDIO	85	93		dB
Matrix through (Matrix mode, Input gain: 0dB, Volume control: 0dB)						
Voltage gain	VG_F		-1.7	-0.7	+0.7	dB
Maximum output voltage	VO_M	THD=1%	1.5	2.0		Vrms
Total harmonic distortion	THD_M	DIN AUDIO		0.04	0.1	%
Output noise voltage	VNO_M	DIN AUDIO		-92	-83	dBV
Cross talk	CT_M	DIN AUDIO	85	91		dB
MONO mode (MONO mode, Input gain: 0dB, Volume control: 0dB)						
Maximum output voltage	VO_S	THD=1%	1.5	2.0		Vrms
Total harmonic distortion	THD_S	DIN AUDIO		0.04	0.5	%
Output noise voltage	VNO_S	DIN AUDIO		-92	-82	dBV
Surround (Surround mode-A, Input gain: 0dB, Volume control: 0dB)						
Maximum output voltage	VO_S	THD=1%	1.5	2.0		Vrms
Total harmonic distortion	THD_S	DIN AUDIO		0.2	0.5	%
Output noise voltage	VNO_S	DIN AUDIO		-90	-81	dBV
Pseudo stereo (Pseudo stereo mode, Input gain: 0dB, Volume control: 0dB)						
Maximum output voltage	VO_S	THD=1%	1.5	2.0		Vrms
Total harmonic distortion	THD_S	DIN AUDIO		0.07	0.5	%
Output noise voltage	VNO_S	DIN AUDIO		-90	-82	dBV

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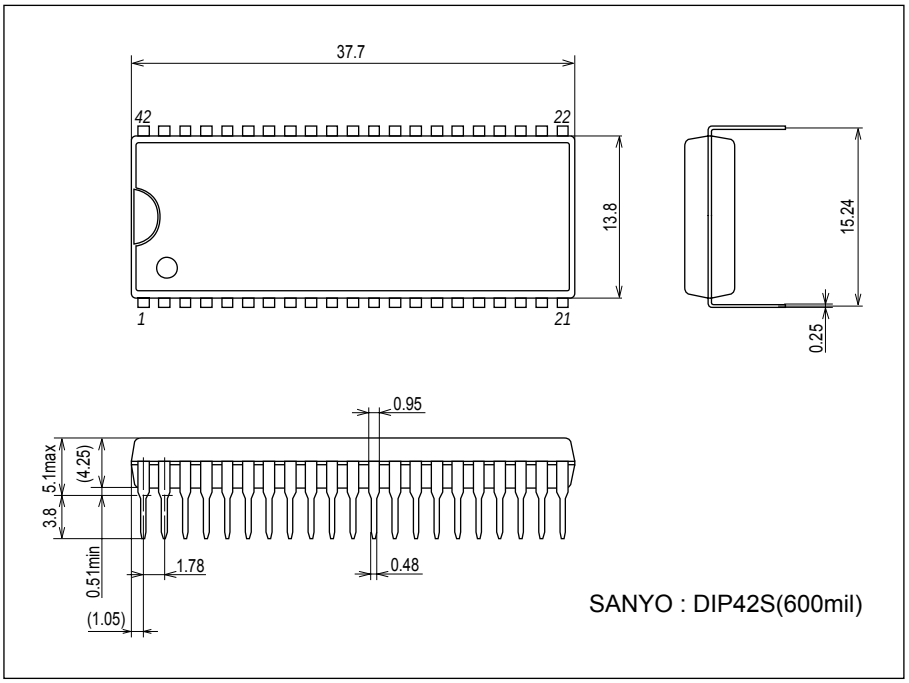
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Bass band EQ (Matrix through mode, Input gain: 0dB, Volume control: 0dB)						
Control Range	Geq_B	Max. Boost/Cut	±17	±20	±23	dB
Step resolution	$Estep_B$		1.0	2.0	3.0	dB
Treble band EQ (Matrix through mode, Input gain: 0dB, Volume control: 0dB)						
Control Range	Geq_T	Max. Boost/Cut	±15	±18	±21	dB
Step resolution	$Estep_T$		1.0	2.0	3.0	dB
L+R output (Output=L+R-OUT, Step=0dB, L+R_Step=Step4)						
Voltage gain	VG_F		-2.3	-1.3	-0.3	dB
Maximum output voltage	VOF	THD=1%	2.0	2.5		Vrms
Total harmonic distortion	THD_F	DIN AUDIO		0.03	0.1	%
Output noise voltage	VNO_F	DIN AUDIO		-99	-85	dBV
Port Output (20/21/22/23pin)						
Low level output voltage	V_{OL}	I_O=1mA			0.3	V
Port output sink Current	I_O				1.0	mA

Note: The output wave form becomes big depending on the surround or tone control setting. Please make sure the output waveform is not distorted. If the waveform is distorted, reduce the gain setting of surround, tone control, or input signal level.

Package Dimensions

unit : mm (typ)

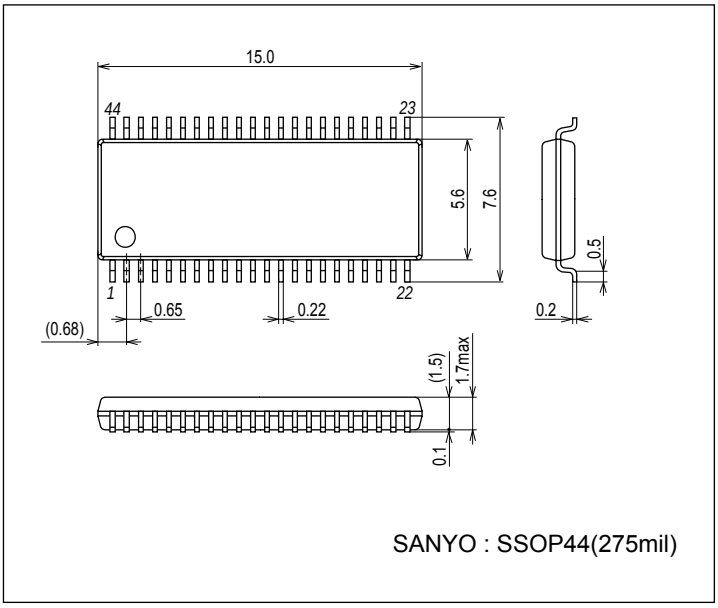
3025C [LV1117N]



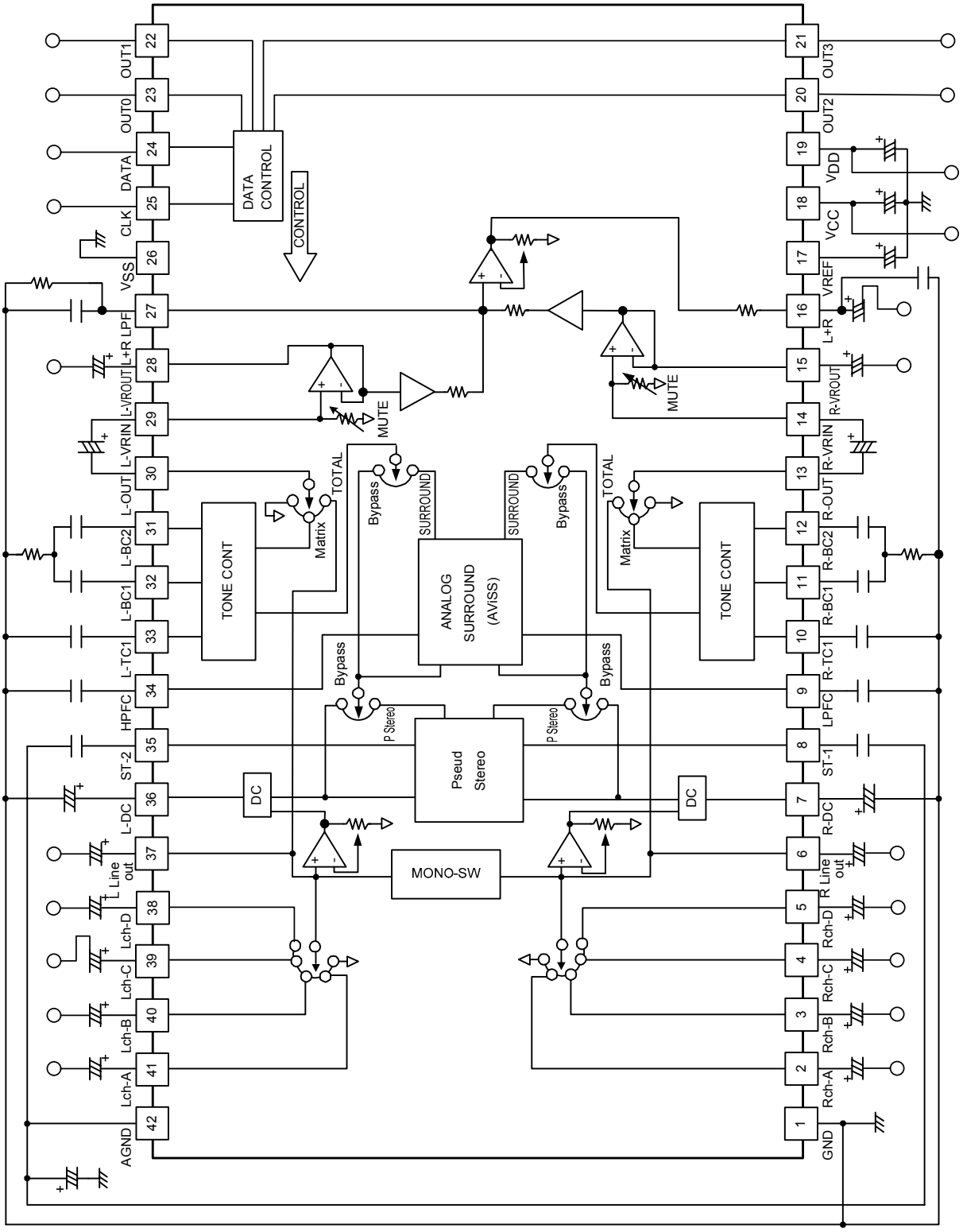
Package Dimensions

unit : mm (typ)

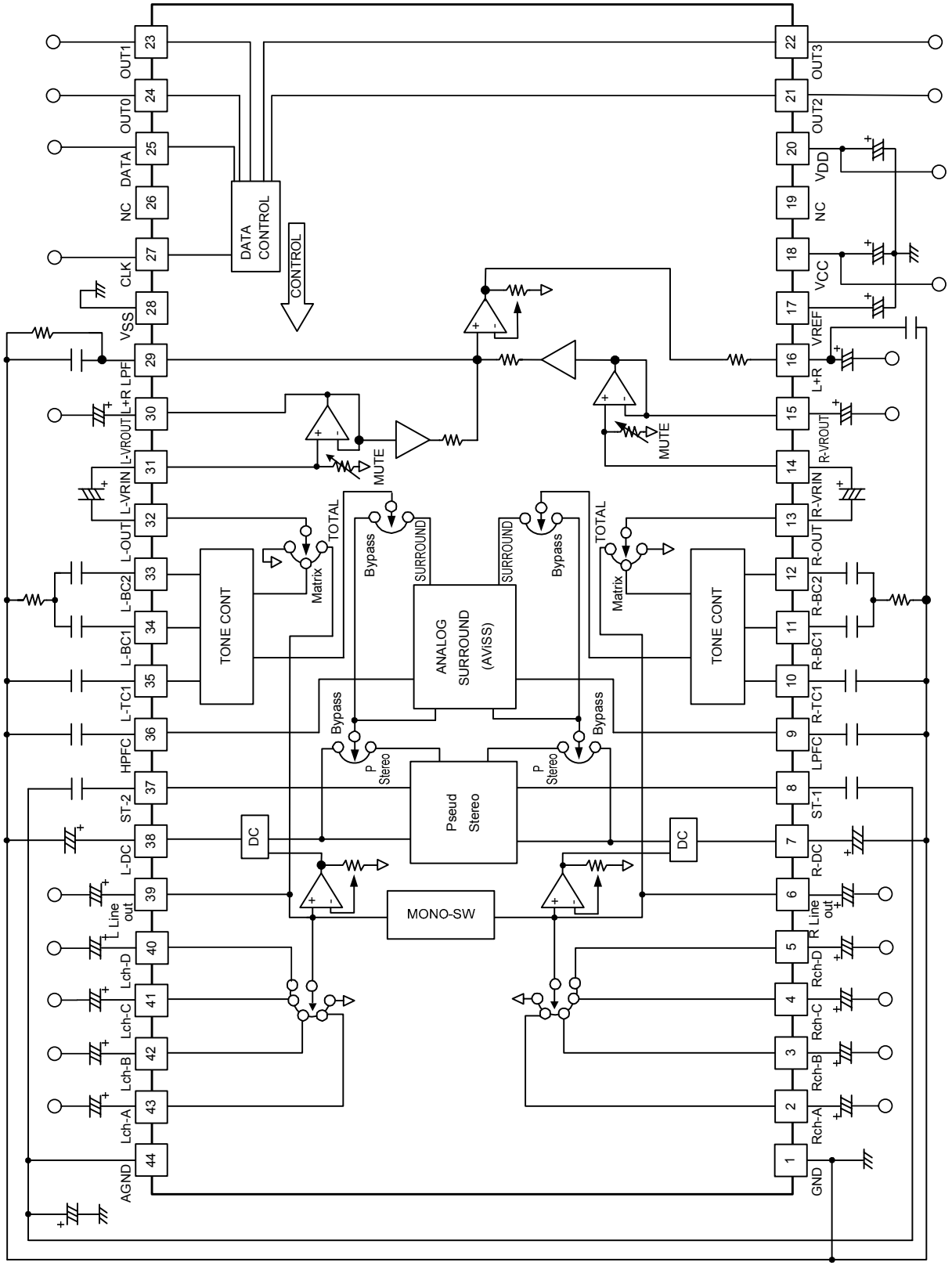
3277 [LV1117NV]



Block Diagram [LV1117N]



Block Diagram [LV1117NV]



I²C BUS Control Signal

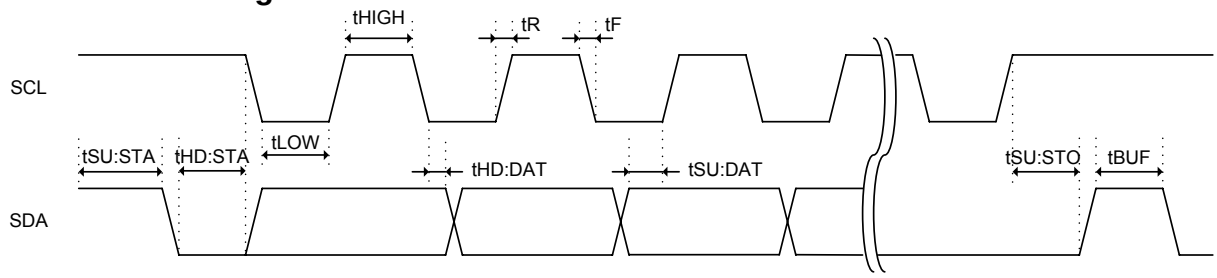
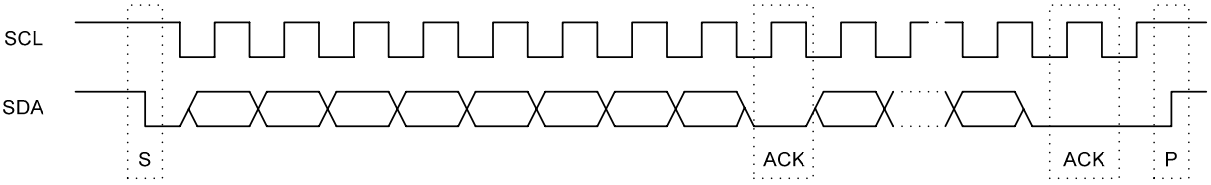


Figure1 I²C BUS Control Signal timing chart

I²C BUS register

1) The explanation of I²C Bus

I²C Bus (Inter IC Bus) is the bus system which the PHILIPS company developed.
It does controls such as the start, the stop by two control signals of SDA (Serial Data) and SCL (Serial Clock).
The output of each signal is open drain and forms out of wired OR.



S: Start condition
P: Stop condition
ACK: Acknowledge

Data is transmitted in the MSB first. 1 unit is composed of 8 bits and ACK is put back from the slave to confirm.
Slave IC reads data with rising edge of SCL. Master IC changes data by falling edge in SCL.

2) The control register

Table1 Slave Address

MSB							LSB
1	1	1	0	1	1	1	0

Note; LV1117N/NV are reception exclusive use. It depends and it uses LSB by the "0" fixation.

Table2 I²C Bus transmission

Function	Sub Address		Data							
	BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Input control/Gain control	0000 0001	01	0	0	Gain			Input		
Volume control	0000 0010	02	Channel		Volume					
Output/Surround/MODE control	0000 0011	03	L+R out gain			Surround			MODE	
Tone control [Bass]	0000 0100	04	0	0	0	Bass				
Tone control [TREBLE]	0000 0101	05	0	0	0	TREBLE				
Output port control	0000 0110	06	0	0	0	0	OUT3	OUT2	OUT1	OUT0

Table3 Input Selection

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	1	0	0	*	*	*	0	0	0
In A									0	0	*	*	*	0	0	1
In B									0	0	*	*	*	0	1	0
In C									0	0	*	*	*	0	1	1
In D									0	0	*	*	*	1	0	0

Table4 Gain control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
-6dB	0	0	0	0	0	0	0	1	0	0	0	1	1	*	*	*
-4dB									0	0	0	1	0	*	*	*
0dB									0	0	0	0	0	*	*	*
+4dB									0	0	1	1	0	*	*	*
+6dB									0	0	1	1	1	*	*	*

Table5 Mode control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Total	0	0	0	0	0	0	1	1	*	*	*	*	*	*	0	0
Matrix									*	*	*	*	*	*	0	1
Mono									*	*	*	*	*	*	1	0
Pseudo									*	*	*	*	*	*	1	1

Table6 Surround control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	0	0	0	1	1	*	*	*	0	0	0	*	*
MODE-C									*	*	*	0	1	1	*	*
MODE-B									*	*	*	0	1	0	*	*
MODE-A									*	*	*	0	0	1	*	*
MODE-F												1	1	1		
MODE-E												1	1	0		
MODE-D									*	*	*	1	0	1	*	*

Note; At the time of forced mono mode, there is not surround effect.
Note; Output gain = Step1 < Step7

Table7 L+R Output Gain control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MUTE	0	0	0	0	0	0	1	1	0	0	0	*	*	*	*	*
Step1									0	0	1	*	*	*	*	*
Step2									0	1	0	*	*	*	*	*
Step3									0	1	1	*	*	*	*	*
Step4									1	0	0	*	*	*	*	*
Step5									1	0	1	*	*	*	*	*
Step6									1	1	0	*	*	*	*	*
Step7									1	1	1	*	*	*	*	*

Note; Output gain = Step1 < Step7

Table8 Tone control [Bass control]

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
+20dB									0	0	0	0	1	0	1	0
+18dB									0	0	0	0	1	0	0	1
+16dB									0	0	0	0	1	0	0	0
+14dB									0	0	0	0	0	1	1	1
+12dB									0	0	0	0	0	1	1	0
+10dB									0	0	0	0	0	1	0	1
+8dB									0	0	0	0	0	1	0	0
+6dB									0	0	0	0	0	0	1	1
+4dB									0	0	0	0	0	0	1	0
+2dB									0	0	0	0	0	0	0	1
0dB	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
-2dB									0	0	0	1	0	0	0	1
-4dB									0	0	0	1	0	0	1	0
-6dB									0	0	0	1	0	0	1	1
-8dB									0	0	0	1	0	1	0	0
-10dB									0	0	0	1	0	1	0	1
-12dB									0	0	0	1	0	1	1	0
-14dB									0	0	0	1	0	1	1	1
-16dB									0	0	0	1	1	0	0	0
-18dB									0	0	0	1	1	0	0	1
-20dB									0	0	0	1	1	0	1	0

Table9 Tone control [TREBLE control]

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
+18dB									0	0	0	0	1	0	0	1
+16dB									0	0	0	0	1	0	0	0
+14dB									0	0	0	0	0	1	1	1
+12dB									0	0	0	0	0	1	1	0
+10dB									0	0	0	0	0	1	0	1
+8dB									0	0	0	0	0	1	0	0
+6dB									0	0	0	0	0	0	1	1
+4dB									0	0	0	0	0	0	1	0
+2dB									0	0	0	0	0	0	0	1
0dB	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
-2dB									0	0	0	1	0	0	0	1
-4dB									0	0	0	1	0	0	1	0
-6dB									0	0	0	1	0	0	1	1
-8dB									0	0	0	1	0	1	0	0
-10dB									0	0	0	1	0	1	0	1
-12dB									0	0	0	1	0	1	1	0
-14dB									0	0	0	1	0	1	1	1
-16dB									0	0	0	1	1	0	0	0
-18dB									0	0	0	1	1	0	0	1

Table10 Volume control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0dB									*	*	0	0	0	0	0	0
-1dB									*	*	0	0	0	0	0	1
-2dB									*	*	0	0	0	0	1	0
-3dB									*	*	0	0	0	0	1	1
-4dB									*	*	0	0	0	1	0	0
-5dB									*	*	0	0	0	1	0	1
-6dB									*	*	0	0	0	1	1	0
-7dB									*	*	0	0	0	1	1	1
-8dB									*	*	0	0	1	0	0	0
-9dB									*	*	0	0	1	0	0	1
-10dB									*	*	0	0	1	0	1	0
-11dB									*	*	0	0	1	0	1	1
-12dB									*	*	0	0	1	1	0	0
-13dB									*	*	0	0	1	1	0	1
-14dB									*	*	0	0	1	1	1	0
-16dB									*	*	0	0	1	1	1	1
-18dB									*	*	0	1	0	0	0	0
-20dB									*	*	0	1	0	0	0	1
-22dB									*	*	0	1	0	0	1	0
-24dB									*	*	0	1	0	0	1	1
-26dB									*	*	0	1	0	1	0	0
-28dB									*	*	0	1	0	1	0	1
-30dB									*	*	0	1	0	1	1	0
-32dB									*	*	0	1	0	1	1	1
-34dB	0	0	0	0	0	0	1	0	*	*	0	1	1	0	0	0
-36dB									*	*	0	1	1	0	0	1
-38dB									*	*	0	1	1	0	1	0
-40dB									*	*	0	1	1	0	1	1
-42dB									*	*	0	1	1	1	0	0
-44dB									*	*	0	1	1	1	0	1
-46dB									*	*	0	1	1	1	1	0
-48dB									*	*	0	1	1	1	1	1
-50dB									*	*	1	0	0	0	0	0
-52dB									*	*	1	0	0	0	0	1
-54dB									*	*	1	0	0	0	1	0
-56dB									*	*	1	0	0	0	1	1
-58dB									*	*	1	0	0	1	0	0
-60dB									*	*	1	0	0	1	0	1
-62dB									*	*	1	0	0	1	1	0
-64dB									*	*	1	0	0	1	1	1
-66dB									*	*	1	0	1	0	0	0
-68dB									*	*	1	0	1	0	0	1
-70dB									*	*	1	0	1	0	1	0
-72dB									*	*	1	0	1	0	1	1
-74dB									*	*	1	0	1	1	0	0
-76dB									*	*	1	0	1	1	0	1
-78dB									*	*	1	0	1	1	1	0
-80dB									*	*	1	0	1	1	1	1
-∞dB									*	*	1	1	0	0	0	0

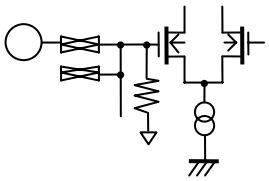
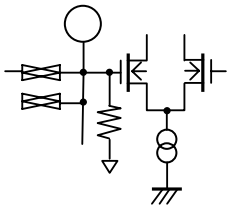
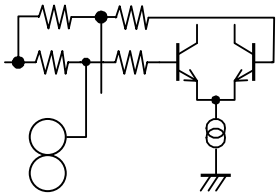
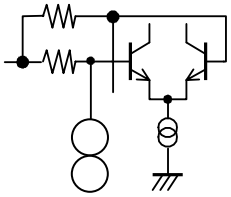
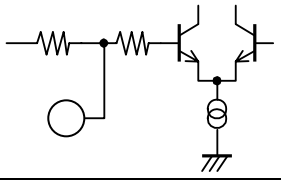
Table11 Volume channel control

	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
L-ch	0	0	0	0	0	0	1	0	0	1	*	*	*	*	*	*
R-ch									1	0	*	*	*	*	*	*
L/R									1	1	*	*	*	*	*	*

Table12 Output port control

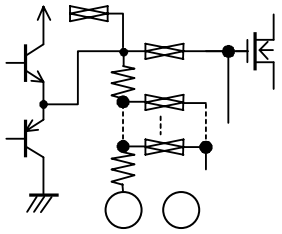
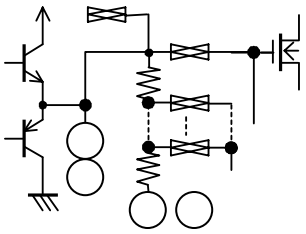
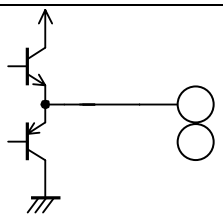
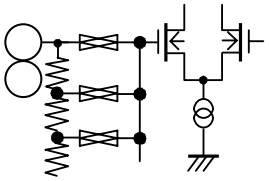
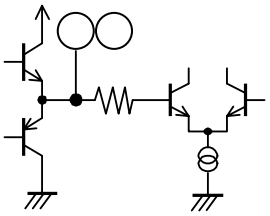
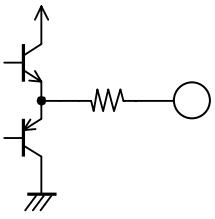
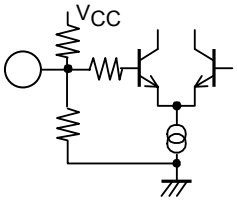
	Sub Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
On (sink)	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Off (open)									0	0	0	0	1	1	1	1

Pin Functions [LV1117N]

Pin No	Function	Voltage	Remarks	Internal equivalent circuit
1	GND	0		
2	INPUT-A(R)	VREF	Input Impedance ri=50kΩ	
41	INPUT-A(L)			
3	INPUT-B(R)			
40	INPUT-B(L)			
4	INPUT-C(R)			
39	INPUT-C(L)			
5	INPUT-D(R)			
38	INPUT-D(L)			
6	LINE-OUT(R)	VREF	Function SW Output ro=700Ω	
37	LINE-OUT(L)			
7	DC Cut(R)	VREF	DC offset cancellation capacitor connection pin	
36	DC Cut(L)			
8	ST-1	VREF	Pseudo stereo phase shift capacitor connection pin	
35	ST-2			
9	AViSS LPF	VREF	Capacitor connection pin for surround low pass filter	

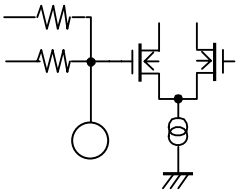
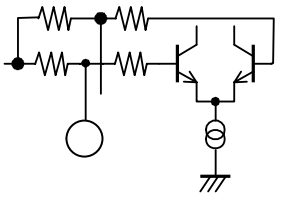
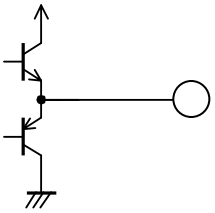
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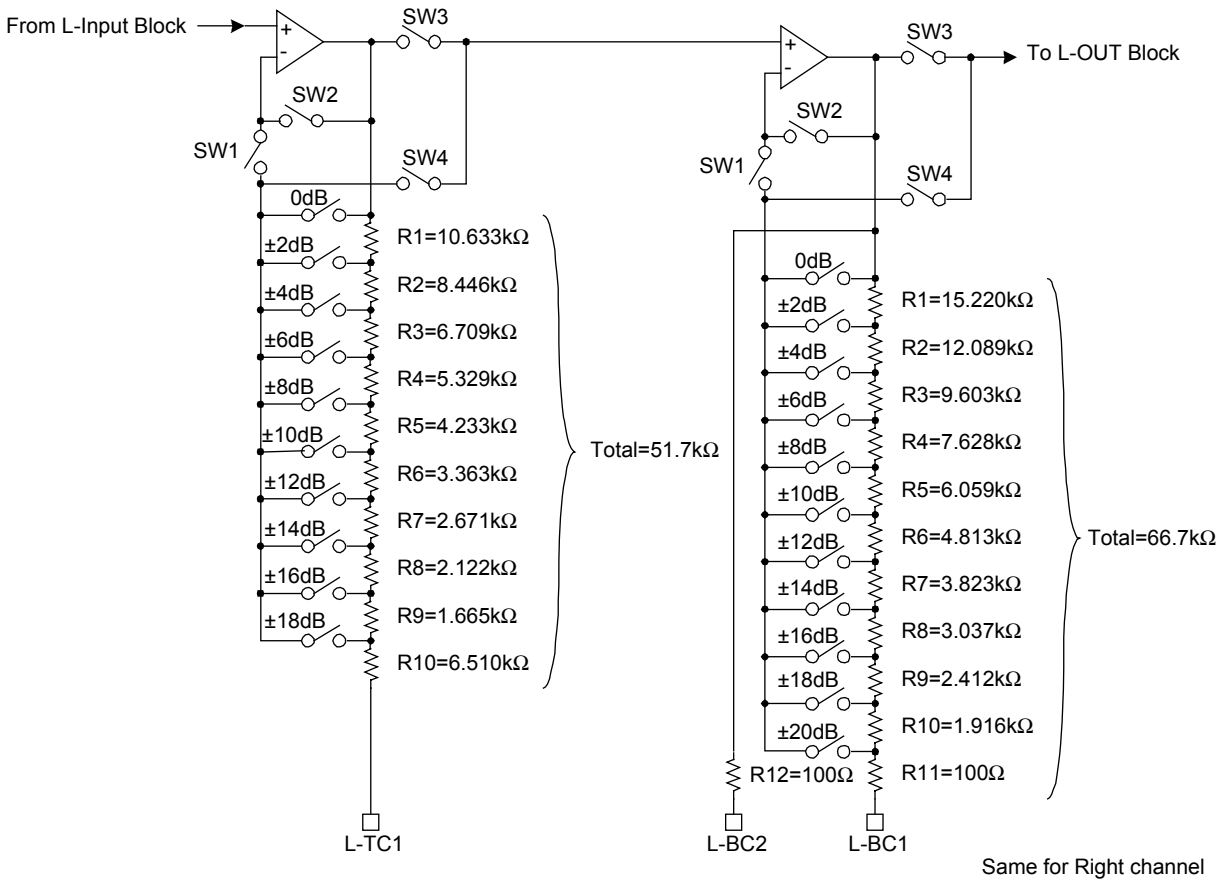
Pin No	Function	Voltage	Remarks	Internal equivalent circuit
10	TREBLE(R)	VREF	Capacitor connection pin for configuring treble filter	
33	TREBLE(L)			
11	BASS-1(R)	VREF	Bass band filter configuration capacitor and resistor connection pins	
32	BASS-1(L)			
12	BASS-2(R)			
31	BASS-2(L)			
13	OUT(R)	VREF	Output Impedance ro=100Ω	
30	OUT(L)			
14	EVR-IN(R)	VREF	Input Impedance ri=50kΩ	
29	EVR-IN(L)			
15	EVR-OUT(R)	VREF	Output Impedance ro=100Ω	
28	EVR-OUT(L)			
16	L+R OUT	VREF	Output Impedance ro=10kΩ	
17	VREF	$0.5V_{CC}$	Reference voltage	

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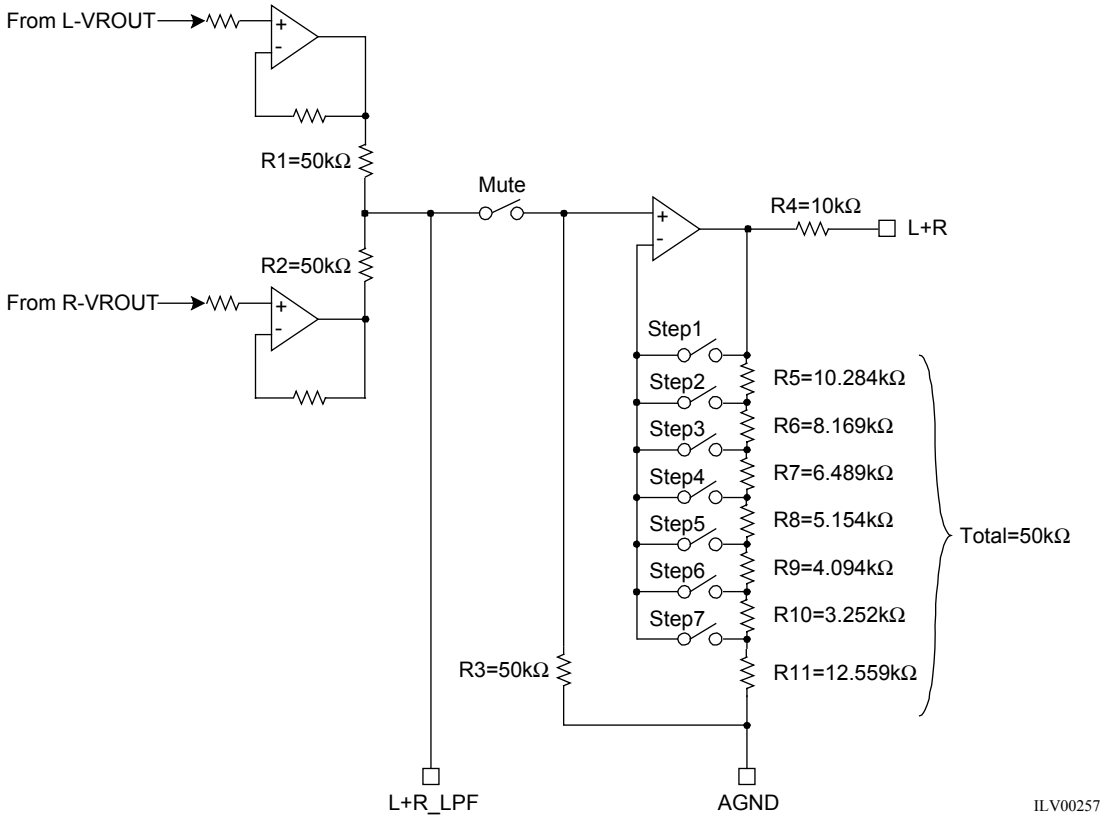
Pin No	Function	Voltage	Remarks	Internal equivalent circuit
18	V_{CC}	V_{CC}		
19	V_{DD}	V_{DD}		
20	Output 2		Nch open drain port output	
21	Output 3			
22	Output 1			
23	Output 0			
24	I^2C-DATA		I^2C control data input	
25	I^2C-CLK			
26	V_{SS}	0		
27	L+R LPF	VREF	Internal resistor	
34	AViSS HPF	VREF		
42	ANALOG GND	VREF		

Treble / Bass Band Block Equivalent Circuit Diagram



During boost, SW1 and SW3 are ON, during cut, SW2 and SW4 are ON, when 0dB, 0dBSW and SW2 and SW3 are ON.

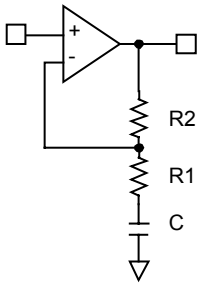
L+R Block Equivalent Circuit Diagram



Tone Circuit Constant Calculation Examples

Treble Band Circuit: The shelving characteristics can be obtained for the treble band.
The equivalent circuit and calculation formula during boost are indicated below.

• Calculation example 1



Specification Set frequency: f = 10000Hz
Gain during maximum boost: G_{+18dB} = 17.5dB
Let us use R1 = 6.51kΩ and R2 = 45.19kΩ
The above constants are inserted in the following formula

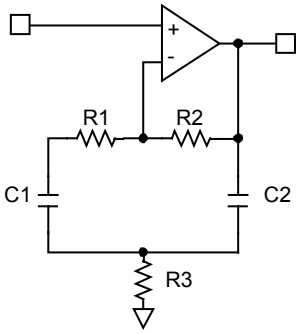
$$G = 20 \times \mathrm{Log}_{10}\left(1+\frac{R2}{\sqrt{R1^2+(1/\omega C)^2}}\right)$$

$$C = \frac{1}{2\pi f\sqrt{\left[\frac{R2}{10^{G/20}-1}\right]^2 - R1^2}}$$

$$= \frac{1}{2\pi 24000\sqrt{\left[\frac{45190}{7.50-1}\right]^2 - 6510^2}} \approx 2700\ (\mathrm{pF})$$

Bass Band Circuit: The equivalent circuit and the formula for calculating the external RC with a mean frequency of 100Hz are shown below.

• Base band equivalent circuit diagram



• Calculation example 1

specification Mean frequency: f0 = 100Hz
Gain during maximum boost: G_{+20dB} = 20dB
Let us use R1 = 0kΩ and R2 = 66.7kΩ, and C1 = C2 = C.

We obtain R2 from G = 20dB

$$G = 20 \times \mathrm{Log}_{10}\left(1+\frac{R2}{2R3}\right)$$

$$R3 = \frac{R2}{2\,(10^{G+20dB/20}-1)} = \frac{66700}{2\,(10-1)} \approx 3.6k\Omega$$

We obtain C from mean frequency f0 = 100Hz

$$f0 = \frac{1}{2\pi\sqrt{(R3R2C1C2)}}$$

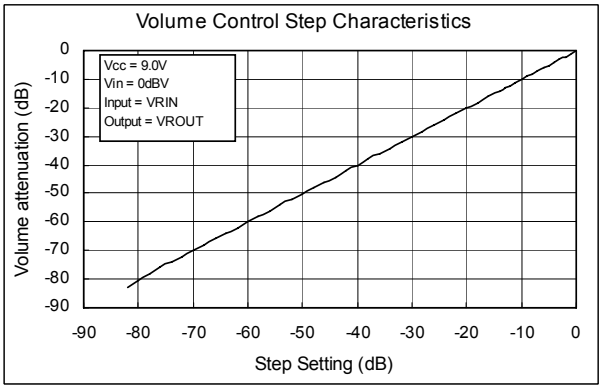
$$C = \frac{1}{2\pi f0\sqrt{R3R2}} = \frac{1}{2\pi \times 100\sqrt{66700 \times 3600}} \approx 0.1\mu F$$

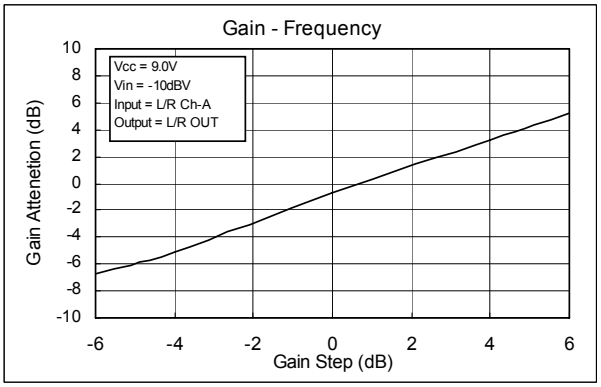
We obtain Q

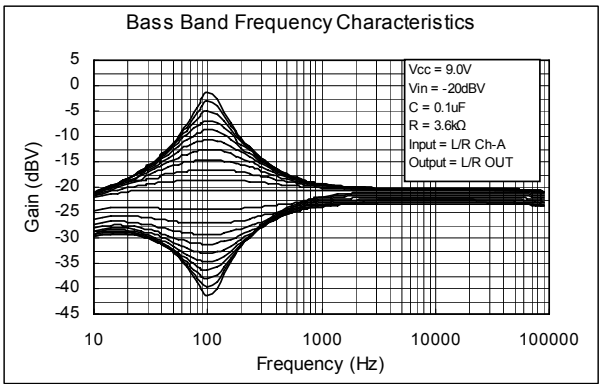
$$Q = \frac{R3R2}{2R3} \times \frac{1}{\sqrt{R3R2}} \approx 2.15$$

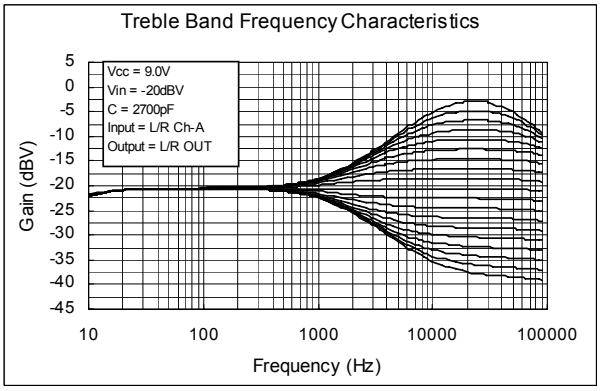
Note item when using

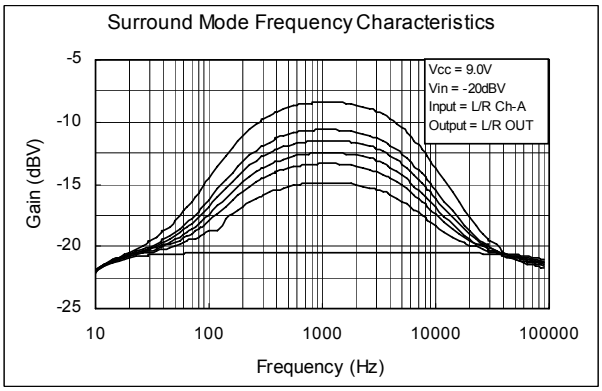
(1) When turning on the power, the setting inside is unsettled.
Before setting control data, it does a mute.
(2) To prevent the digital noise of the high frequency influence a terminal. (SCL, SDA)
It can be protected by a signal line in the ground pattern or by the shielding cable.
(3) To prevent the noise in changing a mode, please set the mute ON.

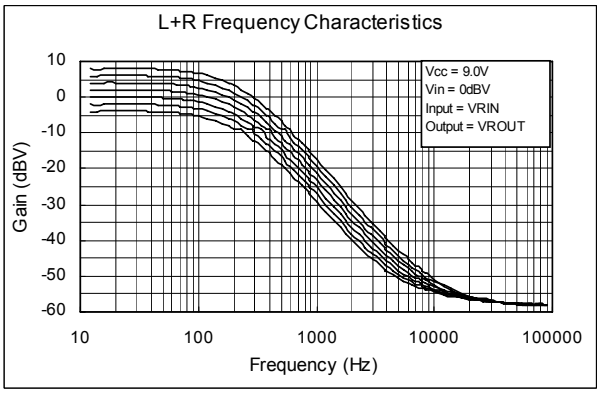

Volume Control Step Characteristics
Vcc = 9.0V
Vin = 0dBV
Input = VRIN
Output = VROUT
Volume attenuation (dB)
Step Setting (dB)

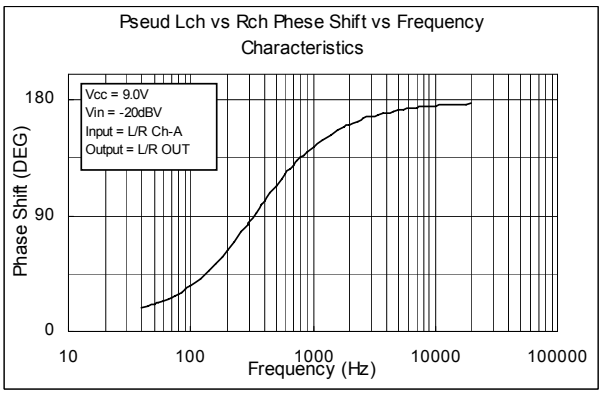

Gain - Frequency
Vcc = 9.0V
Vin = -10dBV
Input = L/R Ch-A
Output = L/R OUT
Gain Attenetion (dB)
Gain Step (dB)

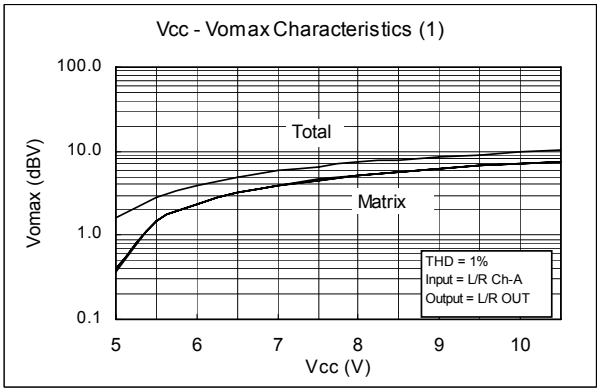

Bass Band Frequency Characteristics
Vcc = 9.0V
Vin = -20dBV
C = 0.1uF
R = 3.6kΩ
Input = L/R Ch-A
Output = L/R OUT
Gain (dBV)
Frequency (Hz)


Treble Band Frequency Characteristics
Vcc = 9.0V
Vin = -20dBV
C = 2700pF
Input = L/R Ch-A
Output = L/R OUT
Gain (dBV)
Frequency (Hz)

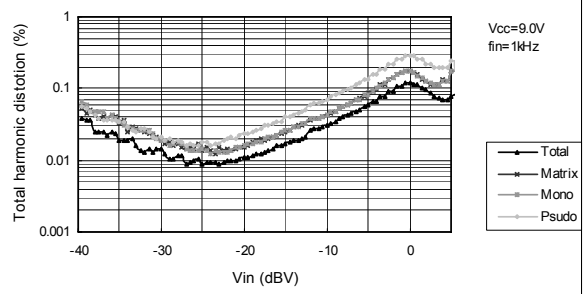

Surround Mode Frequency Characteristics
Vcc = 9.0V
Vin = -20dBV
Input = L/R Ch-A
Output = L/R OUT
Gain (dBV)
Frequency (Hz)


L+R Frequency Characteristics
Vcc = 9.0V
Vin = 0dBV
Input = VRIN
Output = VROUT
Gain (dBV)
Frequency (Hz)

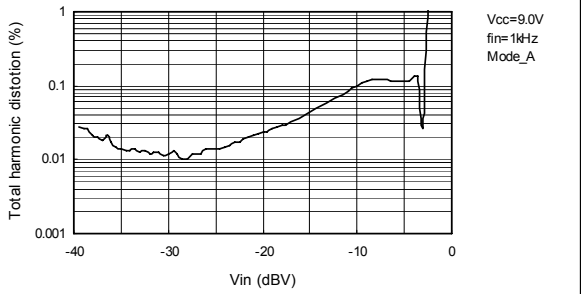

Pseud Lch vs Rch Phese Shift vs Frequency Characteristics
Vcc = 9.0V
Vin = -20dBV
Input = L/R Ch-A
Output = L/R OUT
Phase Shift (DEG)
Frequency (Hz)


Vcc - Vomax Characteristics (1)
Total
Matrix
THD = 1%
Input = L/R Ch-A
Output = L/R OUT
Vomax (dBV)
Vcc (V)

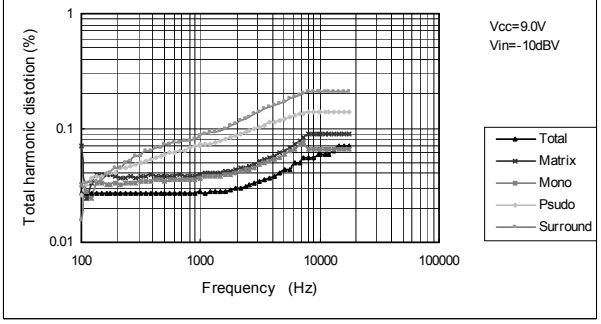
THD - Vin characteristics



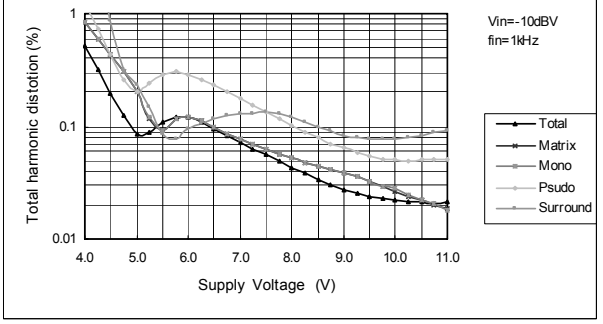
THD - Vin characteristics (Surround)



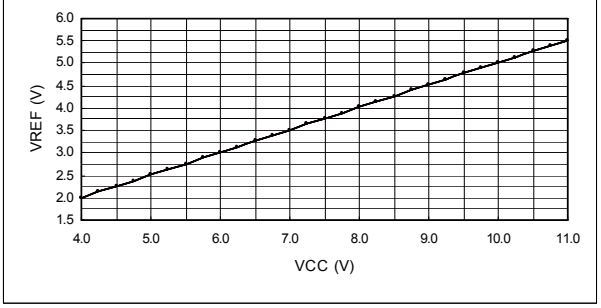
THD - Frequency Characteistics



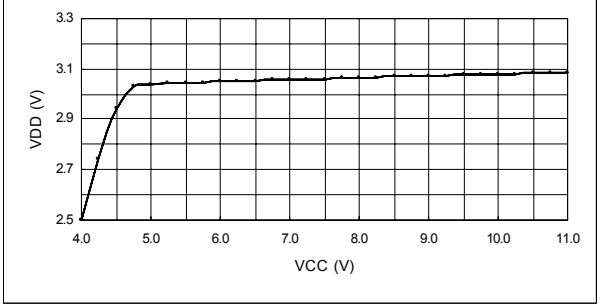
THD - Supply Voltage Characteristics



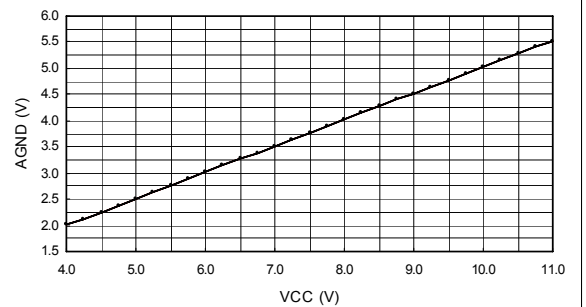
VCC - VREF



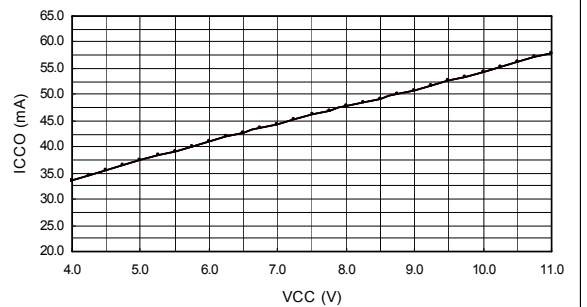
VCC - VDD



VCC - AGND



VCC - ICCO



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