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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR NP20P06SLG

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The NP20P06SLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

| PART NUMBER | LEAD PLATING | PACKING | PACKAGE |
|----------------------------------|---------------|------------------|-----------------|
| NP20P06SLG-E1-AY ^{Note} | Pure Sn (Tin) | Tape 2500 p/reel | TO-252 (MP-3ZK) |
| NP20P06SLG-E2-AY ^{Note} | | | |

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

- Super low on-state resistance
 $R_{DS(on)1} = 48 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$
 $R_{DS(on)2} = 64 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -10 \text{ A)}$
- Low input capacitance
 $C_{iss} = 1650 \text{ pF TYP.}$
- Built-in gate protection diode

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

| | | | |
|---|-----------------------|-------------|----|
| Drain to Source Voltage (V _{GS} = 0 V) | V _{DSS} | -60 | V |
| Gate to Source Voltage (V _{DS} = 0 V) | V _{GSS} | ±20 | V |
| Drain Current (DC) (T _C = 25°C) | I _{D(DC)} | ±20 | A |
| Drain Current (pulse) ^{Note1} | I _{D(pulse)} | ±60 | A |
| Total Power Dissipation (T _C = 25°C) | P _{T1} | 38 | W |
| Total Power Dissipation (T _A = 25°C) | P _{T2} | 1.2 | W |
| Channel Temperature | T _{ch} | 175 | °C |
| Storage Temperature | T _{stg} | -55 to +175 | °C |
| Single Avalanche Current ^{Note2} | I _{AS} | 17 | A |
| Single Avalanche Energy ^{Note2} | E _{AS} | 28 | mJ |

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω, V_{GS} = -20 → 0 V

THERMAL RESISTANCE

| | | | |
|---------------------------------------|-----------------------|-----|------|
| Channel to Case Thermal Resistance | R _{th(ch-C)} | 3.9 | °C/W |
| Channel to Ambient Thermal Resistance | R _{th(ch-A)} | 125 | °C/W |

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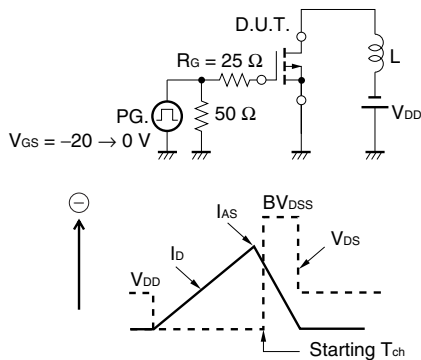
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

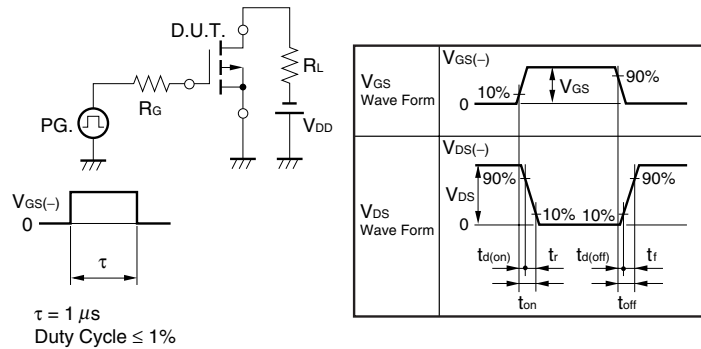
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|----------------------|--|------|------|------|------|
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = -60 V, V _{GS} = 0 V | | | -10 | μA |
| Gate Leakage Current | I _{GSS} | V _{GS} = ±20 V, V _{DS} = 0 V | | | ±10 | μA |
| Gate to Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = -250 μA | -1.0 | -1.6 | -2.5 | V |
| Forward Transfer Admittance ^{Note} | y _{fs} | V _{DS} = -10 V, I _D = -10 A | 7 | 14 | | S |
| Drain to Source On-state Resistance ^{Note} | R _{DS(on)1} | V _{GS} = -10 V, I _D = -10 A | | 36 | 48 | mΩ |
| | R _{DS(on)2} | V _{GS} = -4.5 V, I _D = -10 A | | 42 | 64 | mΩ |
| Input Capacitance | C _{iss} | V _{DS} = -10 V, | | 1650 | | pF |
| Output Capacitance | C _{oss} | V _{GS} = 0 V, | | 200 | | pF |
| Reverse Transfer Capacitance | C _{rss} | f = 1 MHz | | 130 | | pF |
| Turn-on Delay Time | t _{d(on)} | V _{DD} = -30 V, I _D = -10 A, | | 8 | | ns |
| Rise Time | t _r | V _{GS} = -10 V, | | 8 | | ns |
| Turn-off Delay Time | t _{d(off)} | R _G = 0 Ω | | 160 | | ns |
| Fall Time | t _f | | | 80 | | ns |
| Total Gate Charge | Q _G | V _{DD} = -48 V, | | 34 | | nC |
| Gate to Source Charge | Q _{GS} | V _{GS} = -10 V, | | 4 | | nC |
| Gate to Drain Charge | Q _{GD} | I _D = -20 A | | 9 | | nC |
| Body Diode Forward Voltage ^{Note} | V _{F(S-D)} | I _F = -20 A, V _{GS} = 0 V | | 0.95 | 1.5 | V |
| Reverse Recovery Time | t _{rr} | I _F = -20 A, V _{GS} = 0 V, | | 38 | | ns |
| Reverse Recovery Charge | Q _{rr} | di/dt = -100 A/μs | | 51 | | nC |

Note Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

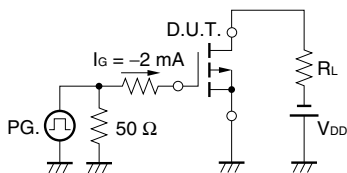
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

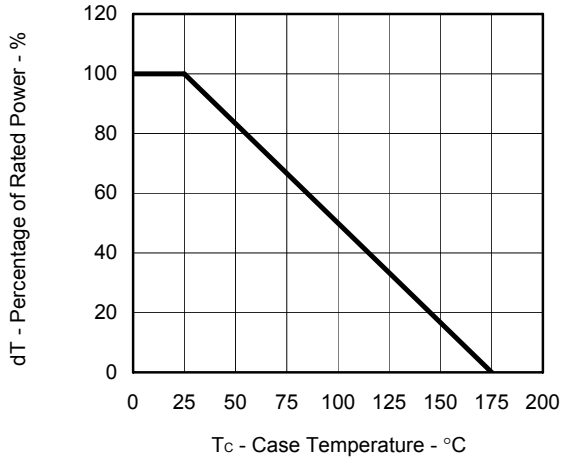


TEST CIRCUIT 3 GATE CHARGE

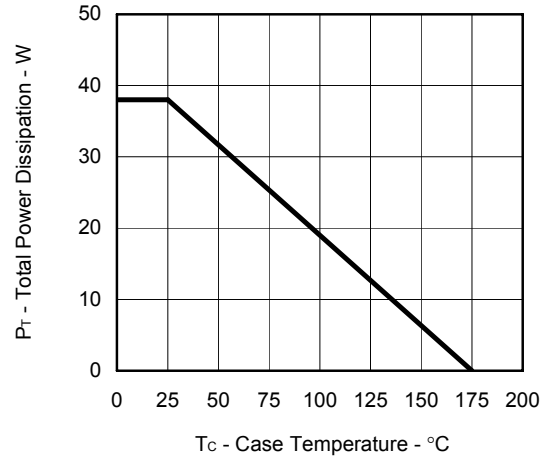


TYPICAL CHARACTERISTICS (T_A = 25°C)

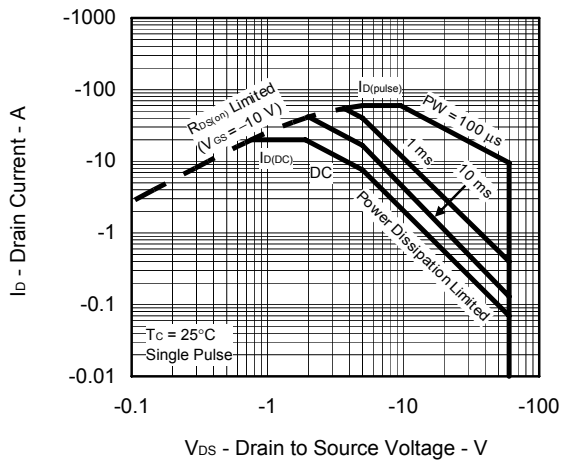
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



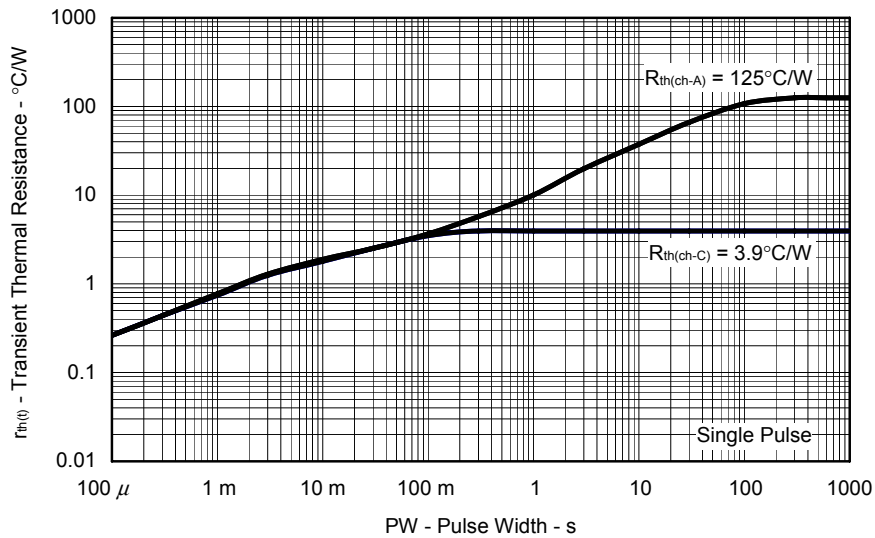
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



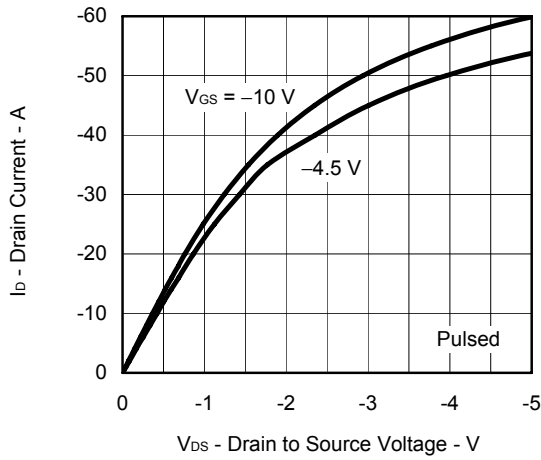
FORWARD BIAS SAFE OPERATING AREA



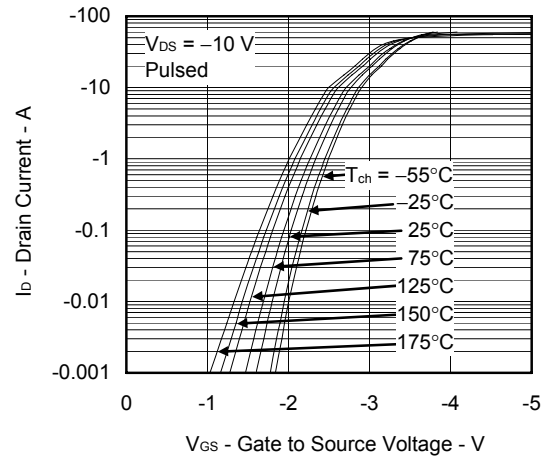
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



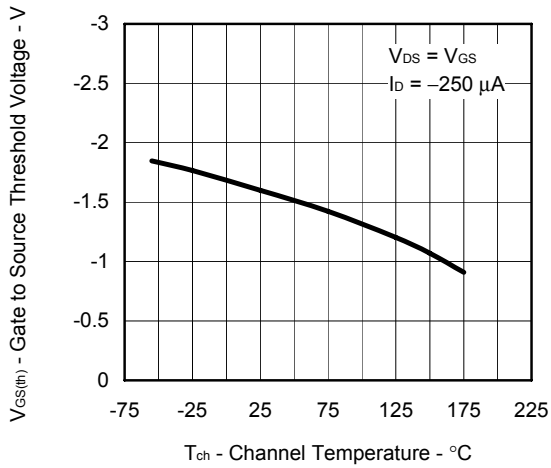
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



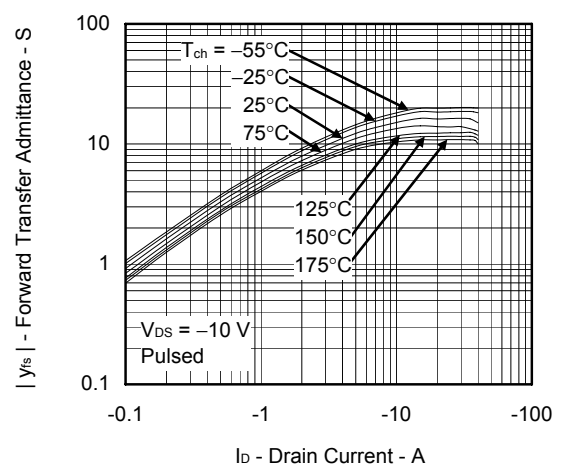
FORWARD TRANSFER CHARACTERISTICS



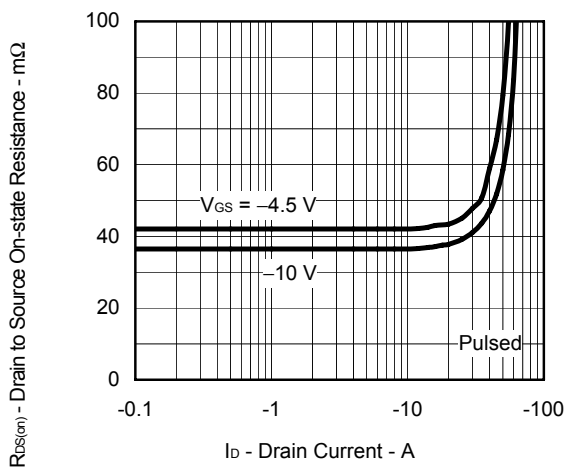
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



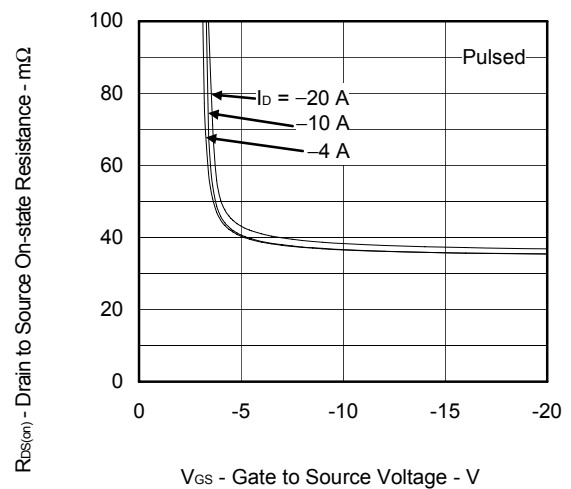
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



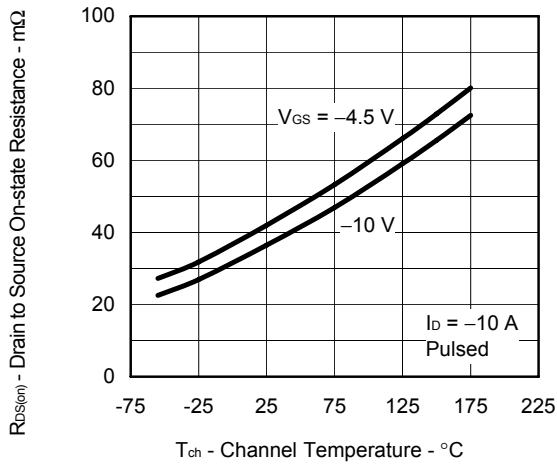
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



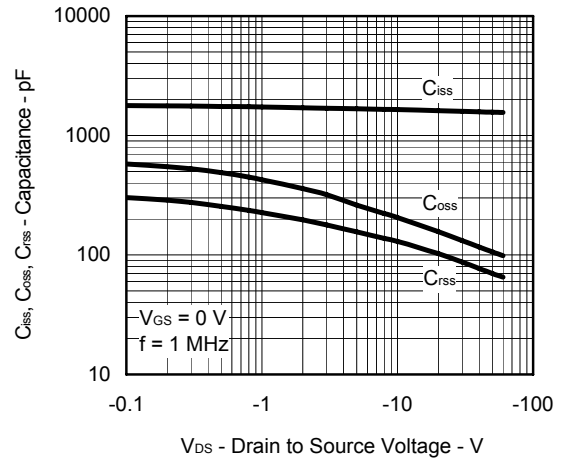
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



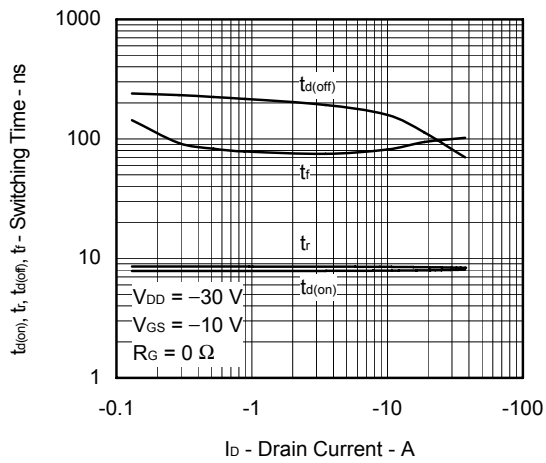
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



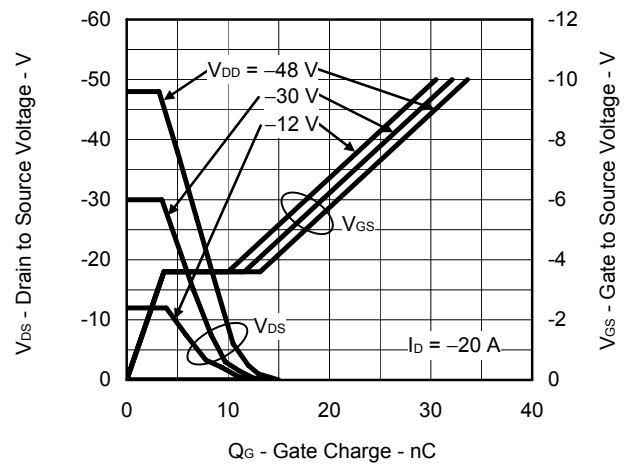
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



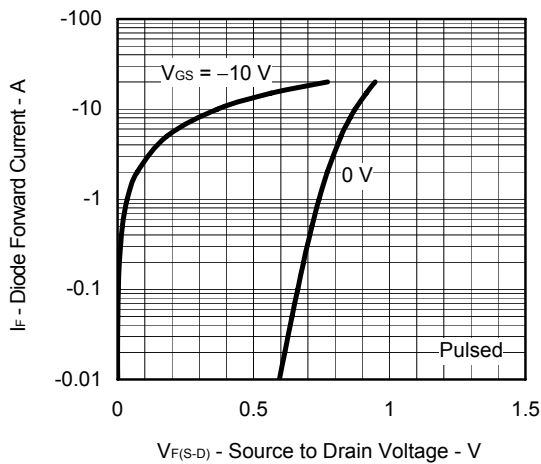
SWITCHING CHARACTERISTICS



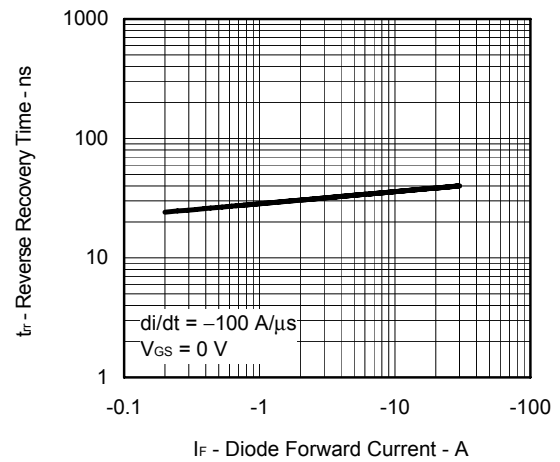
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

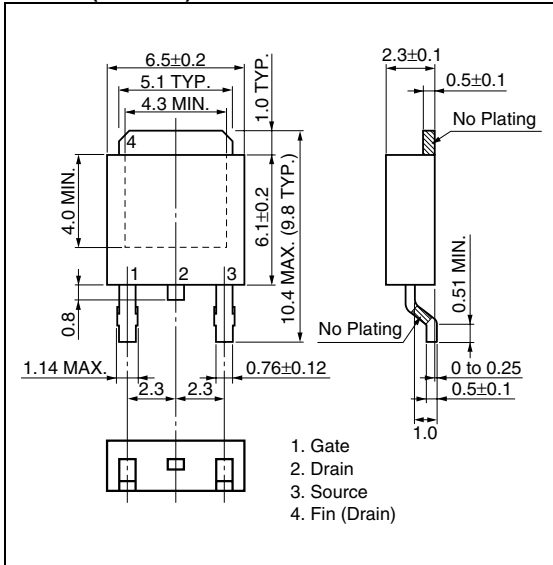


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

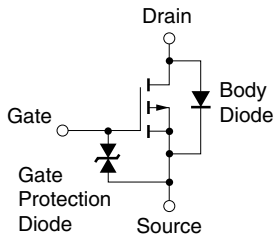


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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