Precision, Rail to Rail Input and Output, Quad Operational Amplifier

OP484

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/aerospace is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/OP484

2.0 Part Number. The complete part number(s) of this specification follow:

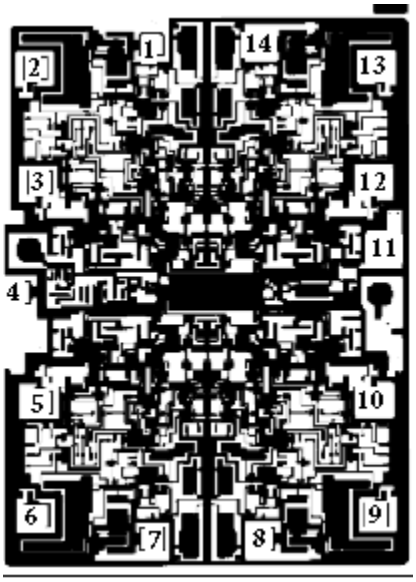
Part Number	Description
OP484-000C	Precision, Rail to Rail Input and Output, Quad Operational Amplifier
OP484R000C	Radiation Tested, Precision, Rail to Rail Input and Output, Quad Operational Amplifier

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
80 mil x 110 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1. OUTPUT A
2. –INPUT A
3. +INPUT A
4. +Vs
5. +INPUT B
6. –INPUT B
7. OUTPUT B
8. OUTPUT C
9. –INPUT C
10. +INPUT C
11. –Vs
12. +INPUT D
13. –INPUT D
14. OUTPUT D

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3.3 Absolute Maximum Ratings 1/

Supply Voltage	±18V
Differential Input Voltage	±0.6V
Input Voltage	±18V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Junction Temperature (T_J)	+150°C

Absolute Maximum Ratings Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Sample Size and Qual Acceptance Criteria – 10/0
(b) Qual Sample Package – DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
V_S = +5V, V_{CM} = 2.5V					
Input Offset Voltage	V_{OS}			200	µV
Input Offset Current	I_{OS}	2/		50	nA
Input Bias Current	I_B	2/		350	nA
Input Voltage Range	IVR		1	4	V
Common Mode Rejection Ratio	CMRR	V_{CM} = IVR	86		dB
Output High Voltage	V_{OH}	I_L = 1mA	4.85		V
Output Low Voltage	V_{OL}	I_L = 1mA		125	mV
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_{OUT} = 1V to 4V	50		V/mV
Supply Current 3/	I_{SY}	V_{OUT} = 2.5V		5.8	mA
V_S = ±15V, V_{CM} = 0V					
Input Offset Voltage	V_{OS}			150	µV
Input Offset Current	I_{OS}			50	nA
Input Bias Current	I_B			350	nA

Table I - Dice Electrical Characteristics (Continued)					
Parameter	**Symbol**	**Conditions 1/**	**Limit Min**	**Limit Max**	**Units**
$V_S = \pm 15V$, $V_{CM} = 0V$					
Input Voltage Range	IVR		-15	+15	
Common Mode Rejection Ratio	CMRR	V_{CM} = IVR	80		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2V$ to $\pm 18V$	90		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	150		V/mV
Supply Current 2/	I_{SY}	$V_{OUT} = 0V$		8	mA

Table I Notes:

1/ T_A = 25°C, unless otherwise specified.
2/ Guaranteed by $V_S = \pm 15V$ test.
3/ I_{SY} limit = total all four amplifiers.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
V_S = +5V, V_{CM} = 2.5V						
Input Offset Voltage	V_{OS}		1		200	µV
			2, 3		400	
		M, D, L, R_3/	1		600	
Input Offset Current	I_{OS}	1/	1, 2, 3		50	nA
		M, D, L, R_3/	1		400	
Input Bias Current	I_B	1/	1		350	
			2, 3		575	
		M, D, L, R_3/	1		3000	
Common Mode Rejection Ratio 4/	CMRR	V_{CM} = 1V to 4V	1, 2, 3	86		dB
Output High Voltage 4/	V_{OH}	I_L = 1mA	4	4.85		V
Output Low Voltage 4/	V_{OL}	I_L = 1mA	4		125	mV
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_{OUT} = 1V to 4V	4	50		V/mV
			5, 6	25		
		$R_L \geq 10k\Omega$, V_{OUT} = 1V to 4V, M, D, L, R_3/	4	25		
Supply Current 2/	I_{SY}	V_{OUT} = 2.5V	1		5.8	mA
		M, D, L, R_3/	1		5.85	
V_S = ±15V, V_{CM} = 0V						
Input Offset Voltage 4/	V_{OS}		1		250	µV
			2, 3		500	
Average Input Offset Voltage Drift 4/	TCV_{OS}		8		2	µV/°C
Input Offset Current 4/	I_{OS}		1, 2, 3		50	nA
Input Bias Current 4/	I_B		1		350	nA
			2, 3		575	
Common Mode Rejection Ratio 4/	CMRR	V_{CM} = -15V to +15V	1, 2, 3	80		dB
Power Supply Rejection Ratio 4/	PSRR	V_S = ±2V to ±18V	1, 2, 3	90		dB
Large Signal Voltage Gain 4/	A_{VO}	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	4	150		V/mV
			5, 6	75		
Supply Current 2/ 4/	I_{SY}	V_{OUT} = 0V	1		8	mA
		V_S = ±18V, V_{OUT} = 0V	1, 2, 3		9	

Table II Notes:

1/ Guaranteed by V_S = ±15V test.
2/ limit = total all four amplifiers.
3/ I_{SY} Devices tested at 100Krad irradiation.
4/ Parameter not tested post irradiation.

Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table II with the following exceptions)								
Parameter	**Symbol**	**Sub-groups**	**Burn In Limit Min**	**Burn In Limit Max**	**Life Test Limit Min**	**Life Test Limit Max**	**Life Test Delta**	**Units**
Input Offset Voltage $V_S = \pm 15V$	V_{OS}	1		500		750	±250	µV
		2, 3				1000		
Input Bias Current $V_S = \pm 15V$	I_B	1		450		550	±100	nA
		2, 3				775		
Input Offset Current $V_S = \pm 15V$	I_{OS}	1		60		100	±40	nA
		2, 3				100		
Input Offset Voltage $V_S = +5V$	V_{OS}	1		300		450		µV
		2, 3				650		

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	4-Nov-111
B	Update web address	Jan. 25, 2002
C	Add radiation part number. Update web address	Feb. 10, 2003
D	Update header/footer and add to 1.0 scope description.	March 5, 2008
E	Add Junction Temperature (T_J)....+150°C to 3.3-Absolute Max Ratings section & aligned/centered Table II	April 3, 2008
F	Updated Section 4.0c note to indicated pre-screen temp testing being performed.	June 5 2009
G	Updated fonts and size to ADI standards. Touched up die picture for clarity.	Oct 3, 2011

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