FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20210-2E

Semicustom

CMOS

Standard Cell

CS101 Series

■ DESCRIPTION

CS101 series, a 90 nm standard cell product, is a CMOS ASIC that satisfies user's demands for lower power consumption and higher speed. The leakage current of the transistors is the minimum level in the industry. Three types of core transistors with a different threshold voltage can be mixed according to user application.

The design rules match industry standards, and a wide range of IP macros are available for use.

As well as providing a maximum of 100 million gates, approximately twice the level of integration achieved in previous products, the power consumption per gate is also reduced by about half to 2.7 nW. Also, using the high-speed library increases the speed by a factor of approximately 1.3, with a gate delay time of 12 ps.

■ FEATURES

- Technology : 90 nm Si gate CMOS
  7- to 10-metal layers.
  Low-K (low permittivity) material is used for all dielectric inter-layers.
  Three different types of core transistors (low leak, standard, and high speed) can be used on the same chip.
  The design rules comply with industry standard processes.
- Power supply voltage : +1.2 V ± 0.1 V (standard)
- Operation junction temperature : – 40 °C to + 125 °C (standard)
- Gate delay time : tpd = 12 ps (1.2 V, Inverter, F/O = 1)
- Gate power consumption : Pd = 2.7 nW/MHz/BC (1.2 V, 2 NAND, F/O = 1)
- High level of integration : Up to 91 million gates
- Reduced chip sized realized by I/O with pad.
- Support for a wide range of cell sets (from low power versions to ultra high speed versions).
- Compliance with industry standard design rules enables non-Fujitsu commercial macros to be easily incorporated.
- Compiled cell (RAM, ROM, others)
- Support for ultra high speed (up to 10 Gbps) interface macros.
- Special interfaces (LVDS, SSTL2, etc.)
- Supports use of industry standard libraries (.LIB).
- Uses industry standard tools and supports the optimum tools for the application.

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- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support for Signal Integrity, EMI noise reduction
- Support for static timing sign-off
- Optimum package range : FBGA, FC-BGA, PBGA,TEBGA

■ MACRO LIBRARIES (including those in preparation)

1. Logic cells (about 400 types)

Library sets having three different types of core transistors with a different threshold value are provided.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock Buffer
- Decoder
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip Flop
- Selector
- Others

2. IP macros

Compliance with the design rules recommended by the industry standard STARC (Semiconductor Technology Academic Research Center) recommendations which means a wide range of commercially available IP macros can be used.

Fujitsu plans to offer the following macros.

CPU/DSP	ARM9 DSPs for communications, AV, and similar applications, others
Multi-media processing macro	JPEG, MPEG, others
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	RAM (1-port, 2-port), ROM, product sum calculator, others
PLL	Analog PLL

3. Special I/O interface macro

Interface macro	LVDS, SSTL2, HSTL, GTL, others
Fast I/F macro	6 Gbps I/F, 10 Gbps I/F, others

■ COMPILED CELL

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS101 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	16 to 144 K	16 to 1 K	1 to 144
8	32 to 576 K	32 to 8 K	1 to 72
16	64 to 576 K	64 to 16 K	1 to 36

2. Clock synchronous dual port RAM (2 address : 2 read/write)

Column type (bit)	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	16 to 144 K	8 to 1 K	2 to 144
16	64 to 144 K	32 to 4 K	2 to 36

3. Clock synchronous ROM

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	256 to 4 M	128 to 16 K	2 to 256
64	1 K to 4 M	512 to 64 K	2 to 64

4. Clock synchronous register file (2 address : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	8 to 18 K	4 to 128	2 to 144

5. Clock synchronous register file (4 address : 2 read, 2 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	8 to 18 K	4 to 128	2 to 144

■ LARGE CAPACITY MEMORY

Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	64 K to 9 M	8 K to 64 K	8 to 144

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Application	Rating		Unit
			Min	Max	
Power supply voltage	VDD	VDDI (Internal)	− 0.5	+ 1.8	V
		VDDE (External 2.5 V)	− 0.5	+ 3.6	V
		VDDE (External 3.3 V)	− 0.5	+ 4.6	V
Input voltage *1	VI	1.2 V	− 0.5	VDDI + 0.5 (≤ 1.8)	V
		2.5 V	− 0.5	VDDE + 0.5 (≤ 3.6)	V
		3.3 V	− 0.5	VDDE + 0.5 (≤ 4.6)	V
Output voltage	VO	1.2 V	− 0.5	VDDI + 0.5 (≤ 1.8)	V
		2.5 V	− 0.5	VDDE + 0.5 (≤ 3.6)	V
		3.3 V	− 0.5	VDDE + 0.5 (≤ 4.6)	V
Storage temperature	Tstg	Plastic package	− 55	+ 125	°C
Operation junction temperature	Tj	—	− 40	+ 125	°C
Power supply pin current *2	ID	per VDD, VDDI, VDDE VSS pin	—	*4	mA
Output current *3	IO	—	—	*4	mA

*1 : The values vary depending on the type of macros.

*2 : Maximum power supply current that can steadily flow.

*3 : Maximum output current that can steadily flow.

*4 : Contact your Fujitsu representative for details.

Note : VSS = 0 V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• **Single power supply (VDD = 1.2 V ± 0.1 V)**

(VSS = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	VDD	1.1	1.2	1.3	V
H level input voltage	VIH	VDD × 0.7	—	VDD + 0.3	V
L level input voltage	VIL	− 0.3	—	VDD × 0.3	V
Operation junction temperature	Tj	− 40	—	+ 125	°C

• **Dual power supply (VDDE = 2.5 V ± 0.2 V, VDDI = 1.2 V ± 0.1 V)**

(VSS = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	2.5 V	VDDE	2.3	2.5	2.7	V
	1.2 V	VDDI	1.1	1.2	1.3	V
H level input voltage	2.5 V CMOS level	VIH	1.7	—	VDDE + 0.3	V
	1.2 V CMOS level		VDDI × 0.7	—	VDDI + 0.3	V
L level input voltage	2.5 V CMOS level	VIL	− 0.3	—	+ 0.7	V
	1.2 V CMOS level		− 0.3	—	VDDI × 0.3	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

• **Dual power supply (VDDE = 3.3 V ± 0.3 V, VDDI = 1.2 V ± 0.1 V)**

(VSS = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	3.3 V	VDDE	3.0	3.3	3.6	V
	1.2 V	VDDI	1.1	1.2	1.3	V
H level input voltage	3.3 V CMOS level	VIH	2.0	—	VDDE + 0.3	V
	1.2 V CMOS level		VDDI × 0.7	—	VDDI + 0.3	V
L level input voltage	3.3 V CMOS level	VIL	− 0.3	—	+ 0.8	V
	1.2 V CMOS level		− 0.3	—	VDDI × 0.3	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• **Single power supply : VDD = 1.2 V**

(VDD = 1.2 V ± 0.1 V, VSS = 0 V, Tj = – 40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	VOH	IOH = – 100 µA	VDD – 0.1	—	VDD	V
L level output voltage	VOL	IOL = 100 µA	0	—	0.1	V
Input leakage current	IL	—	—	—	—	µA
Pull-up/Pull-down resistor	RP	VIL = 0 at pull-up VIH = VDD at pull-down	—	12 (Target value)	—	kΩ

• **Dual power supply : VDDE = 2.5 V, VDDI = 1.2 V**

(VDDE = 2.5 V ± 0.2 V, VDDI = 1.2 V ± 0.1 V, VSS = 0 V, Tj = – 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	VOH3	2.5 V output, IOH = – 100 µA	VDDE – 0.2	—	VDDE	V
	VOH2	1.2 V output, IOH = – 100 µA	VDDI – 0.1	—	VDDI	V
L level output voltage	VOL3	2.5 V output, IOL = 100 µA	0	—	0.2	V
	VOL2	1.2 V output, IOL = 100 µA	0	—	0.1	V
Input leakage current	IL	—	—	—	—	µA
pull-up/Pull-down resistor	RP	2.5 V, VIL = 0 at pull-up/ VIH = VDDE at pull-down	—	25	—	kΩ
		1.2 V, VIL = 0 at pull-up/ VIH = VDDI at pull-down	—	12	—	kΩ

• **Dual power supply : VDDE = 3.3 V, VDDI = 1.2 V**

(VDDE = 3.3 V ± 0.3 V, VDDI = 1.2 V ± 0.1 V, VSS = 0 V, Tj = – 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	VOH3	3.3 V, IOH = – 100 µA	VDDE – 0.2	—	VDDE	V
	VOH2	1.2 V, IOH = – 100 µA	VDDI – 0.1	—	VDDI	V
L level output voltage	VOL3	3.3 V, IOL = 100 µA	0	—	0.2	V
	VOL2	1.2 V, IOL = 100 µA	0	—	0.1	V
Input leakage current*	IL	—	—	—	± 4	µA
pull-up/Pull-down resistor	RP	3.3 V, VIL = 0 at pull-up/ VIH = VDDE at pull-down	15	33	70	kΩ
		1.2 V, VIL = 0 at pull-up/ VIH = VDDE at pull-down	—	12	—	kΩ

* : The input leakage current may exceed the above value when an input buffer with pull-up or pull-down resistor is used.

■ AC Characteristics (with low power consumption, high density CS101SL library used)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	tpd *1	typ *2 × tmin *3	typ *2 × ttyp *3	typ *2 × tmax *3	ns

*1 : Delay time = propagation delay time, enable time, disable time

*2 : “typ” is calculated based on the cell specifications.

*3 : Measurement condition

Measurement condition	tmin	ttyp	tmax
VDD = 1.2 V ± 0.1 V, VSS = 0 V, Tj = – 40 °C to +125 °C	0.62	1.00	1.57

■ I/O Pin Capacitance

Parameter	Symbol	Value	Unit
Input pin	CIN	Max16	pF
Output pin	COUT	Max16	pF
I/O pin	CI/O	Max16	pF

Note : The capacitance values vary depending on the package and pin positions.

■ DESIGN METHODS

Fujitsu’s Reference Design Flow provides the following functions that help shorten the development time of large scale and high quality LSIs.

- High reliability design estimation in the early stage of physical design realized by physical prototyping.
- Layout synthesis with optimized timing realized by physical synthesis tools.
- High accuracy design environment considering drop in power supply voltage, signal noise, delay penalty, and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.

■ PACKAGES

Packages available for existing series can be used for CS101 series. This allows smooth replacement with previously developed products.

Please contact your Fujitsu agent for details of delivery times.

FBGA package : Max 424 pins

FC-BGA package : Max 2116 pins

PBGA package : Max 420 pins

TEBGA package : Max 900 pins

(Packages under planning are included.)

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