National Semiconductor

December 1994

LM6125/LM6225/LM6325 High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at 800 V/µs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

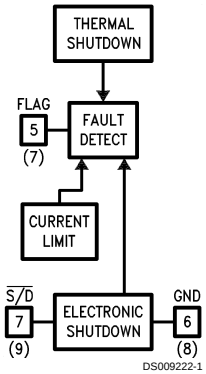
Features

- High slew rate: 800 V/µs
- High output current: ±300 mA
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

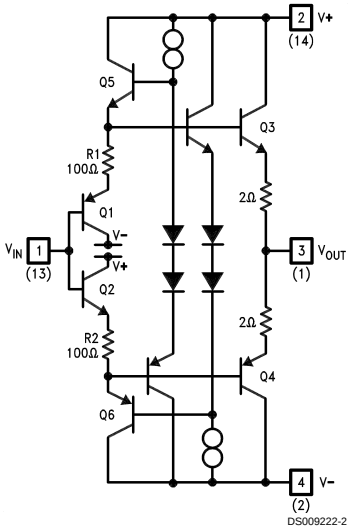
Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic and Block Diagram



DS009222-1



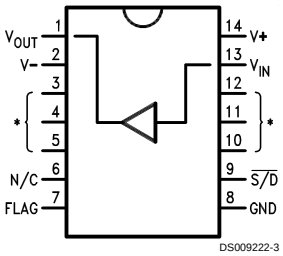
DS009222-2

Numbers in () are for 14–pin N DIP.

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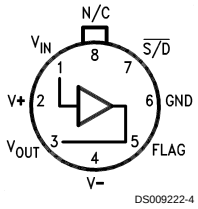
Pin Configurations



DS009222-3

*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N
or LM6325N
See NS Package Number N14A



DS009222-4

Note: Pin 4 connected to case

Top View
Order Number LM6125H/883 (Note 1)
or LM6125H
See NS Package Number H08C

Note 1: Available per 5962-9081501

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36V (±18V)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Flag Output Voltage	GND ≤ Vflag ≤ +Vsupply
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 seconds)	260˚C
ESD Tolerance (Note 9)	±1500V
θ_{JA} (Note 4)	
H Package	150˚C/W
N Package	40˚C/W
Maximum Junction Temperature (T_J)	150˚C
Operating Temperature Range	
LM6125	−55˚C to +125˚C
LM6225	−40˚C to +85˚C
LM6325	0˚C to +70˚C
Operating Supply Voltage Range	4.75V to ±16V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25˚C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	R_L = 1kΩ, V_{IN} = ±10V	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	V/V Min
A_{V3}	Voltage Gain 3 (Note 6)	R_L = 50Ω, V+ = 5V V_{IN} = 2 V_{PP} **(1.5 V_{PP})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	4 **7**	4 **7**	5 **7**	µA Max
R_{IN}	Input Resistance	R_L = 50Ω	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	R_L = ∞	15	18 **20**	18 **20**	20 **22**	
I_{S2}	Supply Current 2	R_L = ∞, V+ = 5V	14	16 **18**	16 **18**	18 **20**	mA Max
$I_{S/D}$	Supply Current in Shutdown	R_L = ∞, V± = ±15V	1.1	1.5 **2.0**	1.5 **2.0**	1.5 **2.0**	
V_{O1}	Output Swing 1	R_L = 1 kΩ	13.5	13.3 **13**	13.3 **13**	13.2 **13**	
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5 **10**	11.5 **10**	11 **10**	±V Min
V_{O3}	Output Swing 3	R_L = 50Ω	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	R_L = 50Ω	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSRR	Power Supply Rejection Ratio	V+ = 5V (Note 6)	70	60 **55**	60 **50**	60 **50**	dB Min
V_{OL}	Flag Pin Output Low Voltage	V± = ±5V to ±15V $V_{S/D}$ = 0V		300 **400**	300 **400**	340 **400**	mV Max

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typ	LM6125	LM6225	LM6325	Units
				Limit (Notes 5, 10)	**Limit** (Note 5)	**Limit** (Note 5)	
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 6)	0.01	10 **20**	10 **20**	10 **20**	µA Max
V_{TH}	Shutdown Threshold		1.4				V
V_{IH}	Shutdown Pin Trip Point High			2.0 **2.0**	2.0 **2.0**	2.0 **2.0**	V Min
V_{IL}	Shutdown Pin Trip Point Low			0.8 **0.8**	0.8 **0.8**	0.8 **0.8**	V Max
I_{IL}	Shutdown Pin Input Low Current	$V_{S/D}$ = 0V	−0.07	−10 **−20**	−10 **−20**	−10 **−20**	µA Max
I_{IH}	Shutdown Pin Input High Current	$V_{S/D}$ = 5V	−0.05	−10 **−20**	−10 **−20**	−10 **−20**	µA Max
I_O	Bi-State Output Current	Shutdown Pin = 0V V_{OUT} = +5V or −5V	1	50 **2000**	50 **100**	100 **200**	µA

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typ	LM6125	LM6225	LM6325	Units
				Limit (Note 5)	**Limit** (Note 5)	**Limit** (Note 5)	
SR_1	Slew Rate 1	V_{IN} = ±11V, R_L = 1 kΩ	1200				V/µs Min
SR_2	Slew Rate 2	V_{IN} = ±11V, R_L = 50Ω (Note 8)	800	550	550	550	
SR_3	Slew Rate 3	V_{IN} = 2 V_{PP}, R_L = 50Ω V+ = 5V (Note 6)	50				
BW	−3 dB Bandwidth	V_{IN} = 100 mV_{PP} R_L = 50Ω, $C_L \leq$ 10 pF	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	8.0				ns
t_{PD}	Propagation Delay Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	4.0				ns
O_S	Overshoot	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	10				%
V_{FT}	V_{IN}, V_{OUT} Feedthrough in Shutdown	Shutdown Pin = 0V V_{IN} = 4 V_{PP}, 1 MHz R_L = 50Ω	−50				dB
C_{OUT}	Output Capacitance in Shutdown	Shutdown Pin = 0V	30				pF
t_{SD}	Shutdown Response Time		700				ns

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 3: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. See Overvoltage Protection in Application Hints.

Note 4: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

AC Electrical Characteristics (Continued)

Note 5: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17˚C/W. The thermal impedance θ_{JA} of the device in the N package is 40˚C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60˚C/W.

Note 6: Limits are guaranteed by testing or correlation.

Note 7: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at −55˚C where it is reduced to 1.5 V_{PP}.

Note 8: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

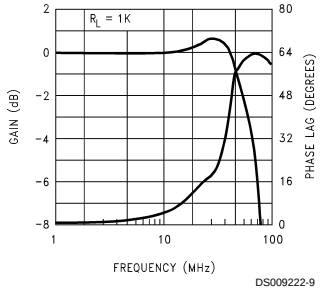
Note 9: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25˚C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/µs.

Note 10: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

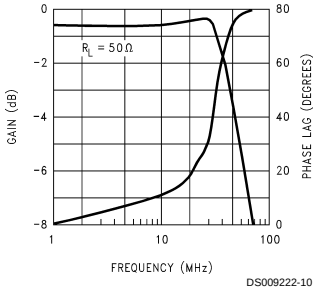
Note 11: A military RETS specification is available on request. At the time of printing, the LM6125H/883 RETS spec complied with the Boldface limits in this column. The LM6125H/883 may also be procured as Standard Military Drawing specification #5962-9081501MXX.

Typical Performance Characteristics T_A = 25˚C, V_S= ± 15V unless otherwise specified

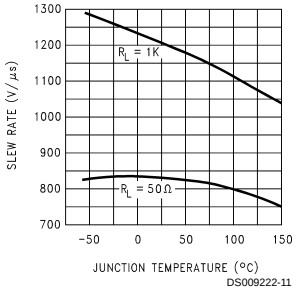
Frequency Response



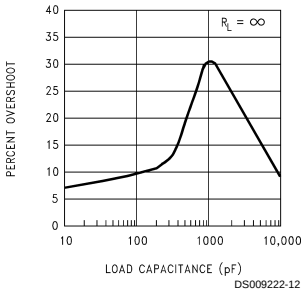
Frequency Response



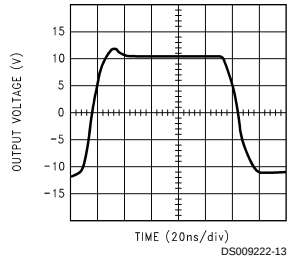
Slew Rate vs Temperature



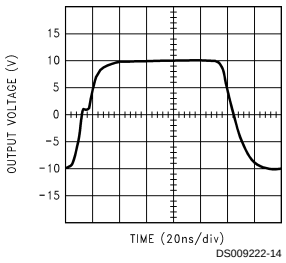
Overshoot vs Capacitive Load



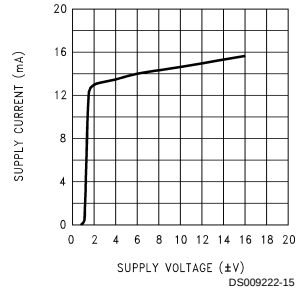
Large Signal Response (R_L = 1 kΩ)



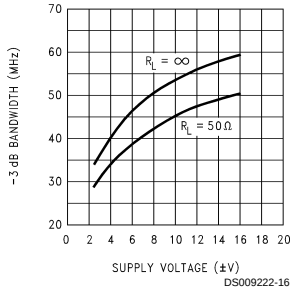
Large Signal Response (R_L = 50Ω)



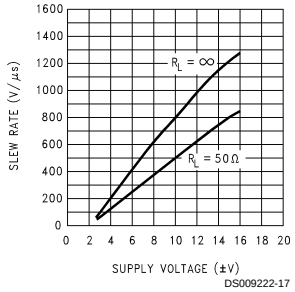
Supply Current



−3 dB Bandwidth

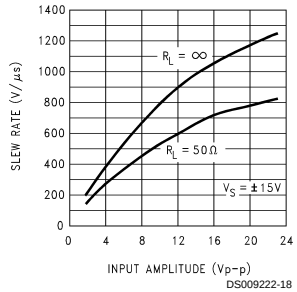


Slew Rate

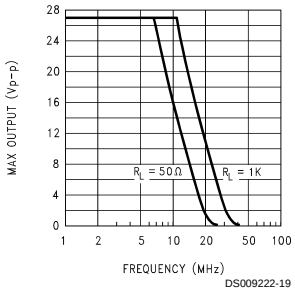


Typical Performance Characteristics T_A = 25˚C, V_S= ± 15V unless otherwise specified (Continued)

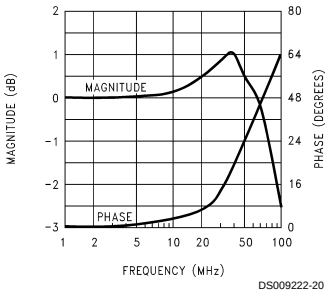
Slew Rate



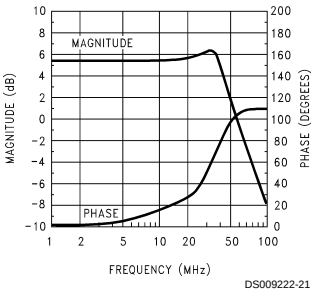
Power Bandwidth



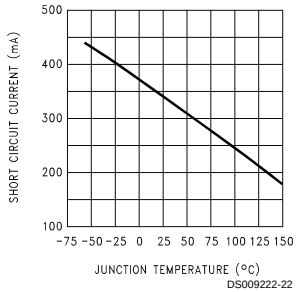
Input Return Gain (S11)



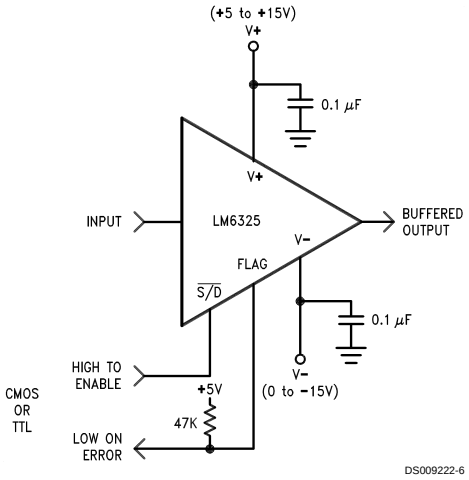
Forward Transmission Gain (S21)



Current Limit



Typical Connection Diagram



Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/µs into a 50Ω load produces a di/dt of 18 A/µs. Multiplying this by a wiring inductance of 50 nH results in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 µF ceramic in parallel with one or two 2.2 µF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

If the S/D pin is not to be used, it should be connected to V^+.

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

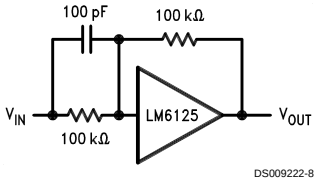
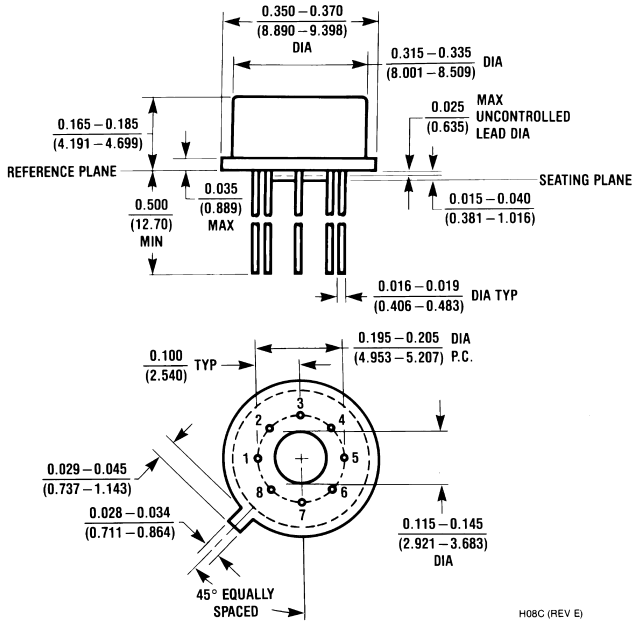
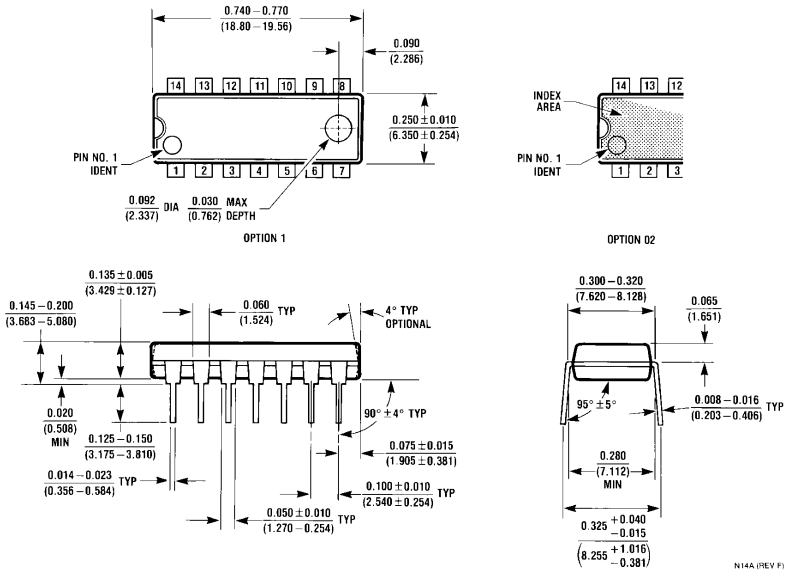


FIGURE 1. LM6125 with Overvoltage Protection

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
Order Number LM6125H/883 or LM6125H
NS Package Number H08C



Molded Dual-In-Line Package (N)
Order Number LM6225N or LM6325N
NS Package Number N14A

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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