Data Sheet June 2001 File Number 4839.2

Wireless LAN Medium Access Controller

The Intersil HFA3842 Wireless LAN Medium Access Controller is part of the PRISM® 2.4GHz radio chip set. The HFA3842 directly interfaces with the Intersil HFA386x family of Baseband Processors, offering a complete end-to-end chip set solution for wireless LAN products. Protocol and PHY support are implemented in firmware to allow custom protocol and different PHY transceivers.

The HFA3842 is designed to provide maximum performance with minimum power consumption. Package pin layout provides optimal PC board layout to all user interfaces.

Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgement, fragmentation and de-fragmentation, and automatic beacon monitoring are handed without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers. Additional firmware functions specific to access point applications are also available.

Designing wireless protocol systems using the HFA3842 is made easier with the availability of evaluation board, firmware, software device drivers, and complete documentation.

The HFA3842 is a WLAN MAC Controller IC, based on the HFA3841. Pin-for-pin upgrade replacement for the HFA3841.

Features

- New start up modes allow the PCMCIA Card Information Structure to be initialized from a serial EEPROM. This allows firmware to be downloaded from the host, eliminating the parallel Flash memory device.
- Firmware can be loaded from serial Flash memory.
- Direct attachment to a typical x16 SRAM using five control signals (RAMCS_, MOE_, MWEL_, MLBE_, and MUBE_).
- Low frequency crystal oscillator to maintain time and allow baseband clock source to power off during sleep mode.
- Improved performance of internal WEP engine.
- On-chip execution can now be viewed while in debug mode.
- Independent programmable cycle timing for external chip selects allows attachment of slow memory devices without compromising higher speed instruction execution.
- Pinout is backward compatible with HFA3841.
- IEEE802.11 Standard Data Rates: 1, 2, 5.5 and 11Mbps
- Part of the Intersil PRISM Wireless LAN Chip Set
- Full Implementation of the MAC Protocol Specified in IEEE Standards 802.11-1999 and 802.11b
- PCMCIA Host Interface Supports Full 16-Bit Implementation of PC Card 16 (1995), also ISA PNP with Additional Chip
- Host Interface Provides Dual Buffer Access Paths
- External Memory Interface Supports up to 4M bytes RAM
- Internal Encryption Engine Executes IEEE802.11 WEP
- Low Power Operation; 25mA Active, 8mA Doze, <1mA Sleep
- Operation at 2.7V to 3.6V Supply
- 5V Tolerant Host Interface Input/Outputs
- 128 Pin LQFP Package Targeted for Type II PC Cards
- IEEE802.11 Wireless LAN MAC Protocol Firmware and Microsoft® Windows® Software Drivers
- Pin for Pin Replacement for the HFA3841 Supporting all Functions and operations of the HFA3841

Applications

- High Data Rate Wireless LAN
- PC Card Wireless LAN Adapters
- PCI Wireless LAN Cards (Using Ext. Bridge Chip)
- Wireless LAN Modules
- Wireless LAN Access Points
- Wireless Bridge Products
- Wireless Point-to-Multipoint Systems
- ISA, ISA PNP WLAN Cards

Ordering Information

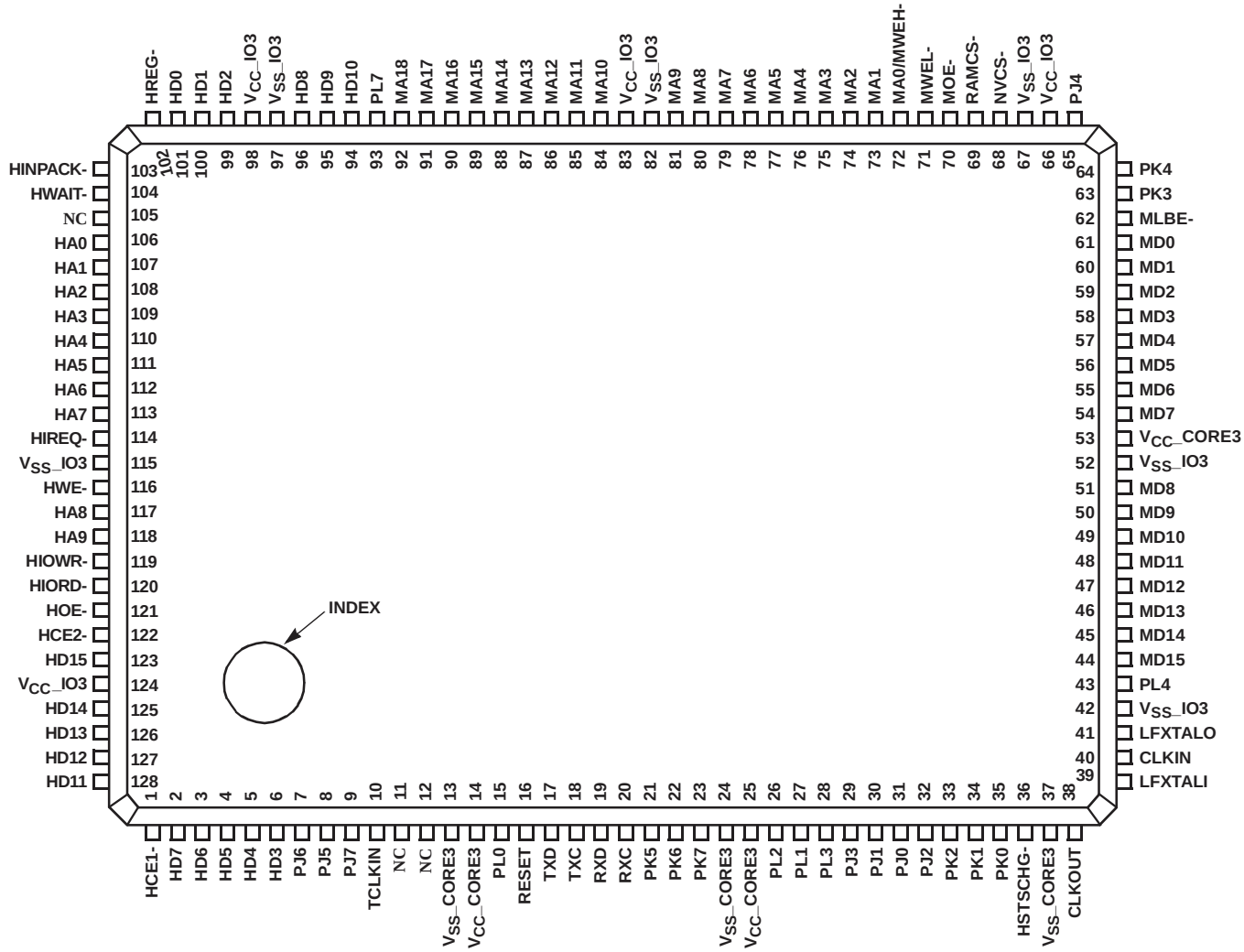
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3842IN	-40 to 85	128 Ld LQFP	Q128.14x20
HFA3842IN96	-40 to 85	Tape and Reel	

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PRISM® is a registered trademark of Intersil Americas Inc.
PRISM and design is a trademark of Intersil Americas Inc.

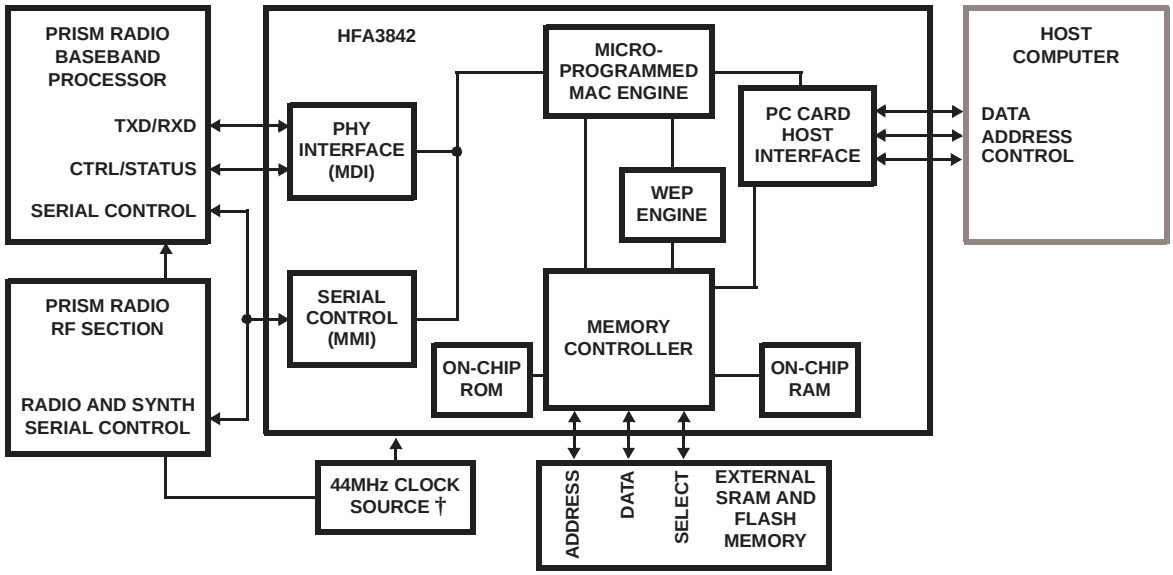
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pinout

128 LEAD LQFP



Simplified Block Diagram



HFA3842 Pin Descriptions

HOST INTERFACE PINS

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
HA0-9	106-113, 117, 118	5V Tol, CMOS, Input, 50K Pull Down	PC Card Address Input, Bits 0 to 9
HCE1-	1	5V Tol, CMOS, Input, 50K Pull Up	PC Card Select, Low Byte
HCE2-	122	5V Tol, CMOS, Input, 50K Pull Up	PC Card Select, High Byte
HD0-15	101-99, 6-2, 96-94, 128-125, 123	5V Tol, BiDir, 2mA, 50K Pull Down	PC Card Data Bus, Bit 0 to 15
HINPACK-	103	CMOS Output, 2mA	PC Card I/O Decode Confirmation
HIORD-	120	5V Tol, CMOS, Input, 50K Pull Up	PC Card I/O Space Read
HIOWR-	119	5V Tol, CMOS, Input, 50K Pull Up	PC Card I/O Space Write
HRDY/HIREQ-	114	CMOS Output, 4mA	PC Card interrupt Request (I/O Mode) Card Ready (Memory Mode)
HOE-	121	5V Tol, CMOS, Input, 50K Pull Up	PC Card Memory Attribute Space Output Enable
HREG-	102	5V Tol, CMOS, Input, 50K Pull Up	PC Card Attribute Space Select
HRESET	16	5V Tol, CMOS, ST Input, 50K Pull Up	Hardware Reset
HSTSCHG-	36	CMOS Output, 4mA	PC Card Status Change
HWAIT-	104	CMOS Output, 4mA	PC Card Not Ready (Force Host Wait State)
HWE-	116	5V Tol, CMOS Input, 50K Pull Up	PC Card Memory Attribute Space Write Enable

TABLE 1. MEMORY INTERFACE PINS

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
MUBE- / MA0 / MWEH-	72	CMOS TS Output, 2mA	MBUS Upper Byte Enable for x16 Memory; MBUS Address Bit 0 (byte) for x8 Memory; High Byte Write Enable for 2 x8 Memories
MA1-18	73-81, 84-92	CMOS TS Output, 2mA	MBUS Address Bits 1 to 18
PL4	43	CMOS BiDir, 2mA	MBUS Address Bit 19
PL5	12	CMOS BiDir, 2mA, 50K Pull Up	MBUS Address Bit 20
PL6	11	CMOS BiDir, 2mA	MBUS Address Bit 21
MLBE-	62	CMOS TS Output, 2mA, 50K Pull Up	MBUS Lower Byte Enable, or I/O as PM2
MOE-	70	CMOS TS Output, 2mA	Memory Output Enable
MWE- / MWEL-	71	CMOS TS Output, 2mA	Low (or only) Byte Memory Write Enable
RAMCS-	69	CMOS TS Output, 2mA	RAM Select
NVCS-	68	CMOS TS Output, 2mA	NV Memory Select
MD0-7	61-54	5V Tol, CMOS, BiDir, 2mA, 100K Pull Up	MBUS Low Data Byte, Bits 0 to 7
MD8-15	51-44	5V Tol, CMOS, BiDir, 2mA 50K Pull Down	MBUS High Data Byte, Bits 8 to 15

1

2

TABLE 2. GENERAL PURPOSE AND EEPROM PORT PINS

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION OF FUNCTION (IF OTHER THAN IO PORT)
GENERAL PURPOSE PORT PINS			
TXD	17	CMOS BiDir, 2mA, 50K Pull Down	Transmit Data Out
TXC	18	CMOS BiDir, 2mA	Transmit Clock In/Out
RXD	19	CMOS Input	Receive Data In
RXC	20	CMOS Input	Receive Clock In

TABLE 2. GENERAL PURPOSE AND EEPROM PORT PINS (Continued)

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION OF FUNCTION (IF OTHER THAN IO PORT)
PJ0	31	CMOS BiDir, 2mA, 50K Pull Down	MMI Clock (SCLK)
PJ1	32	CMOS BiDir, 2mA, 50K Pull Down	MMI Serial Data (SD)
PJ3	29	CMOS BiDir, 2mA	MMI Device Enable 0 (CS_BAR)
PJ4	65	CMOS BiDir, 2mA	MMI Device Enable 1 (PE1)
PJ5	8	CMOS BiDir, 2mA, 50K Pull Up	MBUS Request (LE_IF)
PJ6	7	CMOS BiDir, 2mA	MBUS Grant; LED
PJ7	9	CMOS BiDir, 2mA, 50K Pull Up	(RADIO_PE)
PK0	35	CMOS BiDir, 2mA, ST, 50K Pull Down	MPSI Clock (LE_RF)
PK1	34	CMOS BiDir, 2mA, 50K Pull Down	MPSI Data Out (SYNTHCLK)
PK2	33	CMOS BiDir, 2mA, 50K Pull Down	MPSI Data In (SYNTHDATA)
PK3	63	CMOS BiDir, 2mA	MPSI Device Select 0 (PA_PE)
PK4	64	CMOS BiDir, 2mA	MPSI Device Select 1 (PE2)
PK5	21	CMOS BiDir, 2mA	PHY Data Available (MDREADY)
PK6	22	CMOS BiDir, 2mA	PHY Medium Busy (CCA)
PK7	23	CMOS BiDir, 2mA	PHY Energy Detect (CAL_EN)
PL0	15	CMOS BiDir, 2mA	Transmitter Enable (TX_PE)
PL1	27	CMOS BiDir, 2mA	Receiver Enable (or PHY Sleep Control) (RX_PE)
PL2	26	CMOS BiDir, 2mA	PHY Reset (RESET_BB)
PL3	28	CMOS BiDir, 2mA	Antenna Select (T/R_SW_BAR)
PL4	43	CMOS BiDir, 2mA	MBUS Address Bit 19 (MA19)
PL5	12	CMOS BiDir, 2mA	MBUS Address Bit 20
PL6	11	CMOS BiDir, 2mA	MBUS Address Bit 21
PL7	93	CMOS BiDir, 2mA, Pull Down	PHY Transmit Ready (T/R_SW)
SERIAL EEPROM PORT PINS			
PJ0	31	CMOS BiDir	SCLK, Serial Clock
PJ1	30	CMOS BiDir, 50K Pull Down	SD, Serial Data Out
PJ2	32	CMOS BiDir, 50K Pull Down	MISO, Serial Data IN
TCLKIN (CS_)	10	CMOS BiDir	CS_, Chip Select

TABLE 3. CLOCKS

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
CLKIN	40	CMOS Input, ST Pull Down	External Clock Input (at >= 2X Desired MCLK Frequency, Typically 44-48MHz)
LFXTALI	39	Analog Input	32.768kHz Crystal Input (Note 2)
LFXTALO	41	CMOS Output, 2mA	32.768kHz Crystal Output
CLKOUT	38	CMOS, TS Output, 2mA	Clock Output (Selectable as MCLK, TCLK, or TOUT0)
TCLKIN	10	CMOS BiDir, 2mA, 50K Pull Down	Alternate clock input for timers

TABLE 4. POWER

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
V_{CC}	14, 25, 53, 66, 83, 98, 124	3.3V Supply	
V_{CC}_IO5	105	5V Tolerance Supply	
V_{SS}	13, 24, 37, 42, 52, 67, 82, 97, 115	GND	

ST = Schmitt Trigger (Hysteresis), TS = Three-State. Signals ending with "-" are active low.

NOTE:

3. Pin 39 (V_{CC}_CORE3 in 3841), has been reassigned as LFXTALI. For 3841 compatibility, it may be tied to V_{CC}.
   Pin 62 (TRST- in 3841) has been reassigned as MLBE. For 3841 compatibility, it may be tied low through 1K.
   Pin 105 (V_{CC}_IO5 in 3841) has been reassigned.For 3841 compatibility, it may be tied to V_{CC}.
   Output pins typically drive to positive voltage rail less 0.1V. Hence with a supply of 2.7V the output will just meet 5V TTL signal levels at rated loads.

TABLE 5. PORT PIN USES FOR PRISM APPLICATION

PIN	NAME	PRISM I USE	PRISM II USE
20	RXC	RXC - Receive Clock	RXC - Receive Clock
19	RXD	RXD - Receive Data	RXD - Receive Data
18	TXC	TXC - Transmit Clock	TXC - Transmit Clock
17	TXD	TXD - Transmit Data	TXD - Transmit Data
31	PJ0	SCLK - Clock for the SD Serial Bus	SCLK - Clock for the SD Serial Bus
30	PJ1	SD - Serial Bidirectional Data Bus	SD - Serial Bi-Directional Data Bus
32	PJ2	R/W - An input to the HFA3860A Used to Change the Direction of the SD Bus When Reading or Writing Data on the SD Bus	Not Used
29	PJ3	CS - A Chip Select for the Device to Activate the Serial Control Port (Active Low)	CS_BAR - Chip Select for HFA3861 Baseband (Active Low)
65	PJ4	Not Used	PE1 - Power Enable 1
8	PJ5	SYNTH_LE - Latches a Frame of 22 Bits After it has Been Shifted by the SCLK into the Synthesizer Registers	LE_IF - Load Enable for HFA3783 Quad IF
7	PJ6	LED - Activity Indicator	LED - Activity Indicator
9	PJ7	Not Used	RADIO_PE - RF Power Enable
35	PK0	Not Used	LE_RF - Load Enable for HFA3683 RF Chip
34	PK1	Not Used	SYNTHCLK - Serial Clock to Front End Chips
33	PK2	Not Used	SYNTHDATA - Serial Data to Front End Chips
63	PK3	TX_PE_RF - Power Enable	PA_PE - Transmit PA Power Enable
64	PK4	RX_PE_RF - Power Enable	PE2 - Power Enable 2
21	PK5	MD_RDY - Header Data and Data Packet are Ready to be Transferred From Baseband on RXD	MDREADY - Header Data and Data Packet are Ready to be Transferred from Baseband on RXD
22	PK6	CCA - Signal that the Channel is Clear to Transmit	CCA - Signal that the Channel is Clear to Transmit
23	PK7	RADIO_PE - Master Power Control for the RF Section	CAL_EN - Calibration Mode Enable
15	PL0	TX_PE and PA_PE - Transmit Enable to Baseband	TX_PE - Transmit Enable to Baseband
27	PL1	RX_PE - Receive Enable to Baseband	RX_PE - Receive Enable to Baseband
26	PL2	RESET - Reset to Baseband	RESET_BB - Reset Baseband
28	PL3	Not Used	T/R-SW_BAR - Transient/Receive Control (Inverted)
43	PL4	MA19 (If Required)	MA19 (If Required)
12	PL5	MA20 (If Required)	MA20 (If Required)
11	PL6	MA21 (If Required)	MA21 (If Required)
93	PL7	TX_RDY - Baseband Ready to Receive Data on TXD (Not Used By Firmware)	T/R_SW - Transmit/Receive Control

Absolute Maximum Ratings

Supply Voltage 3.6V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +3.3V
Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ($^oC/W$)
LQFP Package 50
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 100^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.6V, CLK Frequency 44MHz	-	33	45	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	$0.7V_{CC}$	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-	-	$0.3V_{CC}$	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	$0.9V_{CC}$	-	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.2	$0.1V_{CC}$	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. $T_A = 25^oC$	-	5	10	pF
Output Capacitance	C_{OUT}	CLK Frequency 1MHz. All measurements referenced to GND. $T_A = 25^oC$	-	5	10	pF

NOTE:
5. All values in this table have not been measured and are only estimates of the performance at this time.

AC Electrical Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CLOCK SIGNAL TIMING					
OSC Clock Period (Typ. 44MHz)	t_{CYC}	20	20.8	200	ns
High Width	t_{H1}	10	10.4	-	ns
Low Width	t_{L1}	10	10.4	-	ns
EXTERNAL MEMORY INTERFACE					
MOE_Setup Time From Ramcs	t_{S1}	0	-	-	ns
MOE-Setup Time From MA (17.0)	t_{S2}	0	-	-	ns
MA(18-1 Address Hold from MOE- Rising Edge	t_{H1}	20	-	-	ns
RAMCS Hold from MOE_ Rising Edge	t_{H2}	20	-	-	ns
MD(15:0) Enable from MOE-Falling	t_{E1}	5	-	-	ns
MD(15:0) Disable from MOE-Rising Edge	t_{D1}	-	-	100	ns
EXTERNAL WRITE MEMORY INTERFACE					
MA (18...0) Address Setup Time to MWE Falling Edge	t_{S3}	0	-	-	ns
RAMCS-Setup to MWE_	t_{S4}	0	-	-	ns
MA (17.0) Hold From MWE_Rising Edge	t_{H2}	15	-	-	ns
RAMCS_Hold From MWE_Rising Edge	t_{H3}	15	-	-	ns
MD (15.0) Setup to MWE_Rising	t_{S5}	40	-	-	ns
MD (15.0) Hold from MWE_Rising	t_{H4}	15	-	-	ns
SYNTHESIZER					
SYNTHCLK (PK1) Period	t_{CYC}	83	-	4,000	ns
SYNTHCLK (PK1) Width Hi	t_{H1}	$t_{CYC}/2$ - 10	-	$t_{CYC}/2$ + 10	ns
SYNTHCLK (PK1) Width Lo	t_{L1}	$t_{CYC}/2$ - 10	-	$t_{CYC}/2$ + 10	ns
SYNTHDATA (PK2) Hold Time from Falling Edge of SYNTHCLK (PK1)	t_{D2}	0	-	-	ns
SYNTHCLK (PK1) Falling Edge to SYNLE Inactive	t_{D3}	35	-	-	ns

AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYSTEM INTERFACE - PC CARD IO READ 16					
Data Delay After HIORD-	t_{DIORD}	-	-	100	ns
Data Hold Following HIORD-	t_{HIORD}	0	-	-	ns
HIORD- Width Time	t_{WIORD}	165	-	-	ns
Address Setup Before HIORD-	t_{SUA}	70	-	-	ns
Address Hold Following HIORD-	t_{HA}	20	-	-	ns
HCE(1, 2)- Setup Before HIORD-	t_{SUCE}	5	-	-	ns
HCE(1, 2)- Hold After HIORD-	t_{HCE}	20	-	-	ns
HREG- Setup Before HIORD-	t_{SUREG}	5	-	-	ns
HREG- Hold Following HIORD-	t_{HREG}	0	-	-	ns
HINPACK- Delay Falling from HIORD-	$t_{DFINPACK}$	0	-	45	ns
HINPACK- Delay Rising from HIORD-	$d_{DRINPACK}$	30	-	45	ns
Data Delay from HWAIT- Rising	t_{DRWT}	-	-	0	ns
HWAIT- Width Time	t_{WWT}	-	-	12,000	ns
SYSTEM INTERFACE - PC CARD IO WRITE 16					
Data Setup Before HIORD-	t_{SUIOWR}	30	-	92	ns
Data Hold Following HIORD-	t_{HIOWR}	20	-	-	ns
HIOWR- Width Time	t_{WIOWR}	165	-	-	ns
Address Setup Before HIORD-	t_{SUA}	70	-	-	ns
Address Hold Following HIORD-	t_{HA}	20	-	-	ns
HCE(1, 2)- Setup Before HIORD-	t_{SUCE}	5	-	-	ns
HCE(1, 2)- Hold Following HIORD-	t_{HCE}	20	-	-	ns
HREG- Setup Before HIORD-	t_{SUREG}	5	-	-	ns
HREG- Hold Following HIORD-	t_{HREG}	0	-	-	ns
HWAIT- Delay Falling from HIORD-	t_{DFWT}	-	-	35	ns
HWAIT- Width Time	t_{WWT}	-	-	12,000	ns
HIOWR- High from HWAIT- High	t_{DRIOWR}	0	-	-	ns
RADIO TX DATA - TX PATH					
TXC Period	t_{TXC}	$4^* t_{TMCK}$	-	-	ns
TXC Width Hi	t_{CHM}	31	-	-	ns
TXC Width Lo	t_{CLM}	31	-	-	ns
RADIO RX DATA - RX PATH					
RX_RDY Setup Time to RXC Positive Edge (See Note 5)	t_{SURX_RDY}	10	-	-	ns
RX_RDY Hold Time from RXC Positive Edge (See Note 6)	t_{HRX_RDY}	45	-	-	ns
RX_PE2 Delay from RX_RDY deAssert (See Note 10)	t_{DRX_PE2}	-	$3 * t_{MCLK}$	-	ns
RX_PE2 Low Pulse Width (See Note 9)	t_{WRX_PE2}	-	$4 * t_{MCLK}$	-	ns
RXD Setup Time to RXC Positive Edge (See Note 7)	t_{SURXD}	10	-	-	ns
RXD Hold Time from RXC Positive Edge (See Note 7)	t_{HRXD}	0	-	-	ns
RXC Period (See Note 12)	t_{RXC}	-	$3 * t_{MCLK}$	-	ns
RXC Width Hi	t_{RCHM}	31	-	-	ns
RXC Width Lo	t_{RCLM}	31	-	-	ns

NOTES:

6. MD_RDY is and'ed with RXC_ONE_SHOT (RXDAV) to shift data in shift register. RX_RDY is not required to be valid until 1 MCLK after RXC is sampled high. Therefore, a negative setup time could be used. Since this is an unlikely scenario, we will leave it at a nominal 10ns setup time.
7. MD_RDY is and'ed with RXC_ONE_SHOT (RXDAV) to shift data in shift register. Therefore, for the last data bit, the MD_RDY must be held active until RXC_ONE_SHOT is sampled high by MAC's MCLK. However, it is assumed that BBP will be used in a mode that keeps RX_RDY (MD_RDY) and RXC running until RX_PE2 is de-asserted. The MAC will stop processing data after the number of bits retrieved from the PLCP header length field are received. Therefore, the RX_RDY hold time with respect to RXC does not matter. However, should the RX_RDY signal be cleared when the last RXD bit is received the hold time w/r RXC must be honored.
8. RXC positive edge clocks a flop which stores the RXD for internal usage.
9. RXC period (and Hi/Lo times) must be long enough for flops clocked by MAC MCLK to see 1 RXC high and 1 RXC low.
10. RX_PE inactive width at BBP is 3 BBP CLK's. Since BBP CLK and MAC CLK can be async minimum should be 4 MAC CLKs.
11. When RX_RDY drops before expected number of RXD bits is received, then TX/RX FSM in mpctl.v signals timers which clear rx_pe2_int.

Waveforms

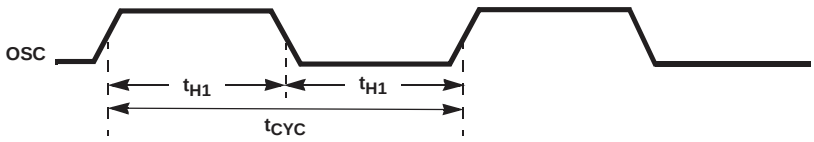


FIGURE 1. CLOCK SIGNAL TIMING

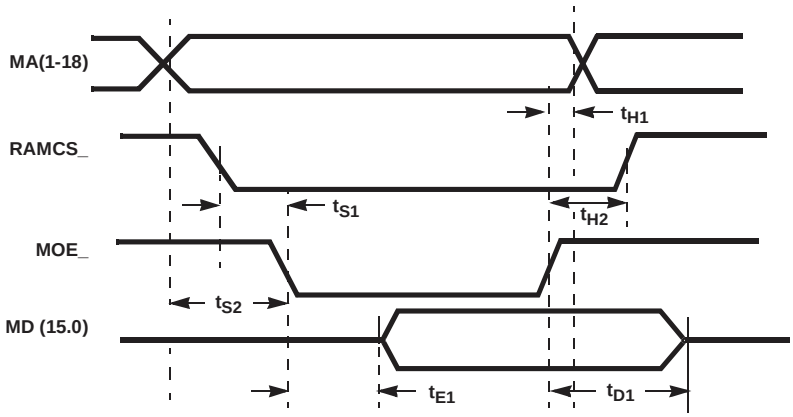


FIGURE 2. EXTERNAL MEMORY READ TIMING

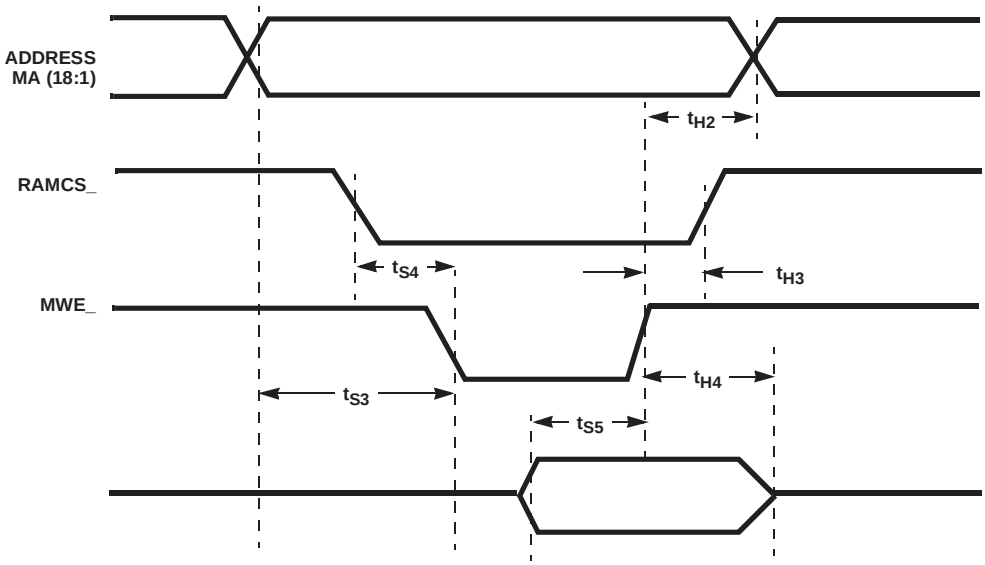


FIGURE 3. EXTERNAL MEMORY WRITE TIMING

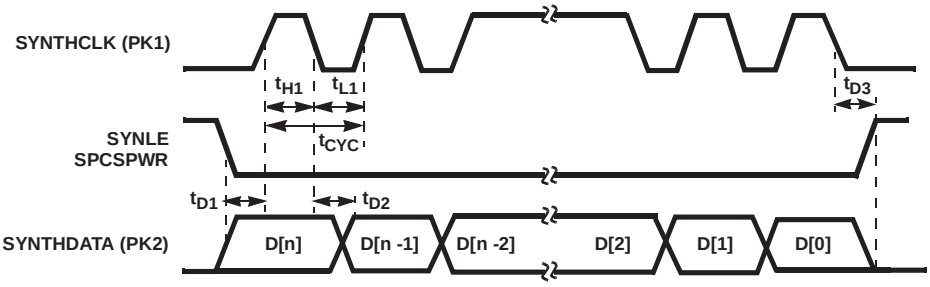


FIGURE 4. SYNTHESIZER

Waveforms (Continued)

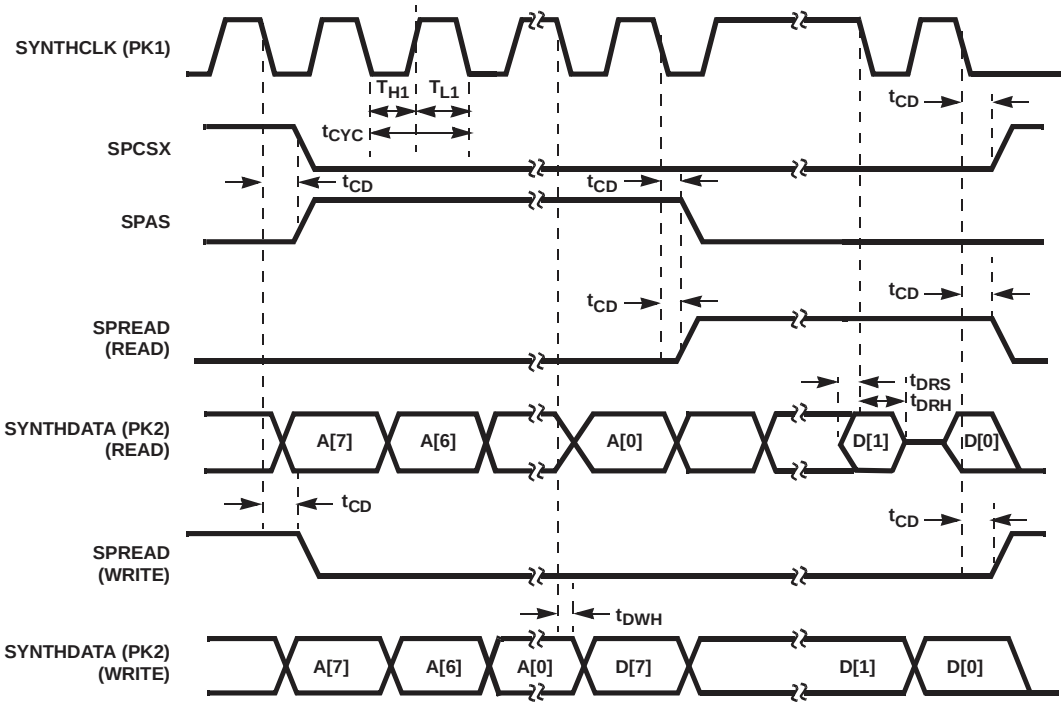


FIGURE 5. SERIAL PORT - HFA3824A/HFA3860B

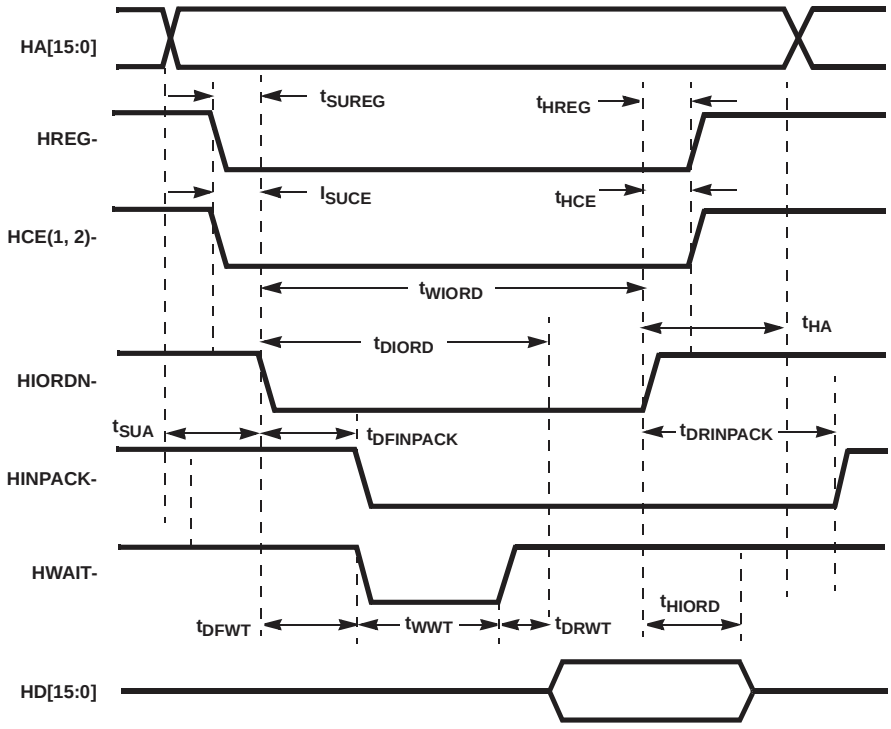


FIGURE 6. PC CARD IO READ 16

Waveforms (Continued)

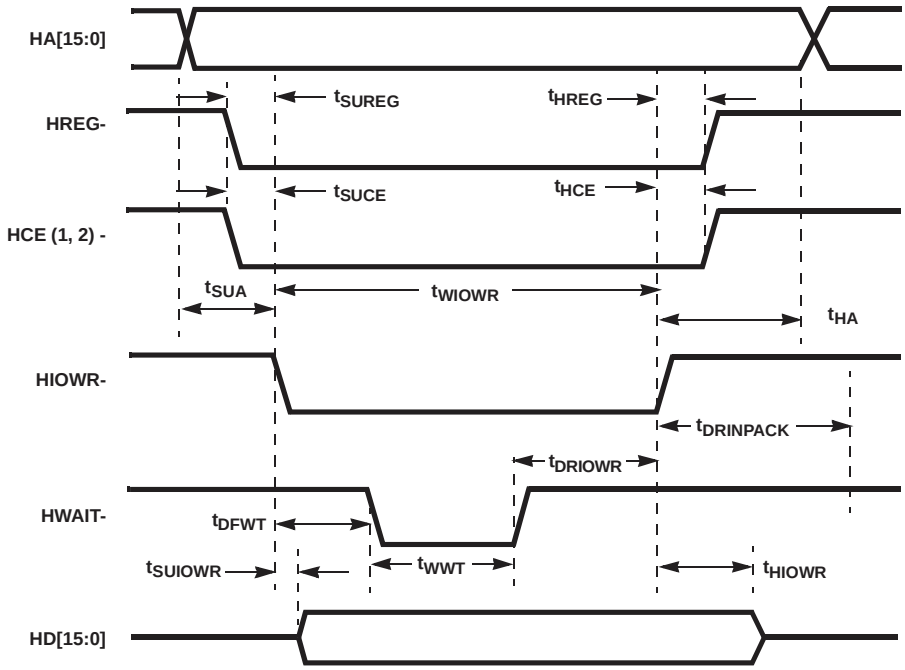


FIGURE 7. PC CARD IO WRITE 16

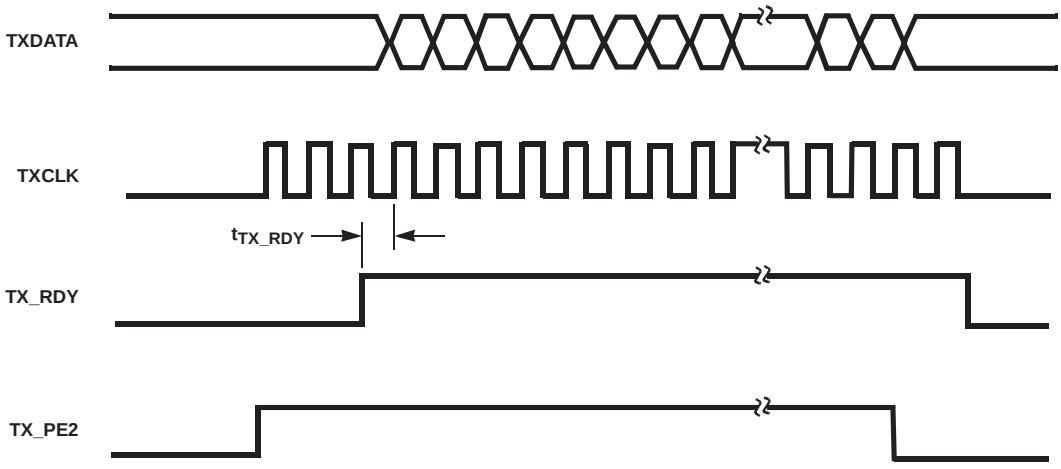


FIGURE 8. TX PATH

Waveforms (Continued)

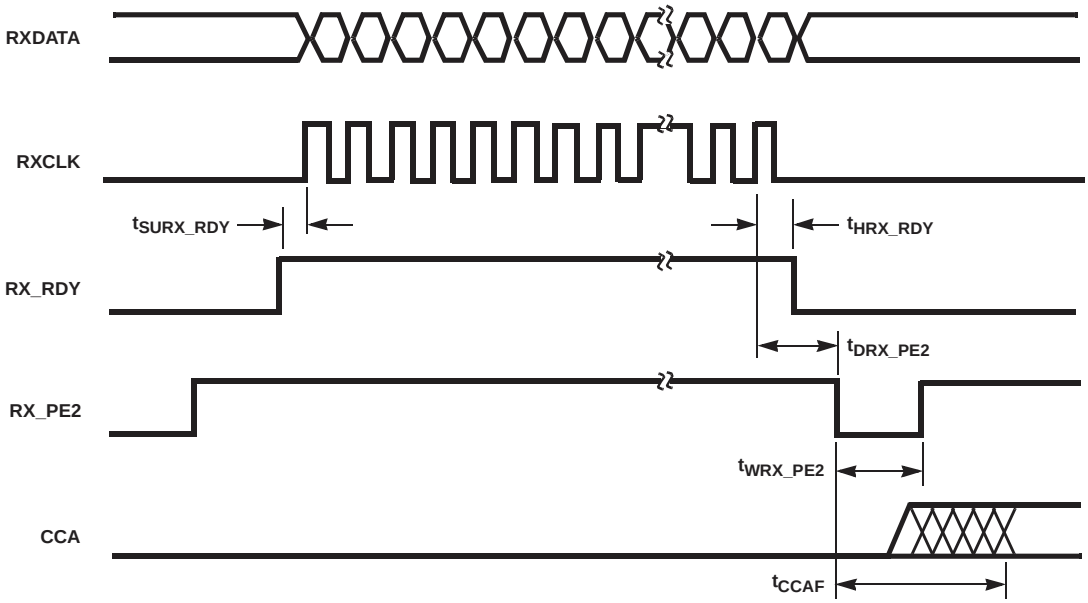


FIGURE 9. RX PATH

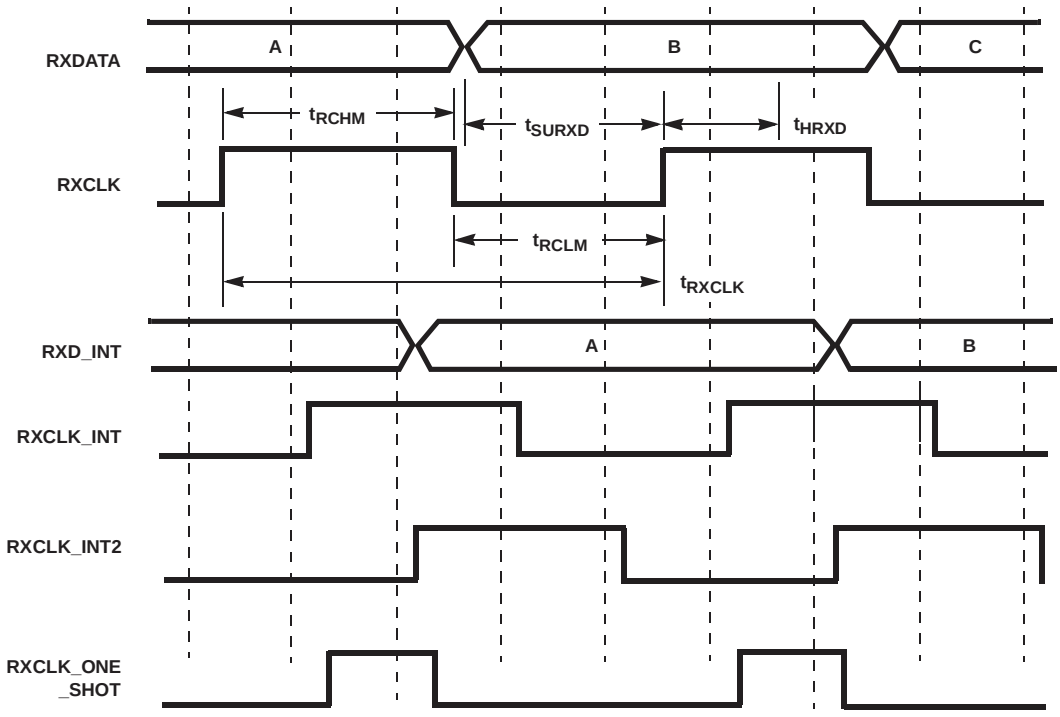


FIGURE 10. EXPANDED RX TIMING

HFA3842 System Overview

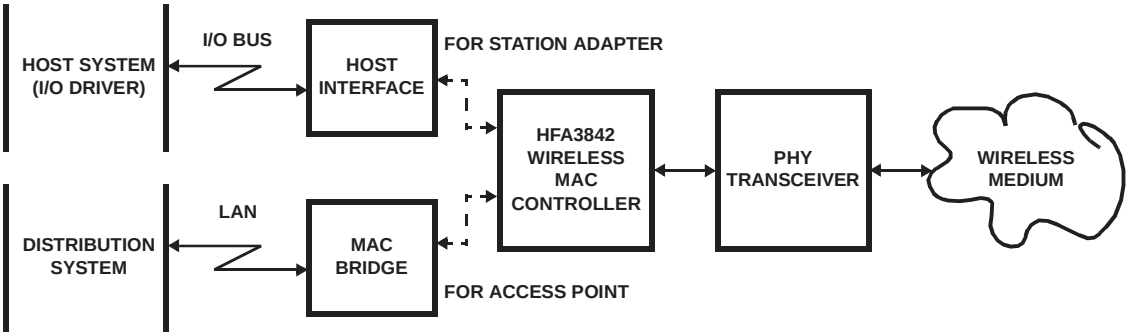


FIGURE 11. TYPICAL APPLICATION

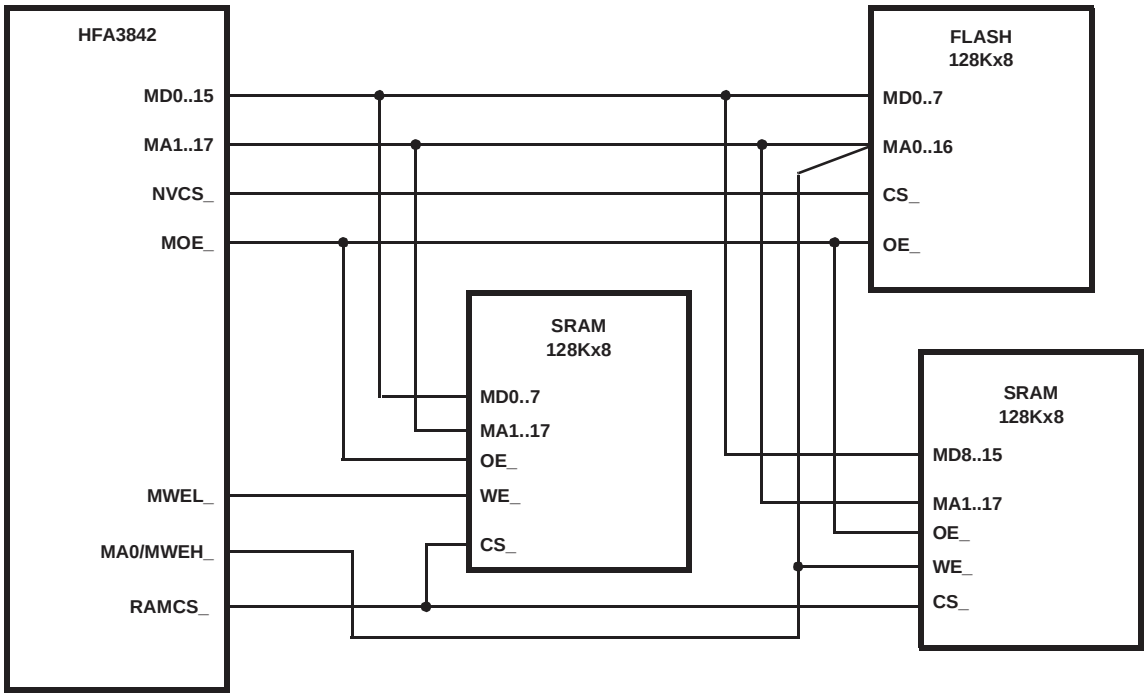


FIGURE 12. 8-BIT MEMORY INTERFACE

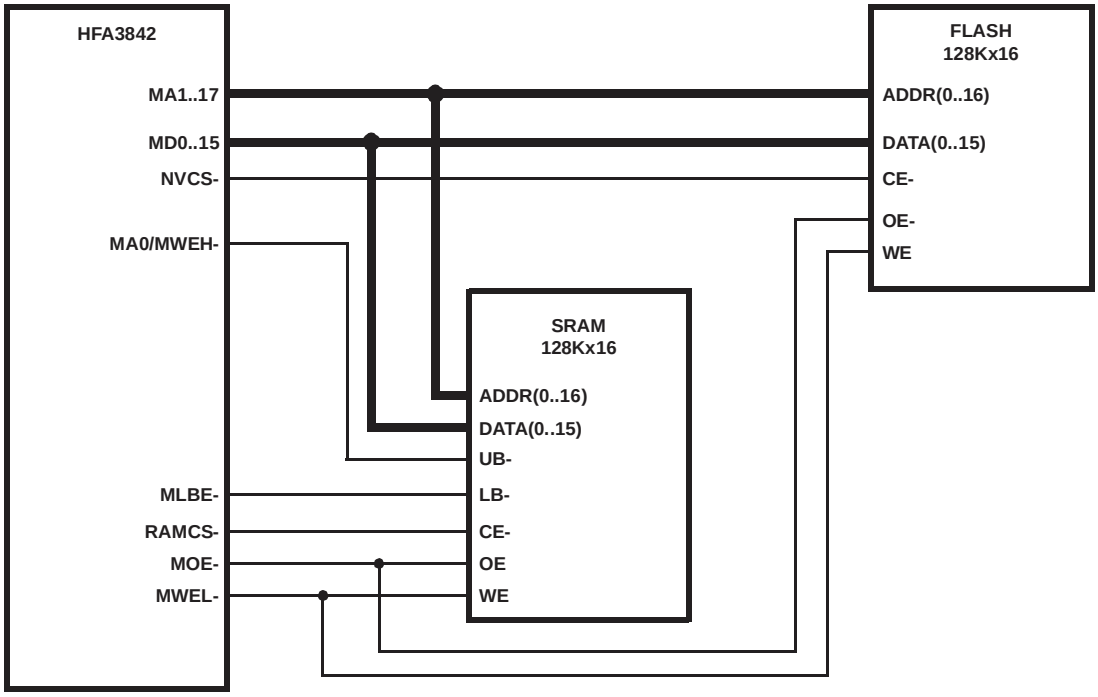


FIGURE 13. 16-BIT MEMORY INTERFACE

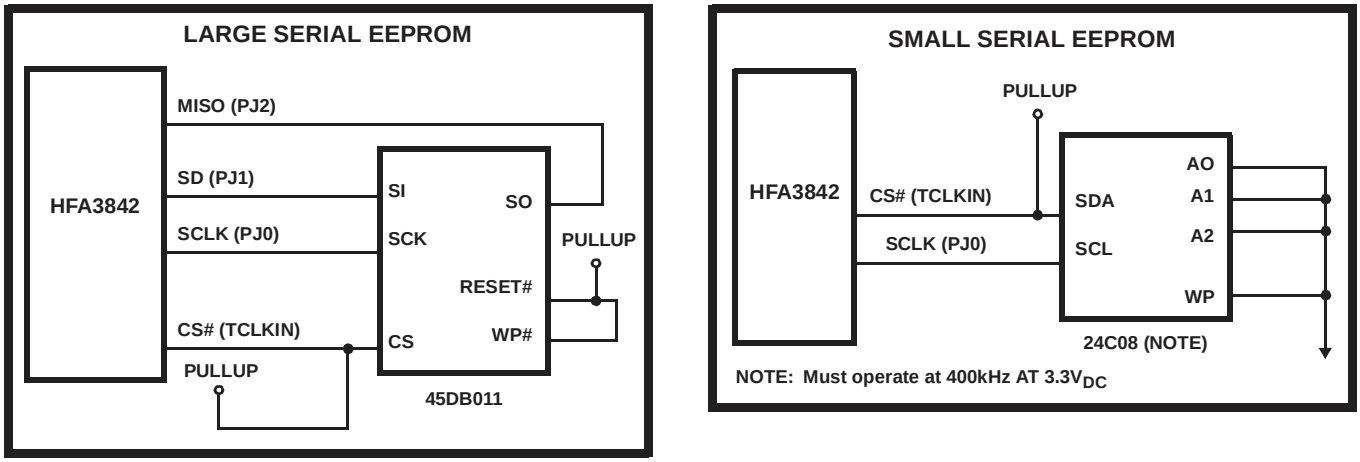


FIGURE 14. SERIAL EEPROM INTERFACE

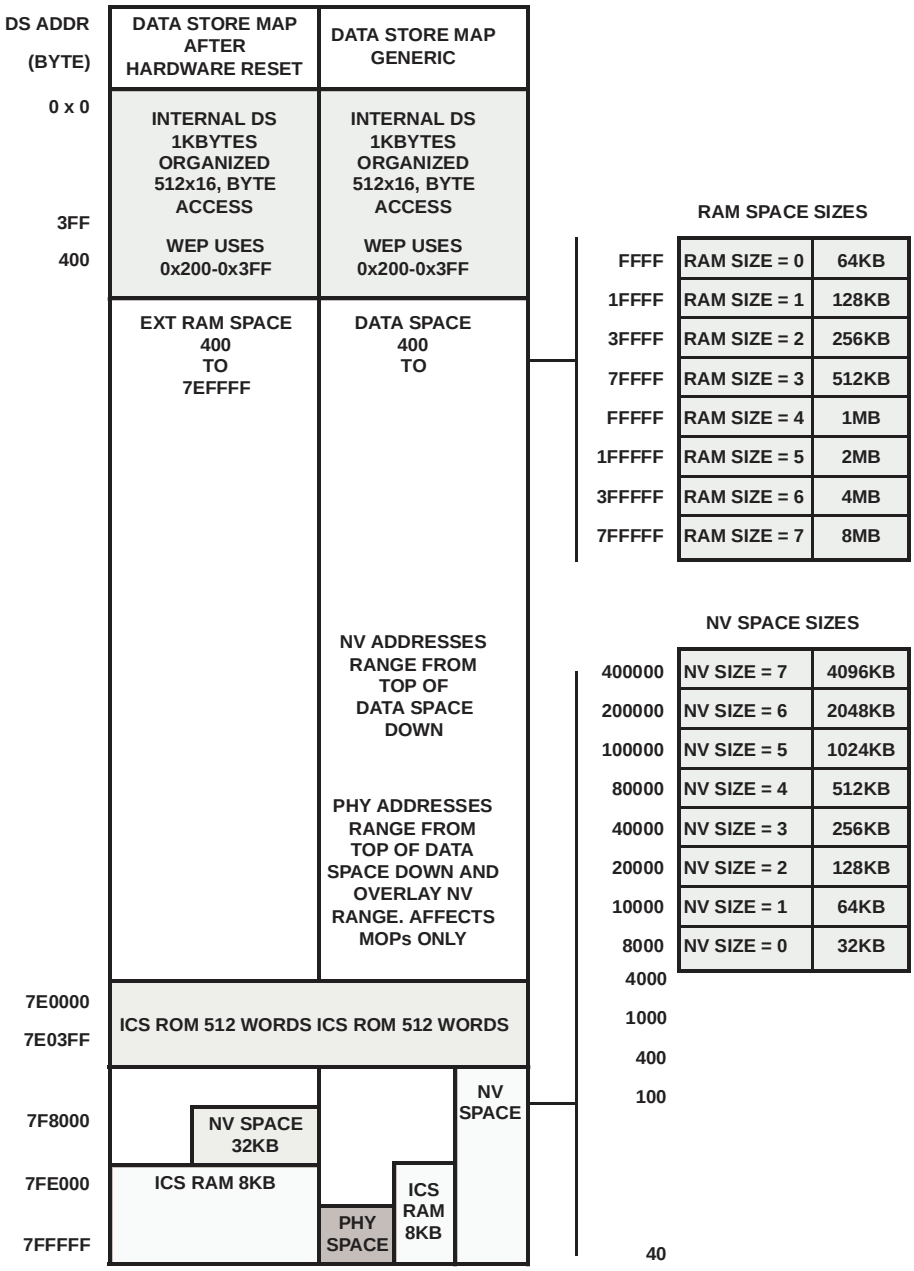


FIGURE 15. MEMORY MAP

External Memory Interface

The HFA3842 provides separate external chip selects for code space and data storage space. Code space is accessible as data space through an overlay mechanism, except for an internal ROM. Refer to Figures 12, 13 and 14 for HFA3842 memory configuration details. Refer to Figure 15 for memory map.

The maximum possible memory space size is 4Mbytes.

Most of the data store space is reserved for storage of received and transmitted data, with some areas reserved for use by firmware. However, a portion of the data store may be allocated as code store. This permits higher speed instruction execution, by using fast RAMs, than is possible from Flash memories. The maximum size of this overlay is the full code space address range, 128Kbytes, and is allocated in independent sections of 16KBytes each, on 16Kbyte boundaries, ranging from the highest address of the actual physical memory space and extending down.

Mapping code execution to RAM requires the RAM to have code written into it. Typically, this is done by placing code in a non-volatile memory such as a Flash in the code space. At initialization, the code in the non-volatile memory transfers itself to RAM, maps the appropriate blocks of the code space to the

RAM, and then branches to begin execution from RAM. This allows low cost, slow Flash devices to hold an entire code image, which can be executed much faster from RAM. If code is not placed in an external non-volatile memory as described here, it must be transferred to the RAM via the Host Interface.

Slow memories are not dynamically sensed. Following reset, the instruction clock operates with a slower cycle while the Flash is copied to RAM. Once code has been copied from Flash to RAM, execution transfers to RAM and the clock is raised to the normal operating frequency.

As mentioned above, it is feasible to operate without a code image in a non-volatile memory. In such a system, the firmware must be downloaded to RAM through the host interface before operation can commence.

The external SRAM memory must be organized in a 16-bit width to provide adequate performance to implement the 802.11 protocol at 11Mb/s rates. Systems designed for lower performance applications may be able to use 8-bit wide memory.

The minimum external memory is 128Kbytes of SRAM, organized 8 or 16 bits wide. Typical applications, including 802.11 station designs, use 256Kbytes organized 128K x 16. An access point application could make use of the full address space of the device with 4Mbytes organized a 2M x 16.

The HFA3842 supports 8 or 16 bit code space, and 8 or 16-bit data space. Code space is typically populated with the less expensive Flash memory available, usually an 8-bit device. Data space is usually populated with high-speed RAMs configured as a 16-bit space. This mixing of 8/16 bit spaces is fully supported, and may be done in any combination desired for code and data space.

The HFA3842 supports direct control of single chip 16-bit wide SRAMs with high/low byte enables, as well as direct control of a 16-bit space constructed from 8-bit wide SRAMs. The type of memory configuration is specified via the appropriate MD pin, sensed when the HFA3842 is reset.

HFA3842 pin MUBE-/MA0/MWEH- functions as Address 0 for 8-bit access, (such as Flash) as MWEH (High Byte Write Enable) when two x8 memories are configured as a single x16 space, and as the upper Byte Enable when a single x16 memory is used. No external logic is required to generate the required signals for both types of memory configurations, even when both exist together; all that is required is for the HFA3842 code to configure the HFA3842 memory controller to generate the proper signals for the particular address space being accessed.

For 8-bit spaces, the HFA3842 dynamically configures pin MUBE-/MA0/MWEH- cycle-by-cycle as the address LSB. MWEL-/MWE- is the only write control, and MOE- is the read output enable.

For 16-bit spaces constructed from 8-bit memories, the HFA3842 dynamically configures pin MUBE-/MA0/MWEH- cycle-by-cycle as the high byte write enable, MWEL- as the low write enable signal, and MOE- as the read output enable.

For 16-bit spaces constructed from single-chip x16 memories (such as SRAMs), the HFA3842 dynamically configures pin MUBE_/MA0/MWEH- cycle-by-cycle as the upper byte enable. Pin MLBE- is connected as the low byte enable, MWEL-/MWE- is the write control, and MOE- is the read output enable.

These memory implementations require no external logic. The memory spaces may each be constructed from any type of memory desired. The only restriction is that a single memory space must be constructed from the same type of memory; for example, data space may not use both x8 and x16 memories, it must be all x8, or all x16. This restriction does not apply across memory spaces; e.g., code space may use a x8 memory and data space a single x16 memory, or code space two x8 memories and data space a single x8 memory.

Contact the factory for additional information in regards to HFA3842 to PRISM II MAC-less Connections.

Serial EEPROM Interface

The HFA3842 contains a small on-chip ROM Firmware which was added to allow the CIS or CIS plus firmware image to be transferred from an off-chip serial non-volatile memory device to RAM after a system Reset. This allows a system configuration without a parallel Flash Device. The operating frequency of the serial port is 400kHz with a voltage of 3.3V. Refer to Figure 14 for additional details on configuring the serial memory of the HFA3842. The Power On Reset Configuration section in this data sheet provides additional details on memory selection and control after a Reset condition.

Host Interface

PC Card Physical Interface

The Host interface is compatible to the PC Card 95 Standard (PCMCIA v2.1). The HFA3842 Host Interface pins connect directly to the correspondingly named pins on the PC Card connector with no external components (other than resistors) required. The HFA3842 operates as an I/O card using less than 64 octet locations. Reads and writes to internal registers and buffer memory are performed by I/O accesses. Attribute memory (256 octets) is provided for the CIS table which is located in external memory. Common memory is not used.

The following describes specific features of various pins:

HA[9:0]

Decoding of the system address space is performed by the HCEx-. During I/O accesses HA[5:0] decode the register. HA[9:6] are ignored when the internal HAMASK register is set to the defaults used by the standard firmware. During attribute memory accesses HA[9:1] are used.

HD[15:0]

The host interface is primarily designed for word accesses, although all byte access modes are fully supported. See HCE1-, HCE2- for a further description. Note that attribute memory is specified for and operates with even bytes accesses only.

HCE1-, HCE2-

The PC Card cycle type and width are controlled with the CE signals. Word and Byte wide accesses are supported, using the combinations of HCE1-, HCE2-, and HA0 as specified in the PC Card standard.

HWE-, HOE-

HOE- and HWE- are only used to access attribute memory. Common Memory, as specified in the PC Card standard, is not used in the HFA3842. HOE- is the strobe that enables an attribute memory read cycle. HWE- is the corresponding strobe for the attribute memory write cycle. The attribute space contains the Card Information Structure (CIS) as well as the Function Configuration Registers (FCR).

HIORD-, HIOWR-

HIORD- and HIOWR- are the enabling strobes for register access cycles to the HFA3842. These cycles can only be performed once the initialization procedure is complete and the HFA3842 has been put into IO mode.

HREG-

This signal must be asserted for I/O or attribute cycles. A cycle with HREG- unasserted will be ignored as the HFA3842 does not support common memory.

HINPACK-

This signal is asserted by the HFA3842 whenever a valid I/O read cycle takes place. A valid cycle is when HCE1-, HCE2-, HREG-, and HIORD- are asserted, once the initialization procedure is complete.

HWAIT-

Wait states are inserted in accesses using HWAIT-. The host interface synchronizes all PC Card cycles to the internal HFA3842 clock. The following wait states should be expected:

Direct Read or Write to Hardware Register

- 1/2 to 1 MCLK assertion of HWAIT- for internal synchronization.

Write to Memory Mapped Register, Buffer Access Path, or Attribute Space (Post-Write)

- The data required for the write cycle will be latched and therefore only the synchronizing wait state will occur.
- Until the queued cycle has actually written to the memory, any subsequent access by the Host will result in a WAIT.

Read to Attribute Space and Memory Mapped Registers

- WAIT will assert until the memory arbitration and access have completed.

Buffer Access Paths, BAP0 and BAP1

- An internal Pre-Read cycle to memory is initiated by a host Buffer Read cycle, after the internal address pointer has auto-incremented. If the next host cycle is a read to the same buffer, the data will be available without a memory arbitration delay.
- A single register holds the pre-read data. Thus, any read access to any other memory-mapped register (or the other buffer access path) will result in the pre-read data becoming invalidated.
- If another read cycle has invalidated the pre-read, then a memory arbitration delay will occur on the next buffer access path read cycle.

HIREQ-

Immediately after reset, the HIREQ- signal serves as the RDY/BSY (per the PC Card standard). Once the HFA3842 firmware initialization procedure is complete, HIREQ- is configured to operate as the interrupt to the PC Card socket controller. Both Level Mode and Pulse Mode interrupts are supported. By default, Level mode interrupts are used, so the interrupt source must be specifically acknowledged or disabled before the interrupt will be removed.

HRESET

When reset is removed, the CIS table is initialized and, once complete, HIREQ- is set high (HIREQ- acts as RDY/BSY from reset and is set high to indicate the card is ready for use). The CIS table resides in Flash memory and is copied to RAM during firmware initialization. The host system can then initialize the card by reading the CIS information and writing to the configuration register.

ISA PnP

The HFA3842 can be connected to the ISA bus and operate in a Plug and Play environment with an additional chip such as the Fujitsu MB86703, Texas Instruments TL16PNP200A, or Fairchild Semiconductor NM95MS15. See the Application Note AN9874, “ISA Plug and Play with the HFA3841” for more details.

Register Interface

The logical view of the HFA3842 from the host is a block of 32 word wide registers. These appear in IO space starting at the base address determined by the socket controller. There are three types of registers.

HARDWARE REGISTERS (HW)

- 1 to 1 correspondence between addresses and registers.
- No memory arbitration delay, data transfer directly to/from registers.
- AUX base and offset are write-only, to set up access through AUX data port.

- Note: All register cycles, including hardware registers, incur a short wait state on the PC Card bus to ensure the host cycle is synchronized with the HFA3842's internal MCLK.

MEMORY MAPPED REGISTERS IN DATA RAM (MM)

- 1 to 1 correspondence.
- Requires memory arbitration, since registers are actually locations in HFA3842 memory.
- Attribute memory access is mapped into RAM as Base-address + 0x400.
- AUX port provides host access to any location in HFA3842 RAM (reserved).

BUFFER ACCESS PATH (BAP)

- No 1 to 1 correspondence between register address and memory address (due to indirect access through buffer address pointer registers).
- Auto increment of pointer registers after each access.
- Require memory arbitration since buffers are located in HFA3842 memory.
- Buffer access may incur additional delay for Hardware Buffer Chaining.

TABLE 6. MEMORY MAPPED REGISTER

I/O OFFSET	NAME	TYPE
00	Command	MM
02	Param0	MM
04	Param1	MM
06	Param2	MM
08	Status	MM
0A	Resp0	MM
0C	Resp1	MM
0E	Resp2	MM
10	InfoFID	MM
20	RxFID	MM
22	AllocFID	MM
24	TxComplFID	MM
18	BAP Select0	MM
1C	BAP Offset0	MM
36	BAP Data0	BAP
1A	BAP Select1	MM
1E	BAP Offset1	MM
38	BAP Data1	BAP
30	EvStat	HW
32	IntEn	HW
34	EvAck	HW
14	Control	MM
28	SwSupport0	MM
2A	SwSupport1	MM
2C	SwSupport2	MM
3A	AuxBase	HW
3C	AuxOffset	HW
3E	AuxData	(Reserved)

Buffer Access Paths

The HFA3842 has two independent buffer access paths, which permits concurrent read and write transfers. The firmware provides dynamic memory allocation between Transmit and Receive, allowing efficient memory utilization. On-the-fly allocation of (128-byte) memory blocks as needed for reception wastes minimal space when receiving fragments. The HFA3842 hides management of free memory from the driver, and allows fast response and minimum data copying for low latency. The firmware provides direct access to TX and RX buffers based on Frame ID (FID). This facilitates Power Management queuing, and allows dynamic fragmentation and defragmentation by controller. Simple Allocate/Deallocate commands ensure low host CPU overhead for memory management.

Hardware buffer chaining provides high performance while reading and writing buffers. Data is transferred between the host driver and the HFA3842 by writing or reading a single register location (The Buffer Access Path, or BAP). Each access increments the address in the buffer memory. Internally, the firmware allocates blocks of memory as needed to provide the requested buffer size. These blocks may not be contiguous, but the firmware builds a linked list of pointers between them. When the host driver is transferring data through a buffer access path and reaches the end of a physical memory block, hardware in the host interface follows the linked list so that the buffer access path points to the beginning of the next memory block. This process is completely transparent to the host driver, which simply writes or reads all buffer data to the same register. If the host driver attempts to access beyond the end of the allocated buffer, subsequent writes are ignored, and reads will be undefined.

PHY Interface

The HFA3842 is intended to support the PRISM family of Baseband processors with no additional components. This family currently includes the HFA3860B, HFA3861B, HFA3861 and HFA3863 baseband processors and the other ICs in the PRISM radio chip set. (Other baseband processors may be supported with custom firmware. See your sales representative for more information). The HFA3842 interfaces to the HFA386X baseband processors through two serial interfaces. The Modem Management Interface (MMI) is used to read and write internal registers in the baseband processor and access per-packet PLCP information. The Modem Data Interface (MDI) provides the receive and transmit data paths which transfer the actual MPDU data.

Serial Control Port (MMI)

The HFA3842 has a serial port that is used to program the baseband processor. There are individual chip selects and shared clock and data lines.

The MMI is used to program the registers and functionality of the PHY baseband processor.

PHY BASEBAND PROCESSOR

The PHY baseband processor is programmed by HFA3842 firmware.

The PRISM II baseband processor mode works as follows:

The Control Port consists of 3 signals: SD (serial data), SCLK (serial clock), and CS_BAR (active-low chip select).

Control Port signaling for read and write operations is illustrated in Figures 17 and 18 respectively. Detailed timing relationships appear in Figure 19 and timing specifications are contained in Table 7.

The BBP always uses the rising edge when clocking data on the Control Port. This means that when the BBP is receiving data it uses the rising edge of clock to sample; when driving data, transitions occur on the rising edge.

Address bits 6 through 1 are significant for selecting configuration registers. Address bits 7 and 0 are unused. See the BBP Programming section for register addresses and suggested values.

For read operations, the rising edge of R/W must occur after the 7th but prior to the 8th rising edge of SCLK. This ensures that the first data bit is clocked out of the BBP prior to the edge used to clock it into the MAC.

For more detailed information on the Control Port and BBP register programming see the HFA386x data sheets.

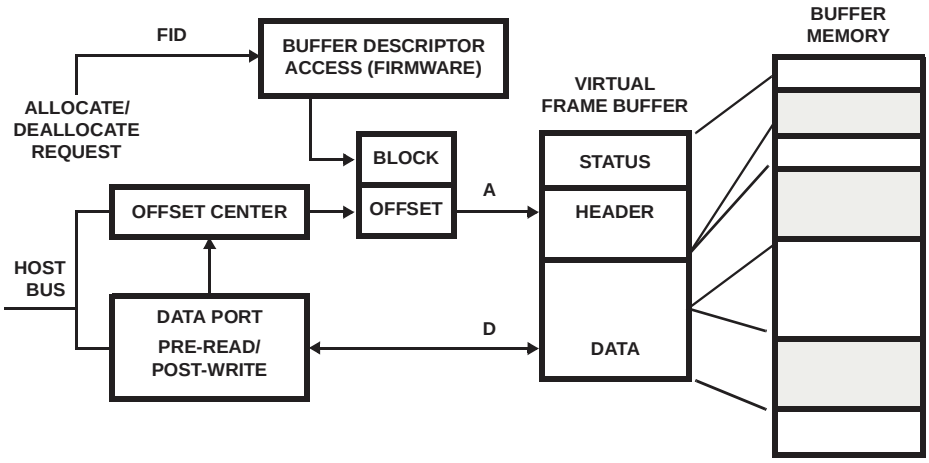


FIGURE 16. BLOCK DIAGRAM OF A BUFFER ACCESS PATH

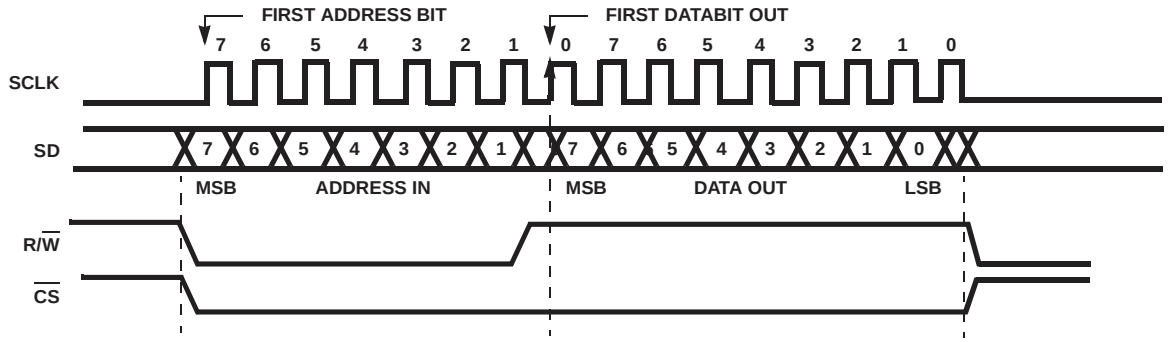


FIGURE 17. PRISM II BASEBAND PROCESSOR CONTROL PORT READ TIMING

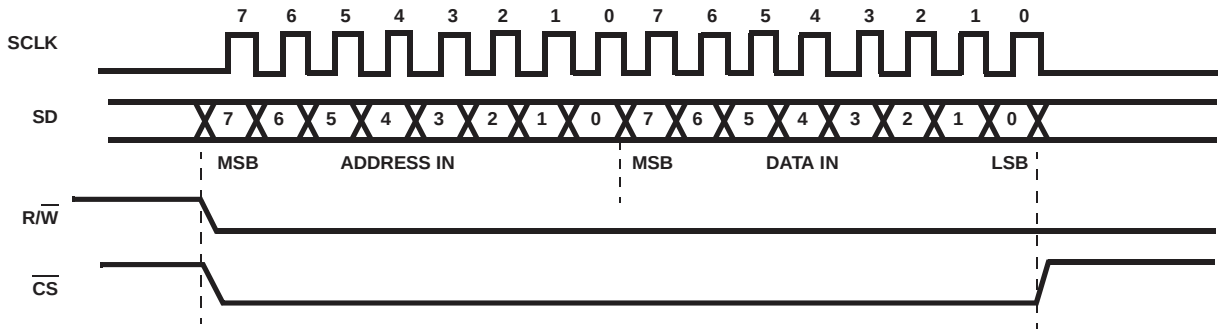


FIGURE 18. PRISM II BASEBAND PROCESSOR SERIAL CONTROL PORT WRITE TIMING

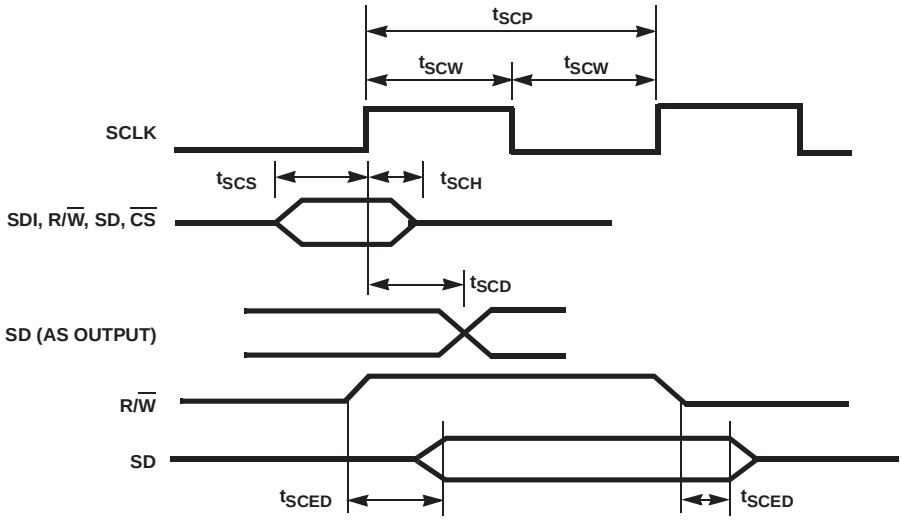


FIGURE 19. BBP CONTROL PORT SIGNAL TIMING

TABLE 7. BBP CONTROL PORT AC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
SCLK Clock Period	t_{SCP}	90	-	ns
SCLK Width Hi or Low	t_{SCW}	20	-	ns
Setup to SCLK + Edge (SD, SDI, R/W, CS)	t_{SCS}	30	-	ns
Hold Time from SCLK + Edge (SD, SDI, R/W, CS)	t_{SCH}	0	-	ns
SD Out Delay from SCLK + Edge	t_{SCD}	-	30	ns
SD Out Enable/Disable from R/W	t_{SCED}	-	15	ns

SYNTHESIZER

For the PRISM II, the synthesizer is programmed by firmware using different pins than the MMI. The HFA3842 will exchange data with the baseband during transmit and receive operations over the MMI interface. If the MMI interface was connected to the front end chips, the transitions on SCLK and SD could couple noise into them. The synthesizer serial bus consists of SYNTHDATA, SYNTHCLK, LE_IF and LE_RF. SYNTHDATA is on pin PK2, SYNTHCLK is on PK1, LE_IF is the enable for the HFA3783 Quad IF chip, and LE_RF is the enable for the HFA3683 synthesizer.

Data is provided on SYNTHDATA and clock on SYNTHCLK. The data is updated the falling edge of SYNTHCLK and expected to be latched into the synthesizer on the rising edge. The enable signal LE_RF is asserted while data is clocked out.

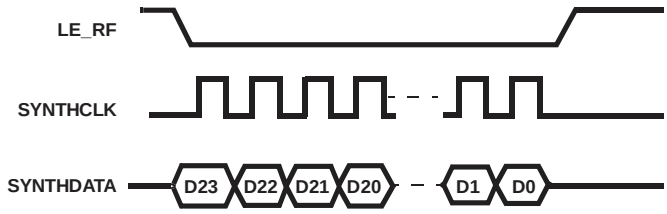


FIGURE 20. SYNTHESIZER DATA FORMAT

PHY Data Interface (MDI)

The HFA3842 has a dedicated serial port to provide the data interface to the baseband processor. This is referred to as the Modem Data Interface (MDI). The MDI operates on the data being transferred to and from the baseband on a word by word basis. There are no FIFOs needed, since the firmware is able to control the protocol in real time.

The MDI performs the following functions:

- Serial to parallel conversion of received data from the baseband, with synchronization between the incoming RX clock to the internal HFA3842 clock.
- Generating CRCs (HEC and FCS) from the received data stream to verify correct reception.
- Decrypt the received data when WEP is enabled.
- Parallel to serial conversion of transmit data, with the serial timing synchronized with the TX clock.
- Insertion of the CRCs (HEC and FCS) at the appropriate point during transmission.
- Encrypt the transmitted data when WEP is enabled.

The receive data path uses RX_RDY, RXC, RXD. The transmit data path uses TX_RDY, TXC, TXD and the CCA input to determine (under the IEEE802.11 protocol) whether to transmit.

In transmit mode, the HFA386X is used in the mode where it generates the PLCP header internally and only the MPDU is passed from HFA3842. In receive, the HFA386X is used in the mode where it passes the PLCP header and the MPDU to the HFA3842.

BBP Packet Reception

There are 4 signals associated with the BBP Receive Port: RX_PE (Receive Enable), MDRDY (Receive Ready), RXD (Receive Data), and RXCLK (Receive Clock). These connect to the HFA3842 on pins PL1, PK5, RXD, and RXC, respectively.

The receive demodulator in the BBP is activated via RX_PE. When RX_PE goes active the demodulator scrutinizes I and Q for packet activity. When a packet arrives at a valid signal level the demodulator acquires and tracks the incoming signal. It then sifts through the demodulator data for the Start Frame Delimiter (SFD). Normally, MDRDY is programmed to go active after SFD is detected. This signals the HFA3842, allowing it to pick off the needed header fields from the real-time demodulated bitstream rather than having to read these fields through the BBP Control Port.

Assuming all is well with the header, the BBP decodes the signal field in the header and switches to the appropriate data rate. If the signal field is not recognized, or the CRC16 is in error, then MDRDY will go inactive shortly after CRC16 and the demodulator will return to acquisition mode looking for another packet. If all is well with the header, and after the demodulator has switched to the appropriate data rate, then the demodulator will continue to provide data to the HFA3842 indefinitely.

Receive Port exchange details are depicted in Figure 21. Detailed timing is related in Figure 22 and Table 8.

For more detailed information concerning BBP packet reception see the HFA386x data sheets.

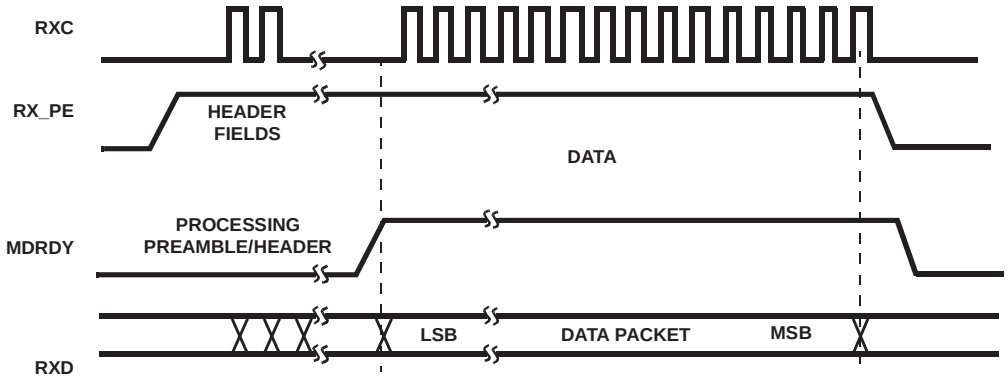


FIGURE 21. BBP RECEIVE PORT TIMING

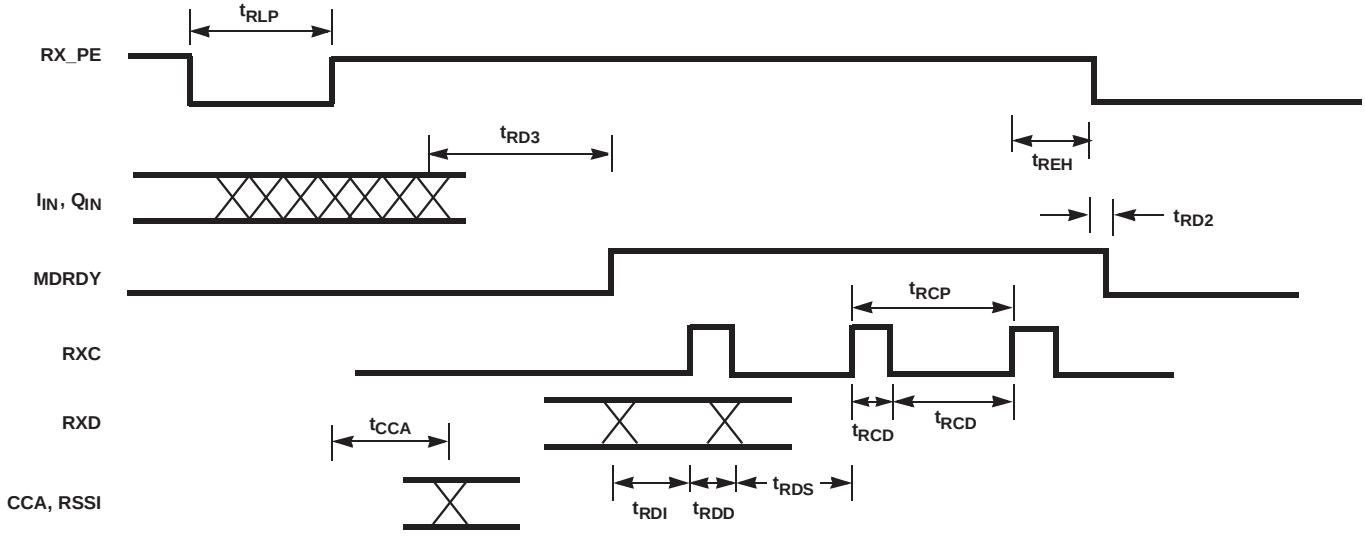


FIGURE 22. BBP RECEIVE PORT SIGNAL TIMING

NOTE: RXD, MDRDY is output two MCLK after RXC rising to provide hold time. RSSI output on TEST (5:0).

TABLE 8. BBP RECEIVE PORT AC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
RX_PE Inactive Width	t_{RLP}	70	-	ns (Note 11)
RXC Period (11MBps Mode)	t_{RCP}	77	-	ns
RXC Width Hi or Low (11MBps Mode)	t_{RCD}	31	-	ns
RXC to RXD	t_{RDD}	20	60	ns
MD_RDY to 1st RXC	t_{RD1}	940	-	ns (Note 12)
RXD to 1st RXC	$t_{RD!}$	940	-	ns
Setup RXD to RXC	t_{RDS}	31	-	ns
RXC to RX_PE Inactive (1MBps)	t_{REH}	0	925	ns (Note 13)
RXC to RX_PE Inactive (2MBps)	t_{REH}	0	380	ns (Note 13)
RXC to RX_PE Inactive (5.5MBps)	t_{REH}	0	140	ns (Note 13)
RXC to RX_PE Inactive (11MBps)	t_{REH}	0	50	ns (Note 13)
RX_PE inactive to MD_RDY Inactive	t_{RD2}	5	30	ns (Note 14)
Last Chip of SFD in to MD_RDY Active	t_{RD3}	2.77	2.86	µs (Note 12)
RX Delay		2.77	2.86	µs (Note 15)
RX_PE to CCA Valid	t_{CCA}	-	10	µs (Note 16)
RX_PE to RSSI Valid	t_{CCA}	-	10	µs (Note 16)

NOTES:

12. RX_PE must be inactive at least 3 MCLKs before going active to start a new CCA or acquisition.
13. MD_RDY programmed to go active after SFD detect (measured from I_{IN}, Q_{IN}).
14. RX_PE active to inactive delay to prevent next RXC.
15. Assumes RX_PE inactive after last RXC.
16. MD_RDY programmed to go active at MPDU start. Measured from first chip of first MPDU symbol at I_{IN}, Q_{IN} to MD_RDY active.
17. CCA and RSSI are measured once during the first 10µs interval following RX_PE going active. RX_PE must be pulsed to initiate a new measurement. RSSI may be read via serial port or from Test Bus.

BBP Packet Transmission

There are 4 signals associated with the BBP Transmit Port: TX_PE (Transmit Enable), TXRDY (Transmit Ready), TXD (Transmit Data), and TXCLK (Transmit Clock). These connect to the HFA3842 on PL0, PL7, TXD, and TXC, respectively.

State machines within the BBP control packet transmission and reception. In the case of a transmission, the MAC signals the BBP with the signal TX_PE. The BBP forms the preamble and header and then signals the MAC to begin transferring data with the signal TXRDY. This sequence is illustrated in Figure 22 with detailed signal timing shown in Figure 23 and specified delays contained in Table 9. Note that if the MAC deactivates TX_PE too early it may cut off modulation of the final symbol. For this reason, when TX_PE is de-asserted the BBP will hold TXRDY active until the last symbol containing data is modulated. This is important for power sequencing and is discussed in more detail in that section.

For more detailed information concerning BBP packet transmission see the HFA3861 data sheet.

TABLE 9. BBP TRANSMIT PORT AC ELECTRICAL SPECIFICATIONS

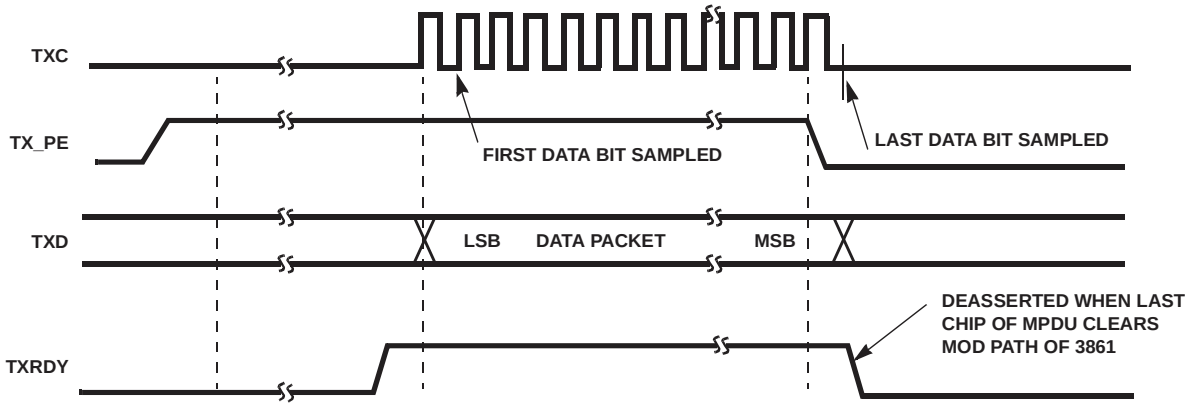
PARAMETER	SYMBOL	MIN	MAX	UNITS
TX_PE to I_{OUT}/Q_{OUT} (1st Valid Chip)	t_{D1}	2.18	2.3	µs (Note 17)
TX_PE Inactive Width	t_{TLP}	2.22	-	µs (Note 18)
TXC Width Hi or Low	t_{TCD}	40	-	ns
TXRDY Active to 1st TX_CLK Hi	t_{RC}	260	-	ns
Setup TXD to TXC Hi	t_{TDS}	30	-	ns
Hold TXD to TXC Hi	t_{TDH}	0	-	ns
TXC to TX_PE Inactive (1MBps)	t_{PEH}	0	965	ns (Note 20)
TXC to TX_PE Inactive (2MBps)	t_{PEH}	0	420	ns (Note 20)
TXC to TX_PE Inactive (5.5MBps)	t_{PEH}	0	160	ns (Note 20)
TXC to TX_PE Inactive (11MBps)	t_{PEH}	0	65	ns (Note 20)

TABLE 9. BBP TRANSMIT PORT AC ELECTRICAL SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
TXRDY Inactive To Last Chip of MPDU Out	t_{RI}	-20	20	ns
TXD Modulation Extension	t_{ME}	2	-	µs (Note 19)

NOTES:

18. I_{OUT}/Q_{OUT} are modulated before first valid chip of preamble is output to provide ramp up time for RF/IF circuits.
19. TX_PE must be inactive before going active to generate a new packet.
20. I_{OUT}/Q_{OUT} are modulated after last chip of valid data to provide ramp down time for RF/IF circuits.
21. Delay from TXC to inactive edge of TXPE to prevent next TXC. Because TXPE asynchronously stops TXC, TXPE going inactive within 40ns of TXC will cause TXC minimum hi time to be less than 40ns.



NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge of TXC.

FIGURE 23. BBP TRANSMIT PORT TIMING

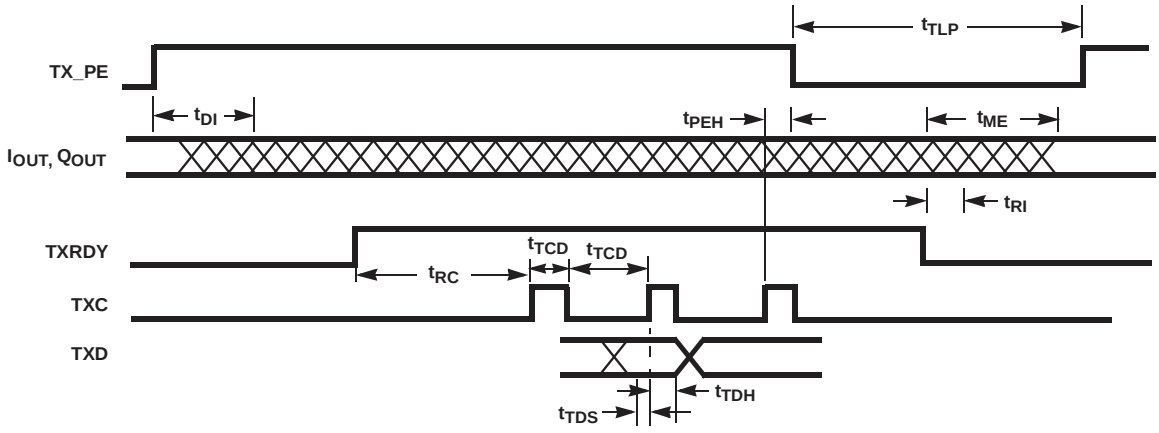


FIGURE 24. BBP TRANSMIT PORT SIGNAL TIMING

Power Sequencing

The HFA3842 provides a number of firmware controlled port pins that are used for controlling the power sequencing and other functions in the front end components of the PHY.

Packet transmission requires precise control of the radio. Ideally, energy at the antenna ceases after the last symbol of information has been transmitted. Additionally, the transmit/receive switch must be controlled properly to protect the receiver. It's also important to apply appropriate modulation to the PA while it's active.

Signaling sequences for the beginning and end of normal transmissions are illustrated in Figure 25. Table 10 lists applicable delays.

A transmission begins with PE2 as shown in Figure 25. Next, the transmit/receive switch is configured for transmission via the differential pair TR_SW and TR_SW_BAR. This is followed by TX_PE which activates the transmit state machine in the BBP. Lastly, PA_PE activates the PA. Delays for these signals related to the initiation of transmission are referenced to PE2.

Immediately after the final data bit has been clocked out of the HFA3842, TX_PE is de-asserted. The HFA3842 then waits for TXRDY to go inactive, signaling that the BBP has modulated the final information-rich symbol. It then immediately de-asserts PA_PE followed by placing the transmit/receive switch in the receive position and ending with PE2 going high. Delays for these signals related to the termination of transmission are referenced to the rising edge of PE2.

TABLE 10. TRANSMIT CONTROL TIMING SPECIFICATIONS

PARAMETER	SYMBOL	DELAY	TOLERANCE	UNITS
PE2 to TR Switch	t_{D1}	2	±0.1	µs
PE2 to PA_PE	t_{D3}	3	±0.1	µs
PA_PE to PE2	t_{D4}	3	±0.1	µs
TR Switch to PE2	t_{D5}	2	±0.1	µs

PE1 and PE2 encoding details are found in Table 11.

Note that during normal receive and transmit operation that PE1 is static and PE2 toggles for receive and transmit

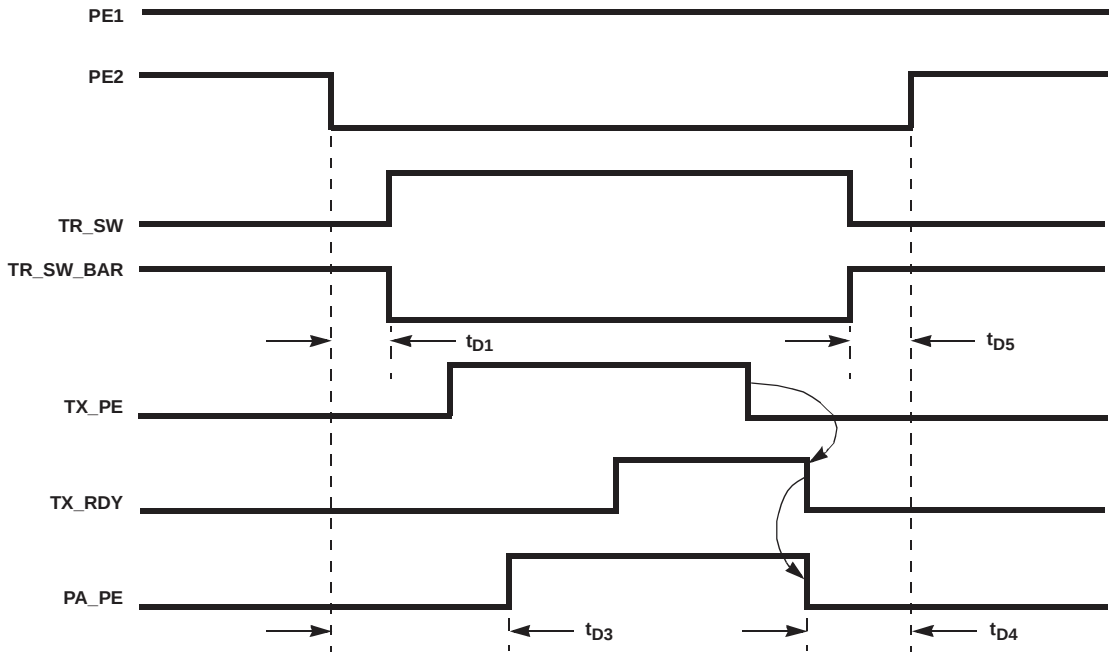


FIGURE 25. TRANSMIT CONTROL SIGNAL SEQUENCING

TABLE 11. POWER ENABLE STATES

	PE1	PE2	PLL_PE
Power Down State	0	0	1
Receive State	1	1	1
Transmit State	1	0	1
PLL Active State	0	1	1
PLL Disable State	X	X	0

TABLE 11. POWER ENABLE STATES

	PE1	PE2	PLL_PE

NOTE:

22. PLL_PE is controlled via the serial interface, and can be used to disable the internal synthesizer, the actual synthesizer control is an AND function of PLL_PE, and a result of the OR function of PE1 and PE2. PE1 and PE2 will directly control the power enable functionality of the LO buffer(s)/phase shifter.

Master Clock

Prescaler

The HFA3842 contains a clock prescaler to provide flexibility in the choice of clock input frequencies. For 11Mb/s operation, the internal master clock, MCLK, must be between 11MHz and 16MHz. The clock generator itself requires an input from the prescaler that is twice the desired MCLK frequency. Thus the lowest oscillator frequency that can be used for an 11MHz MCLK is 22MHz. The prescaler can divide by integers and 1/2 steps (IE 1, 1.5, 2, 2.5). Another way to look at it is that the divisor ratio between the external clock source and the internal MCLK may be integers between 2 and 14.

Typically, the 44MHz baseband clock is used as the input, and the prescaler is set to divide by 2. Another useful configuration is to set the prescaler to divide by 1.5 (resulting in 44MHz ÷3) for an MCLK of 14.67MHz. Contact the factory for further details on setting the clock prescaler register in the HFA3842.

Low-Frequency Crystal

The HFA3841 has an on-chip high-frequency oscillator that can be used to generate the internal master clock (MCLK). However, this on-chip high-frequency oscillator is almost never used because the MAC controller can accept the same clock signal as the PHY baseband processor (typically 44MHz), thereby avoiding the need for a separate, MAC-specific oscillator in close proximity to the PHY RF circuitry. Therefore, on the HFA3842 the high-frequency oscillator is replaced by a low-frequency oscillator. This low-frequency oscillator is intended for use with a 32.768KHz, tuning-fork type watch crystal to permit accurate timekeeping with very low power consumption during sleep state.

For the HFA3842 to achieve footprint compatibility with the HFA3841, pin 40 (OSCIN on the HFA3841) becomes CLKIN, which is the same function, when an external clock is provided to the MAC controller (as is recommended when using the HFA3842 with PRISM radios). The low-frequency crystal attaches between pin 39 (which is a 3.3V power input for the high-frequency oscillator on the HFA3841) and pin 41 (which is XTALO on the HFA3841, hence, unconnected if the on-chip oscillator is not being used). Refer to Figure 26 for additional details.

If a 32.768KHz crystal is connected, the resulting LF clock is supplied to an interval timer to permit measuring sleep intervals as well as providing a programmable wake-up time. In addition, the CHOICE-W clock generator can operate either from CLKIN or (very slowly) from the LF clock. Glitch-free switching between these two clock sources, under firmware control, is provided by two, non-architectural Strobe functions (“FAST” and “SLOW”). In addition, during hardware reset, the clock generator source is set to the LF clock if no edges are detected on CLKIN for two cycles of the LF clock (roughly 61 microseconds). This allows proper initialization with omission of either clock source, since without the LF crystal attached there will not be cycles of the LF clock to activate the detection circuit. The ability to initialize the HFA3842 using the LF oscillator to generate MCLK allows the high-frequency (PHY) oscillator to be powered down during sleep state, which is not possible with the HFA3841. If this is done, firmware can turn on power to the PHY oscillator upon wakeup, and use the interval timer to measure the startup and stabilization period before switching to use CLKIN.

Clock Generator

The HFA3842 can operate with MCLK frequencies up to at least 25MHz and CLKIN frequencies of at least 50MHz. The MCLK prescaler generates MCLK (and QCLK) from the external clock provided at the CLKIN input, or from the output of the LF oscillator. The MCLK prescaler divides the selected input clock by any integer value between 2 and 16, inclusive.

- When using a 44MHz CLKIN, as is typical for 802.11 or 802.11b controllers with a PC Card Host Interface, common divisors are 3 (14.67MHz), 4 (11MHz), or 5 (8.8MHz)
- It is anticipated that a controller for the 802.11a, mandatory data rates will need to operate at an MCLK frequency of a least 24MHz, hence a CLKIN frequency of at least 48MHz.

The MCLK prescaler is set to divide by 16 at hardware reset to allow initialization firmware to be executed from slow memory devices at any CLKIN frequency. The MCLK prescaler generates glitch free output when the divisor is changed. This allows firmware to change the MCLK frequency during operation, which is especially useful to selectively reduce operating speed, thereby conserving power, when full speed processing is not required.

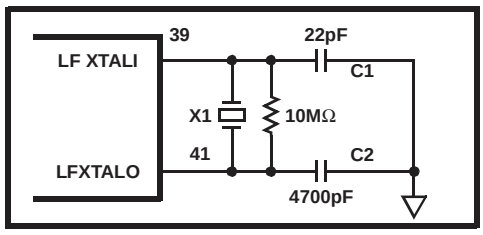


FIGURE 26. 32.768kHz CRYSTAL

Power On Reset Configuration

The HFA3842 supports both hardware and software reset functions. Hardware reset is caused by assertion of the RESET input. When using the PC Card host interface, software reset is caused by setting the Sreset bit in the Configuration Option Register (COR[71]. Hardware and software reset leave the HFA3842 in the same state except in the case of soft reset from the PC Card Host Interface, in which case the COR and HCR registers come into play.

The MD[15:8] pin values are sampled during HRESET or SRESET. These pins have internal 50K pull-down resistors. External pull-up resistors (typically 10kΩ) are used for bits that should be read as high at reset.

Table 12 summarizes the effect per pin. Table 13 provides the MD15 and MD14 bit values required by the HFA3842 to allow usage of Serial EEPROM Devices.

TABLE 12. INITIALIZATION STRAPPING OPTIONS ON MBUS DATA PINS

BITS	NAME	DEFAULT	FUNCTION
15:14	NVtype[1:01]	0	Indicates type of serial NV memory to be read by initialization firmware in on-chip ROM.
I 2	4wire	1	Use 4-wire interface to SRAM (CS-, OE-, WEH-, WEL-) as appropriate when using x8 SRAMs. When 0 = selects 5-wire interface for use with x16 SRAM (CS-, OE-, WE-, UBE-, LBE-).
11	Strldle	0	Start Idle. If ROMds = 0, then the “hardware” ignores this bit, but it is examined by the ICSROM boot code which will halt after loading the serial NV. If ROMds = 1, then setting this bit will cause the processor to wait for download of data From the AuxPort.
10	Mem16	0	RAM and NV space at startup is 516. When = 0 RAM and NV space at startup is x8. IF starting from off-chip NV memory this setting must indicate the width of the startup Flash EPROM. During initialization, firmware can set separate widths for RAM and NV space in the Memory Control Register.
9	NVds	0	Disable mapping of off-chip control store to NV, space hence map off-chip control store to RAM space). When = 0 off-chip control store is mapped to NV memory. This bit is used only to set initial values in the MOR and CSCR registers. It controls the setting of the NVRE and MAPxx bits therein.
8	ROMds	1	Disable on-chip ICSROM (Internal Control Store ROM - bootstrap code). When = 0 enable on-chip ICS-ROM.
7	ISA Mode	0	Set host interface control signals and address decoding For PC Card. When = 1 set host interface signals and address decoding is for ISA bus, with all registers in I/O space and Attribute space disabled. To use ISA mode, PHIenable must be = I to enable a Parallel Host Interface.
6	FCRinIO	0	Enable I/O space decoding for the physical FCRs. When = 1, the COR. CSR, and PRR registers (see Section 4.3) are accessible at I/O space offsets 0 x 40, 0 x 42, and 0 x 44 respectively. When = 0 these registers are only accessible in Attribute space. This bit is ignored when PHIenable = 0, and is overridden (forced = 1) when ISA mode = 1. FCRinIO = 1 is useful For PC Card operation PHIenable = 1 ISA mode = 0 to allow non OS software to access the COR/HCR in OS environments where the system software does not permit application software to access Attribute space.[a]
5:0	Spare	00	Not assigned.

TABLE 13. SERIAL EEPROM SELECTION

MD15	MD14	DEVICE TYPE	FUNCTION
0	0	AT45DB011	Large Serial Device used to transfer firmware to SRAM
0	1	24C08 (Note)	Small Serial Device which contains only CIS. MAC goes idle after loading CIS and waits for host.
1	X	None	Modes not supported in firmware at this time. Consult factory for additional device types added.

NOTE: The operating frequency of the serial port is 400kHz with a voltage of 3.3V.

References

For Intersil documents available on the internet, see web site www.intersil.com/

[1] IEEE Std 802.11-1999 Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification.

[2] *HFA3860B Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, FN4594.

[3] *HFA3861 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, FN4699.

[4] *HFA3783 Data Sheet*, Quad IF, Intersil Corporation, FN4633.

[5] *HFA3683 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, FN4634.

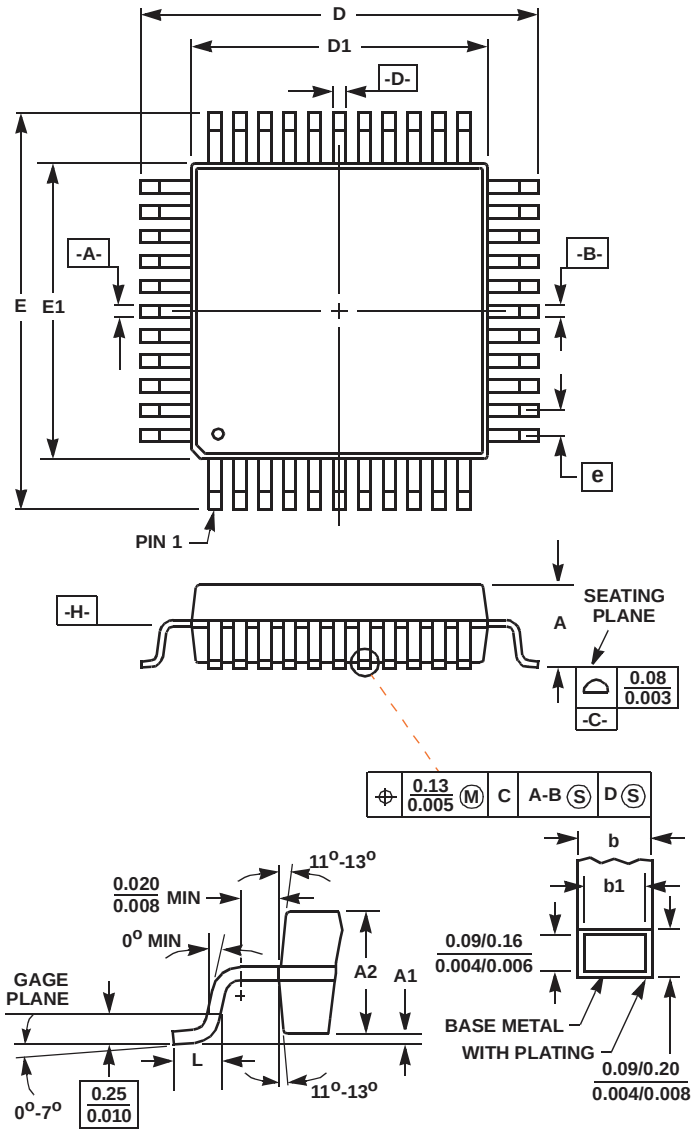
[6] PC Card Standard 1996, PCMCIA/JEIDA.

[7] *AN9874 Application Note*, Intersil Corporation, “ISA Plug and Play with the HFA3841”.

[8] *AN9844 Application Note,* Intersil Corporation, “HFA3842 to PRISM II MAC-less Connections”, AN9844.

[9] *AN9893 Application Note,* Intersil Corporation, AN9893 “Using the HFA3842 WLAN MAC Evaluation Board”.

Thin Plastic Quad Flatpack Packages (LQFP)



Q128.14x20 (JEDEC MS-026BHB ISSUE C)
128 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.862	0.870	21.90	22.10	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.626	0.634	15.90	16.10	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	128		128		7
e	0.0197 BSC		0.50 BSC		-

Rev. 0 7/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

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