VG025

High Linearity Variable Gain Amplifier

The Communications Edge ™

Product Information

Product Features

- Tunable within 50 – 2200 MHz
- 21 dB Attenuation Range
- Constant +40 dBm OIP3 and +21 dBm P1dB over all gain settings
- Single +5V Supply Voltage
- 16-pin 4x4mm lead-free/green/ RoHS-compliant QFN Package
- MTTF > 1000 years

Applications

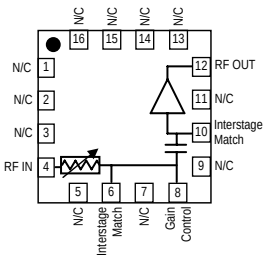
- AGC circuitry
- Temperature compensation circuits
- DCS/PCS, cdma2000™, W-CDMA

Product Description

The VG025 is a high dynamic range variable gain amplifier (VGA) capable of achieving an analog attenuation range of up to 21 dB. The +21 dBm output compression point and +40 dBm output intercept point of the amplifier are maintained over the entire attenuation range, making the VG025 ideal for use in temperature compensation circuits or AGC loops.

The VG025 is available in a lead-free/green/RoHS-compliant 16-pin 4x4mm QFN surface-mount package with an exposed backside paddle to allow an MTTF rating of over 1000 years at a mounting temperature of +85º C. All devices are 100% RF & DC tested and packaged on tape and reel for automated surface-mount assembly.

Functional Diagram



Function	Pin Number
RF Input	4
Gain Control	8
Interstage Match	6, 10
RF Output / DC bias	12
No Connect or GND	All other pins
Ground	Backside slug

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	50		2200
Test Frequency	MHz		800	
Gain (2)	dB	13.5	15	
Input Return Loss (2)	dB		6.3	
Output Return Loss (2)	dB		7.6	
Output P1dB	dBm		21.3	
Output IP3 (3)	dBm	37	39	
Noise Figure (2)	dB		5.3	
Gain Variation Range (4)	dB	16	21	24
Gain Variation Control Voltage (5)	V	0		4.5
Supply Voltage	V		5	
Operating Current Range	mA	120	150	180
Gain Control Pin Current	mA		26	28

1. Test conditions unless otherwise noted: 25ºC, Vsupply = +5 V, in tuned application circuit. Vctrl is the control voltage through the 120 Ω dropping resistor as shown in the application circuit on page 2.
2. Specifications refer to the device at the maximum gain setting (Vctrl=0V). The input and output return loss will be dramatically improved with an attenuation setting greater than 1 dB.
3. 3OIP measured with two tones at an output power of +5 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
4. The gain variation range is measured as the difference in gain with Vctrl = 0 and 4.5V at 800 MHz.
5. This voltage refers to the V_{CTRL} as shown in the circuit schematic on page 2. There should be a series resistance of 120Ω between the control voltage and pin 8 for proper operation.

Typical Performance (1)

Parameter	Units	Typical			
Frequency	MHz	240	800	1960	2140
Gain (2)	dB	15.4	15	8.4	8.4
Input Return Loss (2)	dB	11	6.3	12	11
Output Return Loss (2)	dB	11	7.6	6.5	5.6
Output P1dB	dBm	21.8	21.3	22	22
Output IP3 (3)	dBm	42	39	40	40
Noise Figure (2)	dB	4.5	5.3	8.1	8.2
Gain Variation Range	dB	20	21	14	13

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
Amplifier Supply Voltage (pin 12)	+6 V
Pin 8 (Gain Control) Current	30 mA
RF Input Power (continuous)	4 dB above Input P1dB
Junction Temperature	+220 °C

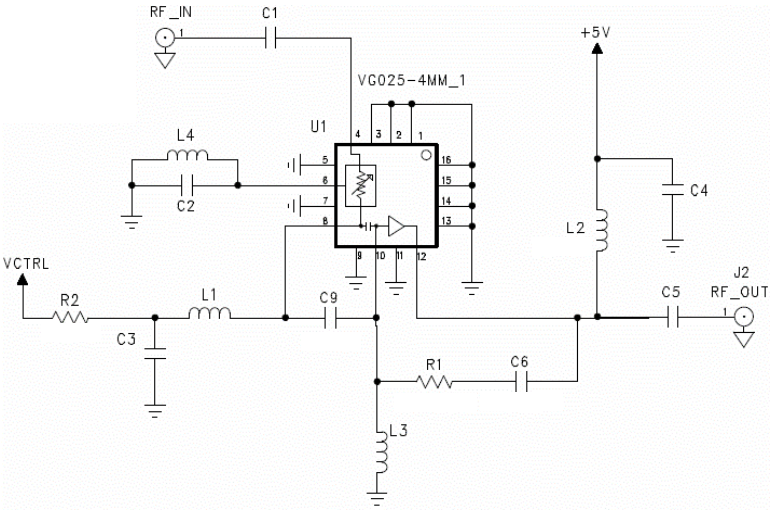
Operation of this device above any of these parameters may cause permanent damage.

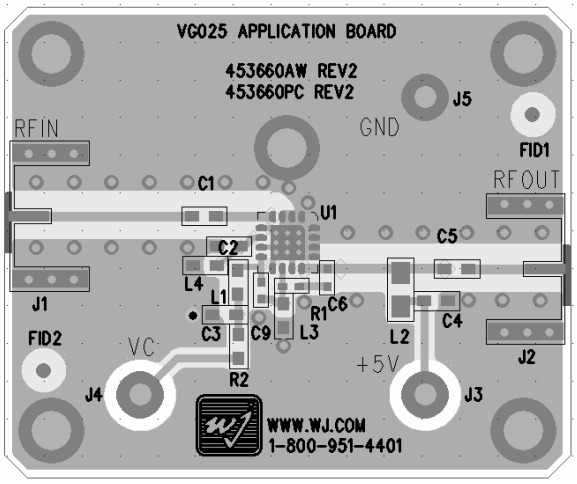
Ordering Information

Part No.	Description
VG025-G	High Linearity Variable Gain Amplifier (lead-free/green/RoHS-compliant 4x4mm QFN package)
VG025-PCB240	240 MHz Evaluation Board
VG025-PCB800	800 MHz Evaluation Board
VG025-PCB2000	1.7 – 2.2 GHz Evaluation Board

Specifications and information are subject to change without notice

Application Circuit Configurations





Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

The WJ VG025 variable gain amplifier can operate over a very broad range of frequencies (50 - 2200MHz), but needs specific matching circuits for specific bands of interest. At the maximum gain state, reasonable matching is only available for about ±10% of the reference frequency. The amplifier operates with a typical current of 150 mA at +5 V while the attenuator current can be varied from 0 to 30 mA, while maintaining constant OIP3 and P1dB. The RF matching of the VG025 for the entire frequency range can be accomplished with the systematic adjustment of only a few parts. The RF matching is not influenced by different attenuator drive methods provided there is adequate decoupling of the attenuator bias. This reference application circuit uses voltage applied between 0 and 4.5V onto the Vctrl as shown on the schematic above. The R2 is a current limiting resistor to help linearize the drive of the attenuator and give better attenuator current control.

To properly design the VG025 for an application, pick the frequency of interest. Choose blocking capacitor values which give RF impedance of less than 3 ohms. Choose the RF chokes for the largest inductance while still having resonant frequency about 30% greater than the Reference frequency (this allows for good isolation and inductor variation). Next choose L3 and C9 for interstage matching. C9 is only needed for lower frequencies and determines the low frequency roll off of the gain. L3 will have dominant control over the input and output return losses at maximum gain state (0 mA gain control pin current). C2 is needed to resonate the package parasitics to achieve the maximum attenuation values with attenuator current. With attenuator control pin current of 26 mA, C2 can be chosen to provide maximum attenuation. See the chart below for suggested component values and predicted performance at various reference frequencies. Component values can be interpolated for reference frequencies not listed.

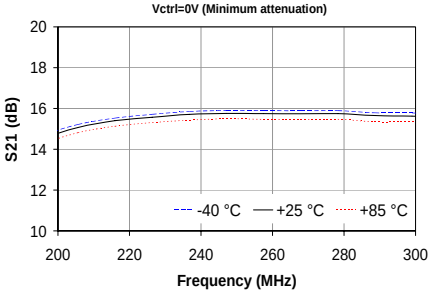
For lower frequencies the lumped element values can be used and the layout with unplaced component pads does not greatly affect the RF performance of the circuit. For frequencies greater than 500 MHz, component size and trace length have more influence on circuit performance. Smaller components and shorter trace lengths reduce the affects of the external component parasitics and interaction with the multichip module parasitics.

Reference Frequency	MHz	240	800	1850	1960	2140
C1, C5	pF	1000	56	56	56	56
C2	pF	0 Ω	27	3.6	3.6	3.6
C3, C4	µF	.01	.01	.01	.01	.01
C6	pF	DNP	DNP	DNP	DNP	DNP
C9	pF	1.2	DNP	DNP	DNP	DNP
L1, L2	nH	220	22	12	12	12
L3	nH	47	8.2	DNP	DNP	DNP
L4	nH	DNP	82	33	33	33
R1	Ω	DNP	DNP	DNP	DNP	DNP
R2	Ω	120	120	120	120	120
Attenuation Range	dB	20	21	12	14	13
Maximum Gain	dB	15.4	15	8.6	8.4	8.4
Input Return Loss	dB	11	6.3	11	12	11
Output Return Loss	dB	11	7.6	7.7	6.5	5.6
Output P1dB	dBm	21.8	21.3	22	22	22
Output IP3	dBm	42	39	40	40	40
Noise Figure	dB	4.5	5.3	7.9	8.1	8.2

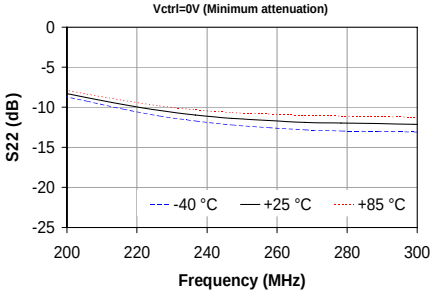
DNP = Do Not Place (Component is not used in the design)

240 MHz Circuit Performance (VG025-PCB240)

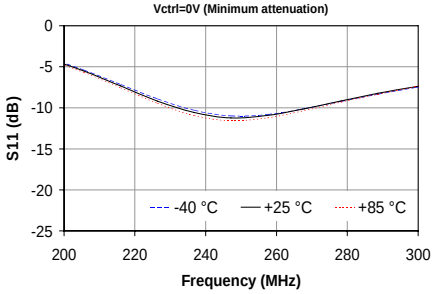
S21 vs. Frequency
Vctrl=0V (Minimum attenuation)



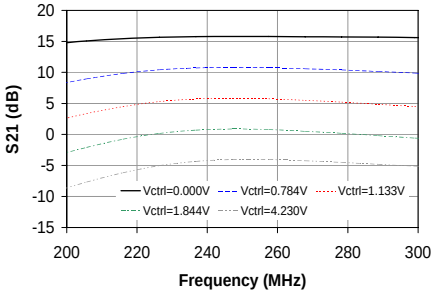
S22 vs. Frequency
Vctrl=0V (Minimum attenuation)



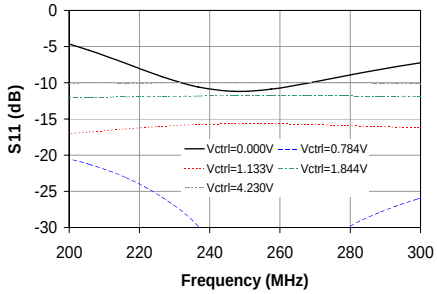
S11 vs. Frequency
Vctrl=0V (Minimum attenuation)



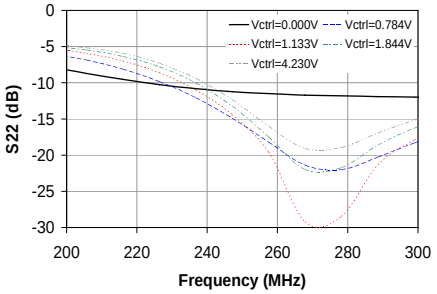
S21 vs. Frequency vs. Control Voltage



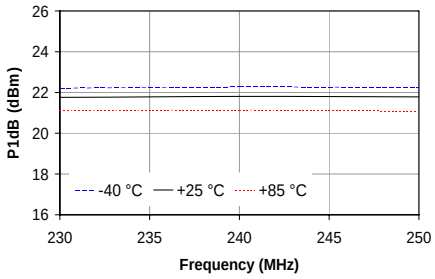
S11 vs. Frequency vs. Control Voltage



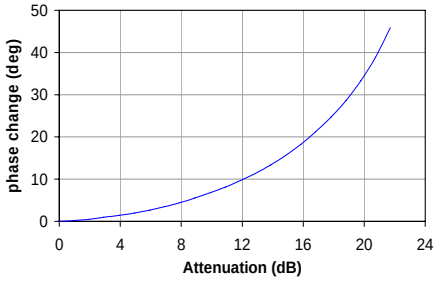
S22 vs. Frequency vs. Control Voltage



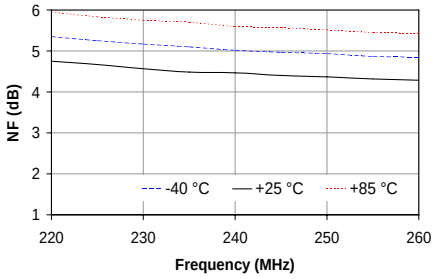
P1dB vs. Frequency
Vctrl=0V (Minimum attenuation)



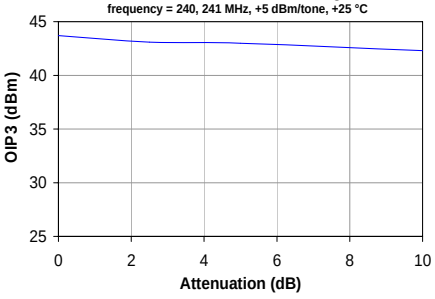
Phase change vs. Attenuation
25 °C, 240 MHz



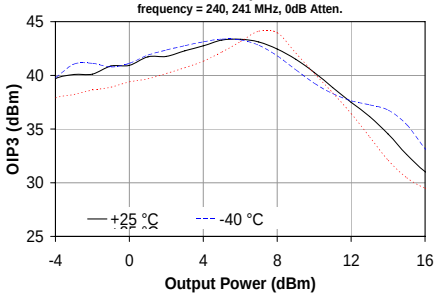
Noise Figure vs. Frequency
Vctrl=0V (Minimum attenuation)



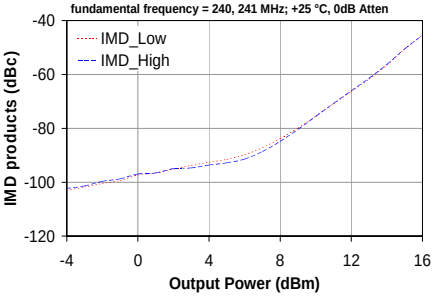
OIP3 vs. Attenuation Setting
frequency = 240, 241 MHz, +5 dBm/tone, +25 °C



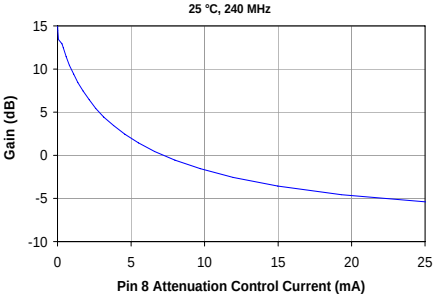
OIP3 vs. Output Power
frequency = 240, 241 MHz, 0dB Atten.



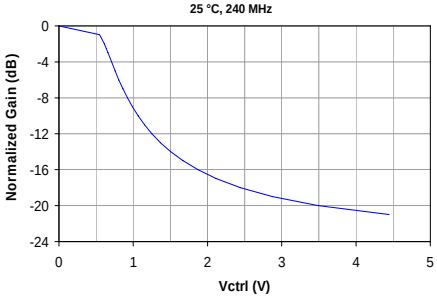
IMD products vs. Output Power
fundamental frequency = 240, 241 MHz; +25 °C, 0dB Atten



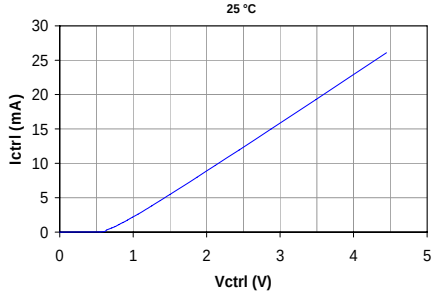
Gain vs. Pin 8 Attn. Control Current
25 °C, 240 MHz



Normalized Gain vs. Vctrl
25 °C, 240 MHz

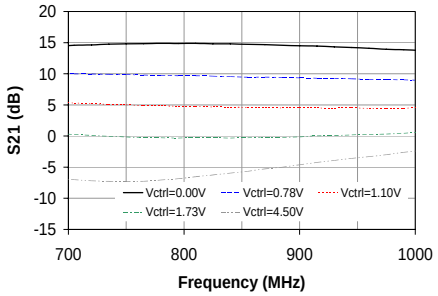


Ictrl vs. Vctrl
25 °C

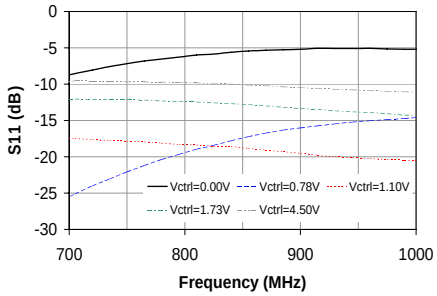


800 MHz Circuit Performance (VG025-PCB800)

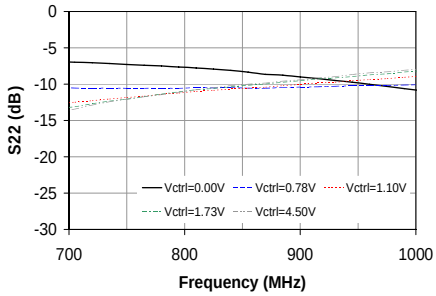
S21 vs. Frequency vs. Control Voltage



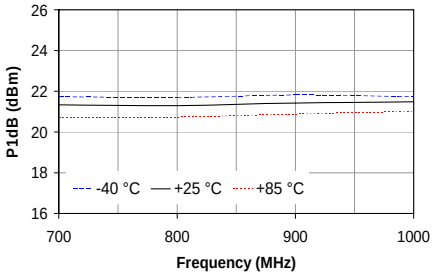
S11 vs. Frequency vs. Control Voltage



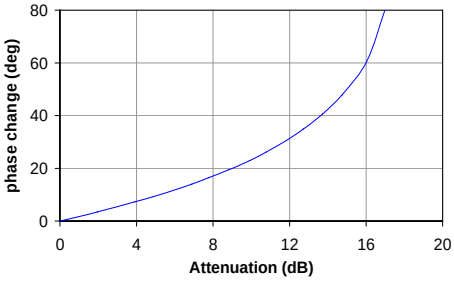
S22 vs. Frequency vs. Control Voltage



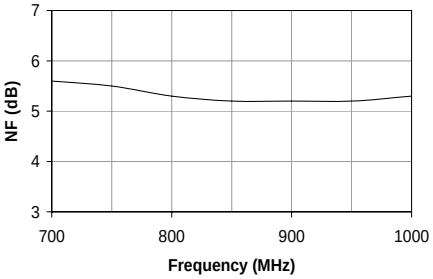
P1dB vs. Frequency
Vctrl=0V (Minimum attenuation)



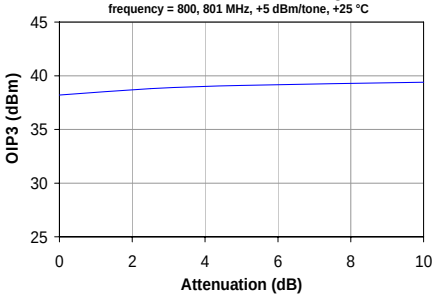
Phase change vs. Attenuation
25 °C, 800 MHz



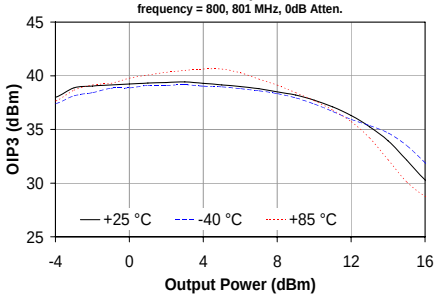
Noise Figure vs. Frequency
Vctrl=0V (Maximum Gain Setting)



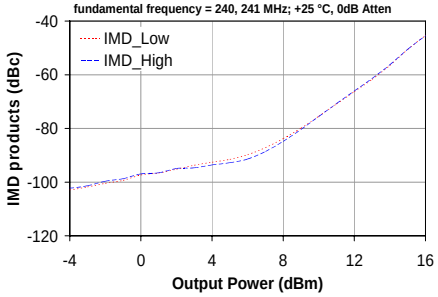
OIP3 vs. Attenuation Setting
frequency = 800, 801 MHz, +5 dBm/tone, +25 °C



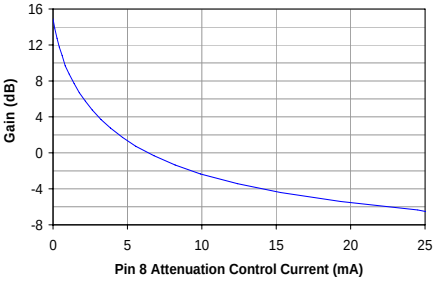
OIP3 vs. Output Power
frequency = 800, 801 MHz, 0dB Atten.



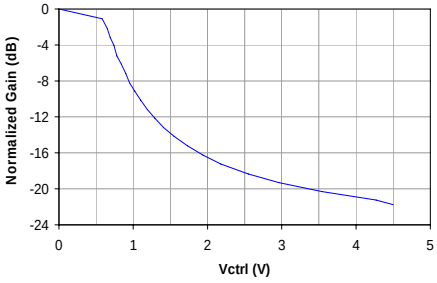
IMD products vs. Output Power
fundamental frequency = 240, 241 MHz; +25 °C, 0dB Atten



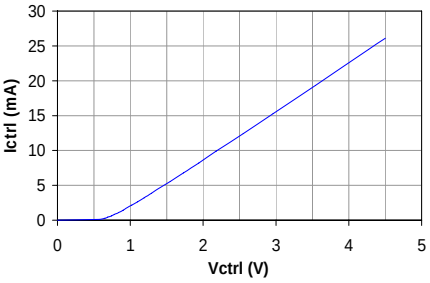
Gain vs. Pin 8 Attn. Control Current
25 °C, 800 MHz



Normalized Gain vs. Vctrl
25 °C, 800 MHz

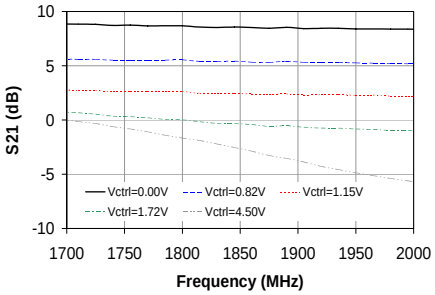


Ictrl vs. Vctrl
25 °C

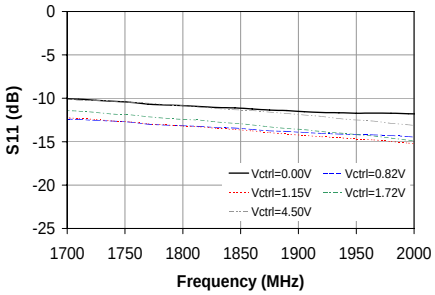


1960 MHz Circuit Performance (VG025-PCB2000)

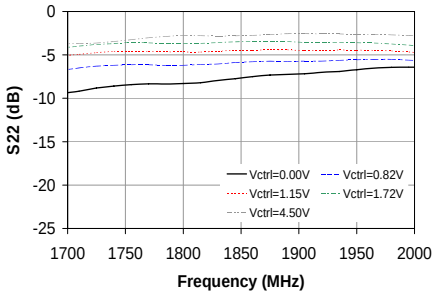
S21 vs. Frequency vs. Control Voltage



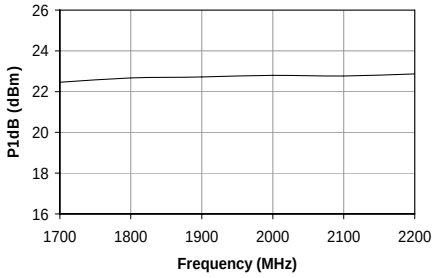
S11 vs. Frequency vs. Control Voltage



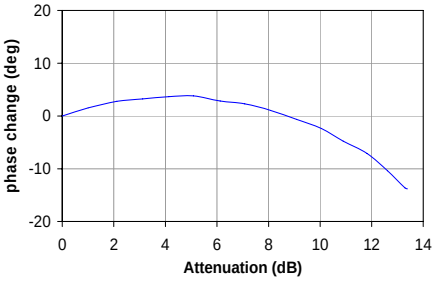
S22 vs. Frequency vs. Control Voltage



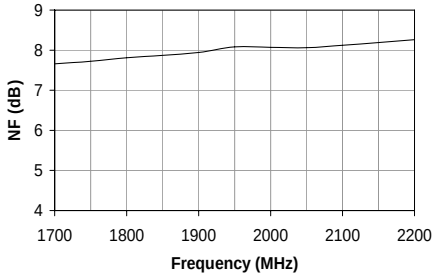
P1dB vs. Frequency
Vctrl=0V (Minimum attenuation)



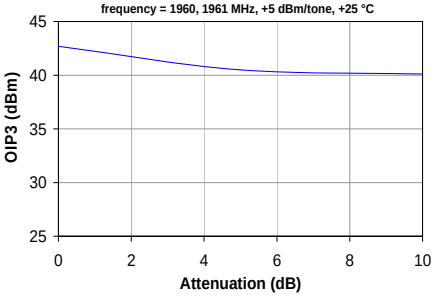
Phase change vs. Attenuation
25 °C, 1900 MHz



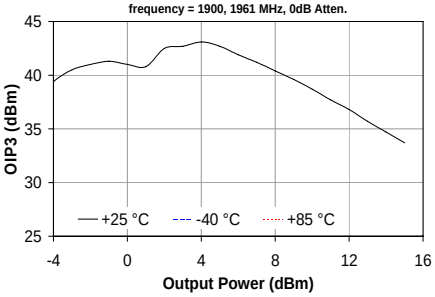
Noise Figure vs. Frequency
Vctrl=0V (Maximum Gain Setting)



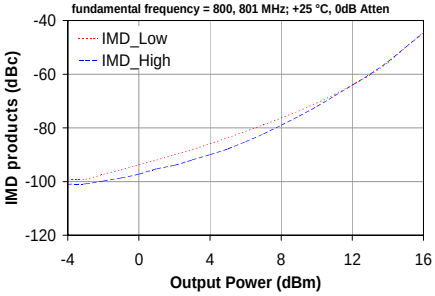
OIP3 vs. Attenuation Setting
frequency = 1960, 1961 MHz, +5 dBm/tone, +25 °C



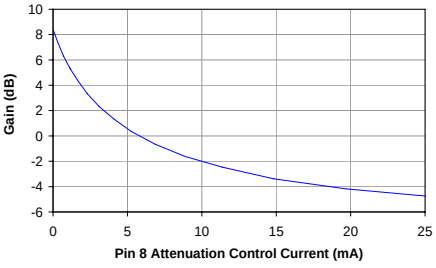
OIP3 vs. Output Power
frequency = 1900, 1961 MHz, 0dB Atten.



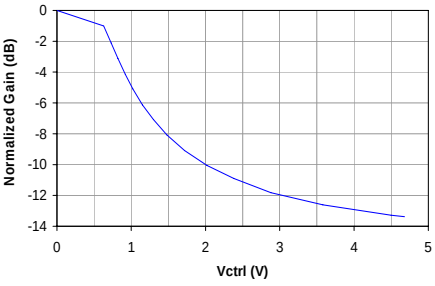
IMD products vs. Output Power
fundamental frequency = 800, 801 MHz; +25 °C, 0dB Atten



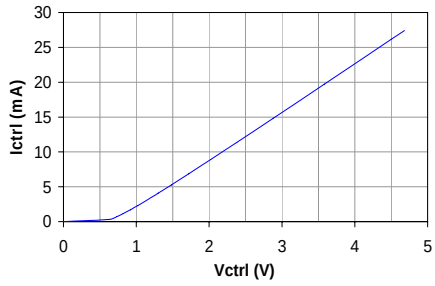
Gain vs. Pin 8 Attn. Control Current
25 °C, 1900 MHz



Normalized Gain vs. Vctrl
25 °C, 1900 MHz

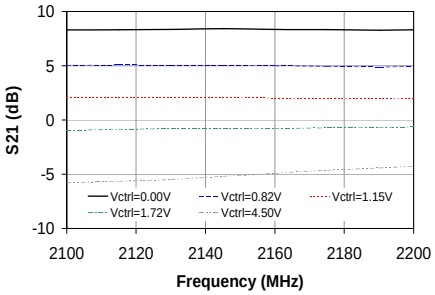


Ictrl vs. Vctrl
25 °C

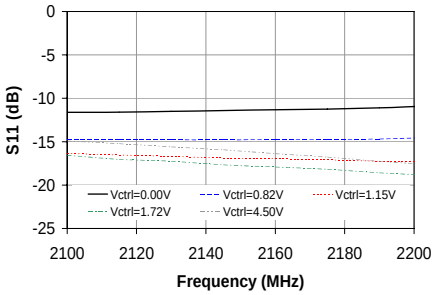


2140 MHz Circuit Performance (VG025-PCB2000)

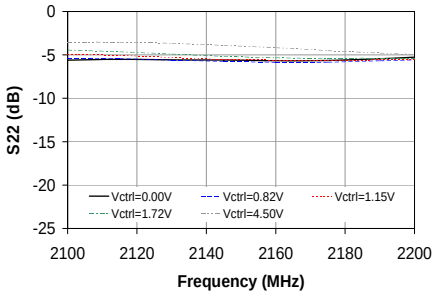
S21 vs. Frequency vs. Control Voltage



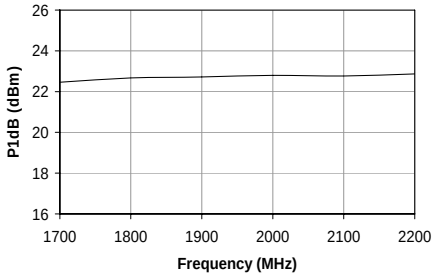
S11 vs. Frequency vs. Control Voltage



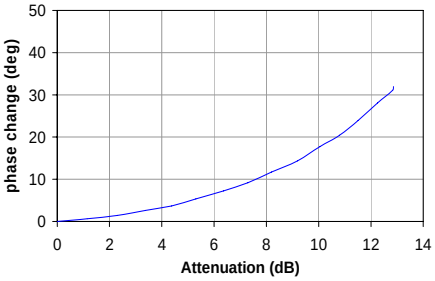
S22 vs. Frequency vs. Control Voltage



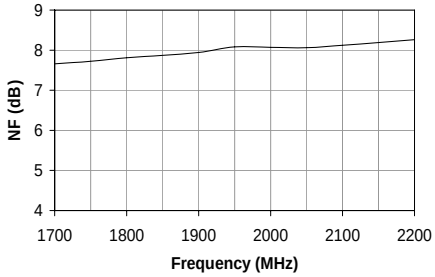
P1dB vs. Frequency
Vctrl=0V (Minimum attenuation)



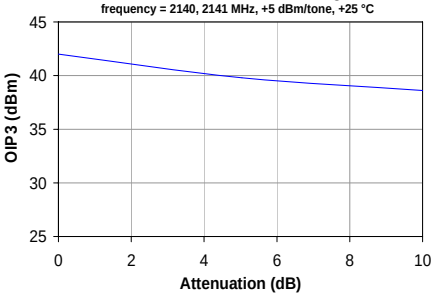
Phase change vs. Attenuation
25 °C, 2140 MHz



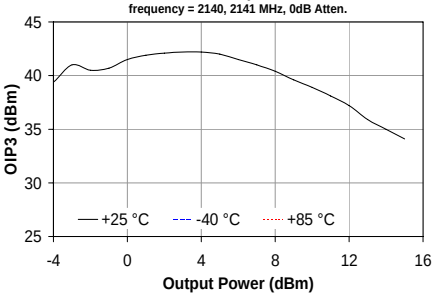
Noise Figure vs. Frequency
Vctrl=0V (Maximum Gain Setting)



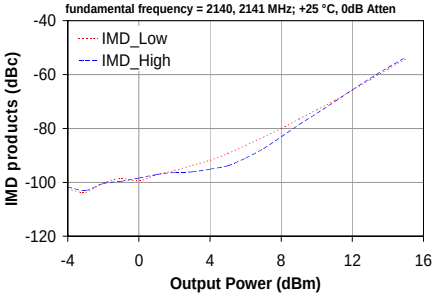
OIP3 vs. Attenuation Setting
frequency = 2140, 2141 MHz, +5 dBm/tone, +25 °C



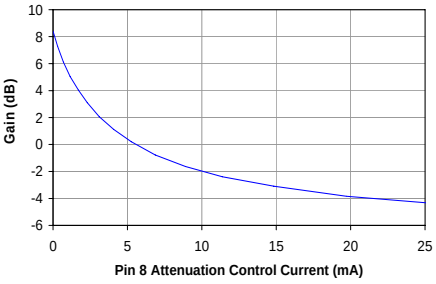
OIP3 vs. Output Power
frequency = 2140, 2141 MHz, 0dB Atten.



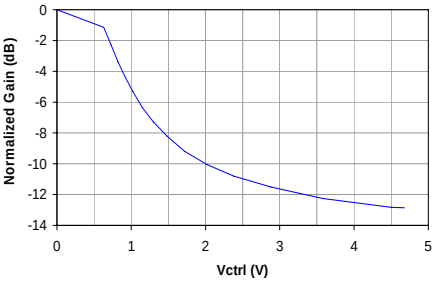
IMD products vs. Output Power
fundamental frequency = 2140, 2141 MHz; +25 °C, 0dB Atten



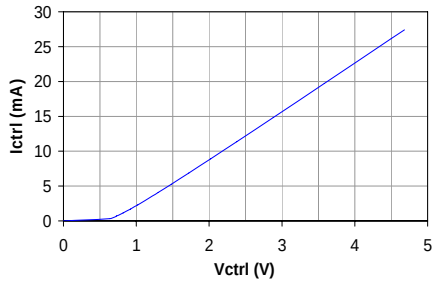
Gain vs. Pin 8 Attn. Control Current
25 °C, 2140 MHz



Normalized Gain vs. Vctrl
25 °C, 2140 MHz



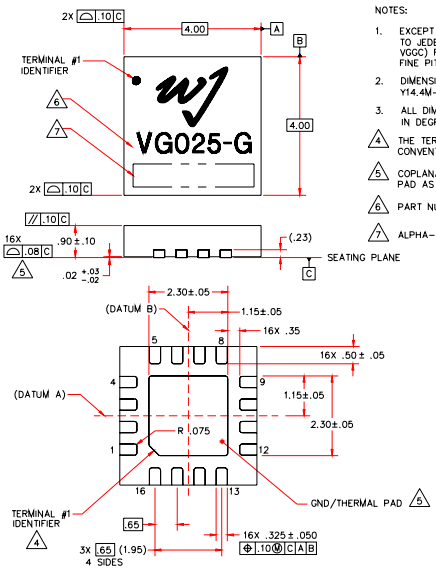
Ictrl vs. Vctrl
25 °C



VG025-G Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

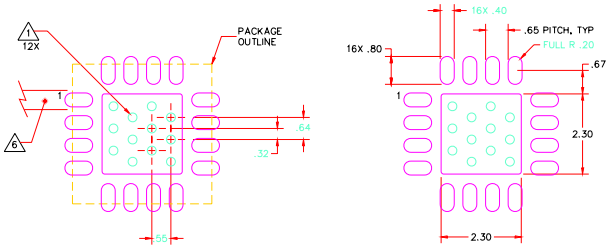
Outline Drawing

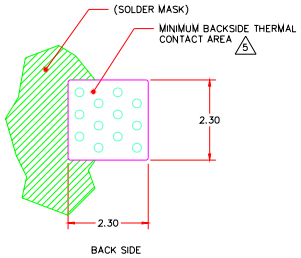


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VGGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PART NUMBER
7. ALPHA-NUMERIC LOT CODE.

Mounting Configuration / Land Pattern





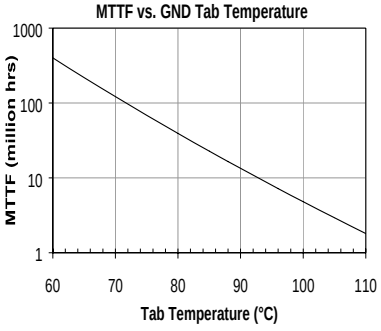
NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Thermal Resistance, Rth (1)	59 °C / W
Junction Temperature, Tjc (2)	129 °C

1. The thermal resistance is referenced from the hottest part of the junction to the backside ground copper tab.
2. This corresponds to the typical biasing condition of +5V, 150 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160° C.



Product Marking

The component will be marked with a "VG025-G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

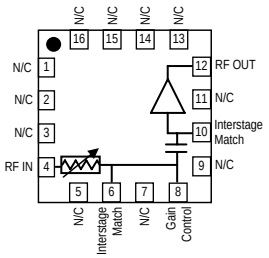
Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ⩾500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ⩾1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL: Level 2 @ 260 ˚C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout



Function	Pin No
RF Input	4
Gain Control	8
Interstage Match	6, 10
RF Output / DC bias	12
No Connect or GND	All other pins
Ground	Backside slug

Specifications and information are subject to change without notice