μPD46184095B
μPD46184185B

18M-BIT DDR II SRAM SEPARATE I/O 2-WORD BURST OPERATION

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Description

The μPD46184095B is a 2,097,152-word by 9-bit and the μPD46184185B is a 1,048,576-word by 18-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD46184095B and μPD46184185B integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and K#) are latched on the positive edge of K and K#.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin PLASTIC BGA.

Features

- 1.8 ± 0.1 V power supply
- 165-pin PLASTIC BGA (13 x 15)
- HSTL interface
- PLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports
- DDR read or write operation initiated each cycle
- Pipelined double data rate operation
- Separate data input/output bus
- Two-tick burst for low DDR transaction size
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability. Normal operation is restored in 20 μs after clock is resumed.
- User programmable impedance output (35 to 70 Ω)
- Fast clock cycle time : 3.3 ns (300 MHz), 4.0 ns (250 MHz)
- Simple control logic for easy depth expansion
- JTAG 1149.1 compatible test access port

Ordering Information

Part No.	Organization (word x bit)	Cycle time	Clock frequency	Core Supply Voltage	Operating Ambient Temperature	Package
μPD46184095BF1-E33-EQ1-A	2M x 9	3.3ns	300MHz	1.8 ± 0.1	T_A = 0 to 70°C	165-pin PLASTIC BGA (13 x 15) Lead-free
μPD46184095BF1-E40-EQ1-A		4.0ns	250MHz			
μPD46184185BF1-E33-EQ1-A	1M x 18	3.3ns	300MHz			
μPD46184185BF1-E40-EQ1-A		4.0ns	250MHz			
μPD46184095BF1-E33Y-EQ1-A	2M x 9	3.3ns	300MHz	1.8 ± 0.1	T_A = −40 to 85°C	
μPD46184095BF1-E40Y-EQ1-A		4.0ns	250MHz			
μPD46184185BF1-E33Y-EQ1-A	1M x 18	3.3ns	300MHz			
μPD46184185BF1-E40Y-EQ1-A		4.0ns	250MHz			
μPD46184095BF1-E33-EQ1	2M x 9	3.3ns	300MHz	1.8 ± 0.1	T_A = 0 to 70°C	165-pin PLASTIC BGA (13 x 15) Lead
μPD46184095BF1-E40-EQ1		4.0ns	250MHz			
μPD46184185BF1-E33-EQ1	1M x 18	3.3ns	300MHz			
μPD46184185BF1-E40-EQ1		4.0ns	250MHz			
μPD46184095BF1-E33Y-EQ1	2M x 9	3.3ns	300MHz	1.8 ± 0.1	T_A = −40 to 85°C	
μPD46184095BF1-E40Y-EQ1		4.0ns	250MHz			
μPD46184185BF1-E33Y-EQ1	1M x 18	3.3ns	300MHz			
μPD46184185BF1-E40Y-EQ1		4.0ns	250MHz			

Pin Arrangement

165-pin PLASTIC BGA (13 x 15)

(Top View)

[μPD46184095B]

2M x 9

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	V_{SS}/72M	A	R, W#	NC	K#	NC/144M	LD#	A	V_{SS}/36M	CQ
B	NC	NC	NC	A	NC/288M	K	BW0#	A	NC	NC	Q4
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DD}Q	V_{SS}	V_{SS}	V_{SS}	V_{DD}Q	NC	D3	Q3
F	NC	NC	NC	V_{DD}Q	V_{DD}	V_{SS}	V_{DD}	V_{DD}Q	NC	NC	NC
G	NC	D6	Q6	V_{DD}Q	V_{DD}	V_{SS}	V_{DD}	V_{DD}Q	NC	NC	NC
H	DLL#	V_{REF}	V_{DD}Q	V_{DD}Q	V_{DD}	V_{SS}	V_{DD}	V_{DD}Q	V_{DD}Q	V_{REF}	ZQ
J	NC	NC	NC	V_{DD}Q	V_{DD}	V_{SS}	V_{DD}	V_{DD}Q	NC	Q2	D2
K	NC	NC	NC	V_{DD}Q	V_{DD}	V_{SS}	V_{DD}	V_{DD}Q	NC	NC	NC
L	NC	Q7	D7	V_{DD}Q	V_{SS}	V_{SS}	V_{SS}	V_{DD}Q	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q8	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A	: Address inputs	TMS	: IEEE 1149.1 Test input
D0 to D8	: Data inputs	TDI	: IEEE 1149.1 Test input
Q0 to Q8	: Data outputs	TCK	: IEEE 1149.1 Clock input
LD#	: Synchronous load	TDO	: IEEE 1149.1 Test output
R, W#	: Read Write input	V_{REF}	: HSTL input reference input
BW0#	: Byte Write data select	V_{DD}	: Power Supply
K, K#	: Input clock	V_{DD}Q	: Power Supply
C, C#	: Output clock	V_{SS}	: Ground
CQ, CQ#	: Echo clock	NC	: No connection
ZQ	: Output impedance matching	NC/xxM	: Expansion address for xxMb
DLL#	: PLL disable		

Remarks 1. ×××# indicates active LOW.

2. Refer to **Package Dimensions** for the index mark.

3. 2A, 7A, 10A and 5B are expansion addresses : 10A for 36Mb
: 10A and 2A for 72Mb
: 10A, 2A and 7A for 144Mb
: 10A, 2A, 7A and 5B for 288Mb

2A and 10A of this product can also be used as NC.

Pin Arrangement

165-pin PLASTIC BGA (13 x 15)

(Top View)

[μPD46184185B]

1M x 18

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	Vss/144M	NC/36M	R, W#	BW1#	K#	NC/288M	LD#	A	Vss/72M	CQ
B	NC	Q9	D9	A	NC	K	BW0#	A	NC	NC	Q8
C	NC	NC	D10	Vss	A	A	A	Vss	NC	Q7	D8
D	NC	D11	Q10	Vss	Vss	Vss	Vss	Vss	NC	NC	D7
E	NC	NC	Q11	VDDQ	Vss	Vss	Vss	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	D5
H	DLL#	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	Vss	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q2
M	NC	NC	D16	Vss	Vss	Vss	Vss	Vss	NC	Q1	D2
N	NC	D17	Q16	Vss	A	A	A	Vss	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A	: Address inputs	TMS	: IEEE 1149.1 Test input
D0 to D17	: Data inputs	TDI	: IEEE 1149.1 Test input
Q0 to Q17	: Data outputs	TCK	: IEEE 1149.1 Clock input
LD#	: Synchronous load	TDO	: IEEE 1149.1 Test output
R, W#	: Read Write input	V_{REF}	: HSTL input reference input
BW0#, BW1#	: Byte Write data select	V_{DD}	: Power Supply
K, K#	: Input clock	$V_{DD}Q$	: Power Supply
C, C#	: Output clock	V_{SS}	: Ground
CQ, CQ#	: Echo clock	NC	: No connection
ZQ	: Output impedance matching	NC/xxM	: Expansion address for xxMb
DLL#	: PLL disable		

Remarks 1. ×××# indicates active LOW.

2. Refer to **Package Dimensions** for the index mark.

3. 2A, 3A, 7A and 10A are expansion addresses : 3A for 36Mb
: 3A and 10A for 72Mb
: 3A,10A and 2A for 144Mb
: 3A, 10A, 2A and 7A for 288Mb

2A and 10A of this product can also be used as NC.

Pin Description

(1/2)

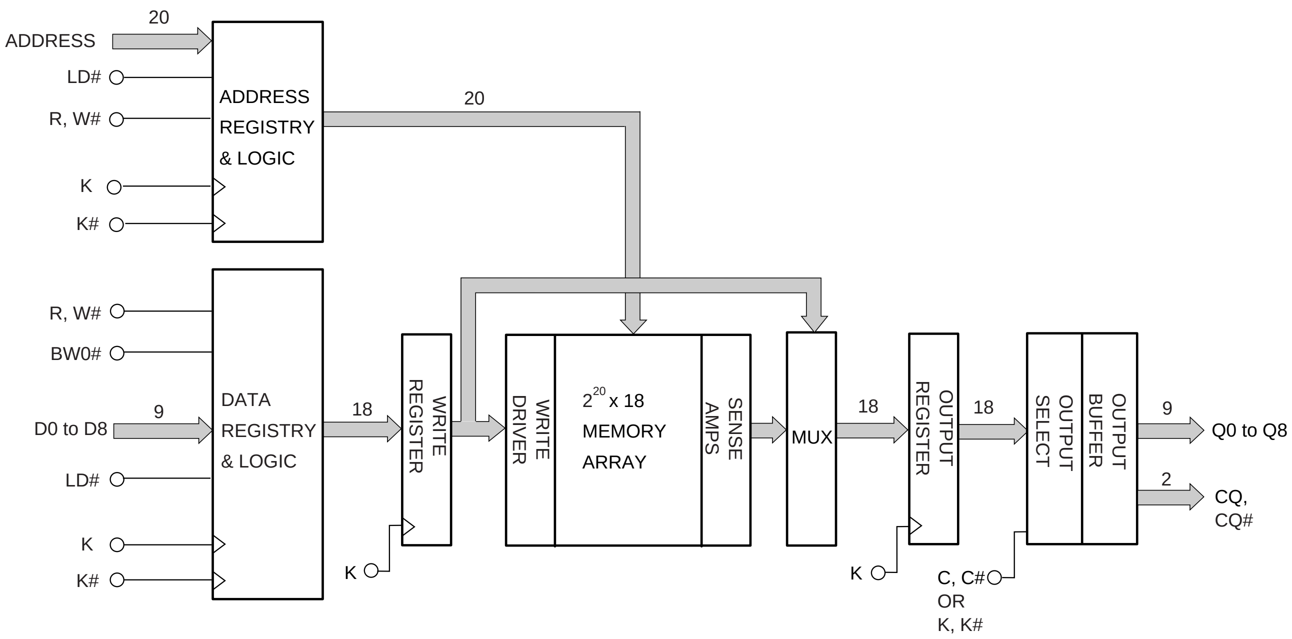
Symbol	Type	Description
A	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of two words (one clock period of bus activity). These inputs are ignored when device is deselected, i.e., NOP (LD# = HIGH).
D0 to Dxx	Input	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See **Pin Arrangement** for ball site location of individual signals. X9 device uses D0 to D8. X18 device uses D0 to D17.
Q0 to Qxx	Output	Synchronous Data Outputs: Output data is synchronized to the respective C and C# or to K and K# rising edges if C and C# are tied HIGH. Data is output in synchronization with C and C# (or K and K#), depending on the LD# and R, W# command. See **Pin Arrangement** for ball site location of individual signals. X9 device uses Q0 to Q8. x18 device uses Q0 to Q17.
LD#	Input	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data (one clock period of bus activity).
R, W#	Input	Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R, W# is HIGH, WRITE when R, W# is LOW) for the loaded address. R, W# must meet the setup and hold times around the rising edge of K.
BWx#	Input	Synchronous Byte Writes: When LOW these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See **Pin Arrangement** for signal to data relationships. X9 device uses BW0#. x18 device uses BW0#, BW1#. See **Byte Write Operation** for relation between BWx# and Dxx.
K, K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C, C#	Input	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of C# is used as the output timing reference for first output data. The rising edge of C is used as the output reference for second output data. Ideally, #C is 180 degrees out of phase with C. When use of K and K# as the reference instead of C and C#, then fixed C and C# to HIGH. Operation cannot be guaranteed unless C and C# are fixed to HIGH (i.e. toggle of C and C#)

(2/2)

Symbol	Type	Description
CQ, CQ#	Output	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tristates. If C and C# are stopped (if K and K# are stopped in the single clock mode), CQ and CQ# will also stop.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. Q, CQ and CQ# output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to ground. The output impedance can be minimized by directly connect ZQ to $V_{DD}Q$. This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 20 μs upon power-up to account for drifts in supply voltage and temperature. After replacement for a resistor, the new output impedance is reset by implementing power-on sequence.
DLL#	Input	PLL Disable: When debugging the system or board, the operation can be performed at a clock frequency slower than TKHKH (MAX.) without the PLL circuit being used, if DLL# = LOW. The AC/DC characteristics cannot be guaranteed. For normal operation, DLL# must be HIGH and it can be connected to $V_{DD}Q$ through a 10 kΩ or less resistor.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 1.8 V I/O level. These balls may be left Not Connected if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 Clock Input: 1.8 V I/O level. This pin must be tied to VSS if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: 1.8 V I/O level. When providing any external voltage to TDO signal, it is recommended to pull up to V_{DD}.
V_{REF}	–	HSTL Input Reference Voltage: Nominally $V_{DD}Q/2$. Provides a reference voltage for the input buffers.
V_{DD}	Supply	Power Supply: 1.8 V nominal. See **Recommended DC Operating Conditions** and **DC Characteristics** for range.
$V_{DD}Q$	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5 V. 1.8 V is also permissible. See **Recommended DC Operating Conditions** and **DC Characteristics** for range.
V_{SS}	Supply	Power Supply: Ground
NC	–	No Connect: These signals are not connected internally.

Block Diagram

[μPD46184095B]



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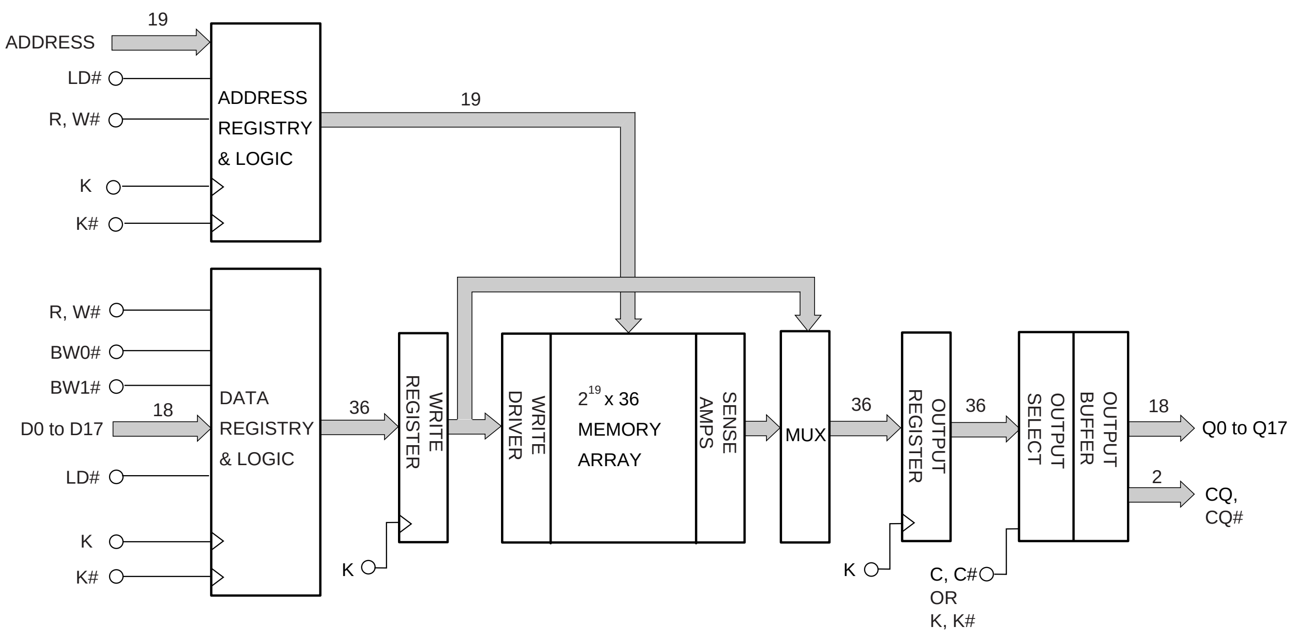


Power-On Sequence in DDR II SRAM

DDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.
The following timing charts show the recommended power-on sequence.

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, $V_{DD}Q$, V_{REF}, then V_{IN}. V_{DD} and $V_{DD}Q$ can be applied simultaneously, as long as $V_{DD}Q$ does not exceed V_{DD} by more than 0.5 V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, $V_{DD}Q$, V_{DD}, V_{SS}. V_{DD} and $V_{DD}Q$ can be removed simultaneously, as long as $V_{DD}Q$ does not exceed V_{DD} by more than 0.5 V during power-down.

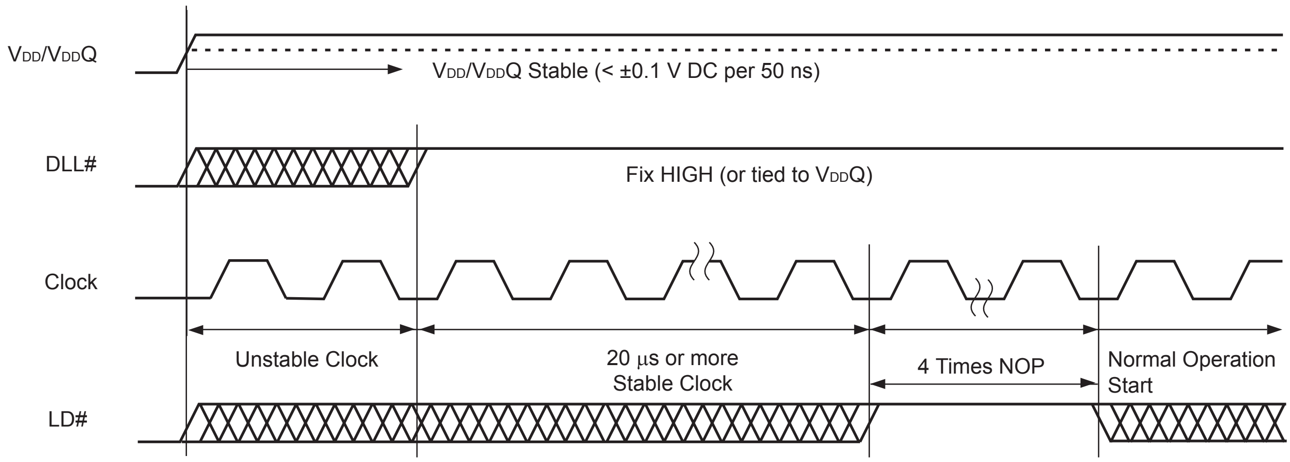
Power-On Sequence

Apply power and tie DLL# to HIGH.
Apply $V_{DD}Q$ before V_{REF} or at the same time as V_{REF}.
Provide stable clock for more than 20 μs to lock the PLL.
Continuous min.4 NOP(LD# = high) cycles are required after PLL lock up is done.

PLL Constraints

The PLL uses K clock as its synchronizing input and the input should have low phase jitter which is specified as TKC var. The PLL can cover 120 MHz as the lowest frequency. If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an undesired clock frequency.

Power-On Waveforms



Truth Table

Operation	LD#	R, W#	CLK	D or Q		
WRITE cycle Load address, input write data on consecutive K and K# rising edge	L	L	L → H	Data in		
				Input data	D(A+0)	D(A+1)
				Input clock	K(t+1) ↑	K#(t+1) ↑
READ cycle Load address, read data on consecutive C and C# rising edge	L	H	L → H	Data out		
				Output data	Q(A+0)	Q(A+1)
				Output clock	C#(t+1) ↑	C(t+2) ↑
NOP (No operation)	H	×	L → H	D = ×, Q = High-Z		
Clock stop	×	×	Stopped	Previous state		

Remarks 1. H : HIGH, L : LOW, × : don't care, ↑ : rising edge.

2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges except if C and C# are HIGH then Data outputs are delivered at K and K# rising edges.

3. All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.

4. This device contains circuitry that ensure the outputs to be in high impedance during power-up.

5. Refer to state diagram and timing diagrams for clarification.

6. It is recommended that K = K# = C = C# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.

Byte Write Operation

[μPD46184095B]

Operation	K	K#	BW0#
Write D0 to D8	L → H	–	0
	–	L → H	0
Write nothing	L → H	–	1
	–	L → H	1

Remarks 1. H : HIGH, L : LOW, → : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

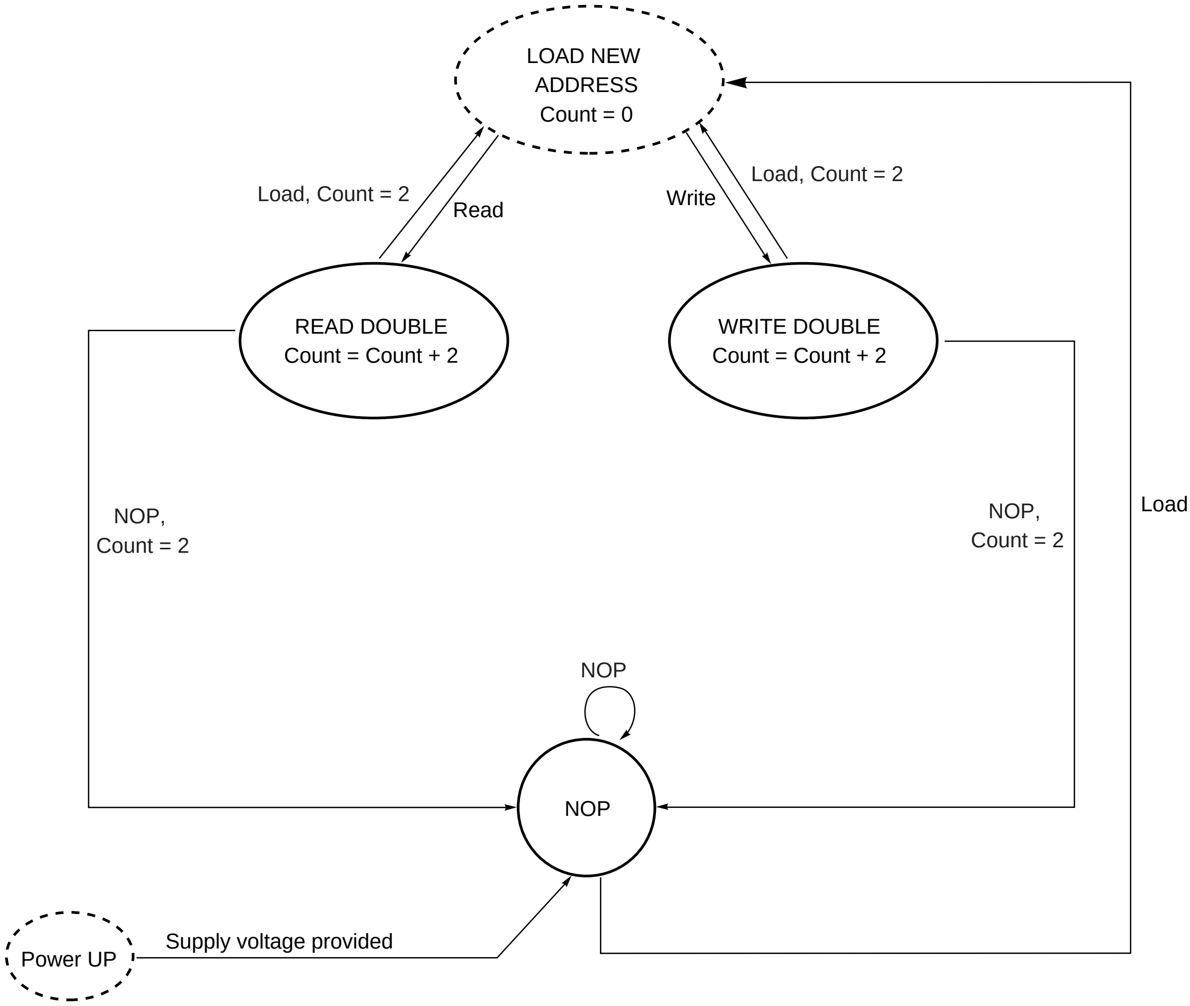
[μPD46184185B]

Operation	K	K#	BW0#	BW1#
Write D0 to D17	L → H	–	0	0
	–	L → H	0	0
Write D0 to D8	L → H	–	0	1
	–	L → H	0	1
Write D9 to D17	L → H	–	1	0
	–	L → H	1	0
Write nothing	L → H	–	1	1
	–	L → H	1	1

Remarks 1. H : HIGH, L : LOW, → : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Remark State machine control timing sequence is controlled by K.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +2.5	V
Output supply voltage	$V_{DD}Q$		–0.5 to V_{DD}	V
Input voltage	V_{IN}		–0.5 to V_{DD}+0.5 (2.5 V MAX.)	V
Input / Output voltage	$V_{I/O}$		–0.5 to $V_{DD}Q$+0.5 (2.5 V MAX.)	V
Operating ambient temperature	T_A	(E** series)	0 to 70	°C
		(E**Y series)	–40 to 85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C, T_A = –40 to 85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		1.7	1.8	1.9	V	
Output supply voltage	$V_{DD}Q$		1.4		V_{DD}	V	1
Input HIGH voltage	$V_{IH (DC)}$		V_{REF} +0.1		$V_{DD}Q$+0.3	V	1, 2
Input LOW voltage	$V_{IL (DC)}$		–0.3		V_{REF} –0.1	V	1, 2
Clock input voltage	V_{IN}		–0.3		$V_{DD}Q$+0.3	V	1, 2
Reference voltage	V_{REF}		0.68		0.95	V	

Notes 1. During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

2. Power-up: VIH ≤ $V_{DD}Q$ + 0.3 V and V_{DD} ≤ 1.7 V and $V_{DD}Q$ ≤ 1.4 V for t ≤ 200 ms

Recommended AC Operating Conditions (T_A = 0 to 70°C, T_A = –40 to 85°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	$V_{IH (AC)}$		V_{REF} +0.2		V	1
Input LOW voltage	$V_{IL (AC)}$			V_{REF} –0.2	V	1

Note 1. Overshoot: $V_{IH (AC)}$ ≤ V_{DD} + 0.7 V (2.5 V MAX.) for t ≤ TKHKH/2

Undershoot: $V_{IL (AC)}$ ≥ –0.5 V for t ≤ TKHKH/2

Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).

DC Characteristics 1 (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition		MIN.	MAX.		Unit	Note
					x9	x18		
Input leakage current	I_{LI}			–2	+2		μA	
I/O leakage current	I_{LO}			–2	+2		μA	
Operating supply current (Read cycle / Write cycle)	I_{DD}	$V_{IN} \le V_{IL}$ or $V_{IN} \ge V_{IH}$, $I_{I/O}$ = 0 mA, Cycle = MAX.	-E33		500	530	mA	
			-E40		450	480		
Standby supply current (NOP)	I_{SB1}	$V_{IN} \le V_{IL}$ or $V_{IN} \ge V_{IH}$, $I_{I/O}$ = 0 mA, Cycle = MAX. Inputs static	-E33		390	400	mA	
			-E40		380	380		
Output HIGH voltage	$V_{OH(Low)}$	$\|I_{OH}\| \le 0.1$ mA		$V_{DD}Q$–0.2	$V_{DD}Q$		V	3, 4
	V_{OH}	Note1		$V_{DD}Q$/2–0.12	$V_{DD}Q$/2+0.12		V	3, 4
Output LOW voltage	$V_{OL(Low)}$	$I_{OL} \le 0.1$ mA		V_{SS}	0.2		V	3, 4
	V_{OL}	Note2		$V_{DD}Q$/2–0.12	$V_{DD}Q$/2+0.12		V	3, 4

Notes 1. Outputs are impedance-controlled. $| I_{OH} | = (V_{DD}Q/2)/(RQ/5) \pm 15\%$ for values of 175 Ω ≤ RQ ≤ 350 Ω.

2. Outputs are impedance-controlled. $I_{OL} = (V_{DD}Q/2)/(RQ/5) \pm 15\%$ for values of 175 Ω ≤ RQ ≤ 350 Ω.

3. AC load current is higher than the shown DC values.

4. HSTL outputs meet JEDEC HSTL Class I standards.

DC Characteristics 2 (T_A = –40 to 85°C, V_{DD} = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition		MIN.	MAX.		Unit	Note
					x9	x18		
Input leakage current	I_{LI}			–2	+2		μA	
I/O leakage current	I_{LO}			–2	+2		μA	
Operating supply current (Read cycle / Write cycle)	I_{DD}	$V_{IN} \le V_{IL}$ or $V_{IN} \ge V_{IH}$, $I_{I/O}$ = 0 mA, Cycle = MAX.	-E33Y		650	680	mA	
			-E40Y		600	630		
Standby supply current (NOP)	I_{SB1}	$V_{IN} \le V_{IL}$ or $V_{IN} \ge V_{IH}$, $I_{I/O}$ = 0 mA, Cycle = MAX. Inputs static	-E33Y		510	530	mA	
			-E40Y		490	500		
Output HIGH voltage	$V_{OH(Low)}$	$\|I_{OH}\| \le 0.1$ mA		$V_{DD}Q$–0.2	$V_{DD}Q$		V	3, 4
	V_{OH}	Note1		$V_{DD}Q$/2–0.12	$V_{DD}Q$/2+0.12		V	3, 4
Output LOW voltage	$V_{OL(Low)}$	$I_{OL} \le 0.1$ mA		V_{SS}	0.2		V	3, 4
	V_{OL}	Note2		$V_{DD}Q$/2–0.12	$V_{DD}Q$/2+0.12		V	3, 4

Notes 1. Outputs are impedance-controlled. | I_{OH} | = ($V_{DD}Q$/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.

2. Outputs are impedance-controlled. I_{OL} = ($V_{DD}Q$/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.

3. AC load current is higher than the shown DC values.

4. HSTL outputs meet JEDEC HSTL Class I standards.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Input capacitance (Address, Control)	C_{IN}	V_{IN} = 0 V		5	pF
Input / Output capacitance (D, Q, CQ, CQ#)	$C_{I/O}$	$V_{I/O}$ = 0 V		7	pF
Clock Input capacitance	C_{clk}	V_{clk} = 0 V		6	pF

Remark These parameters are periodically sampled and not 100% tested.

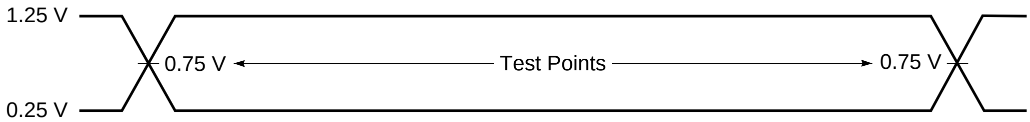
Thermal Characteristics

Parameter	Symbol	Substrate	Airflow	TYP.	Unit
Thermal resistance from junction to ambient air	θja	4-layer	0 m/s	16.5	°C/W
			1 m/s	13.2	°C/W
		8-layer	0 m/s	15.5	°C/W
			1 m/s	12.6	°C/W
Thermal characterization parameter from junction to the top center of the package surface	Ψjt	4-layer	0 m/s	0.07	°C/W
			1 m/s	0.13	°C/W
		8-layer	0 m/s	0.06	°C/W
			1 m/s	0.12	°C/W
Thermal resistance from junction to case	θjc			3.86	°C/W

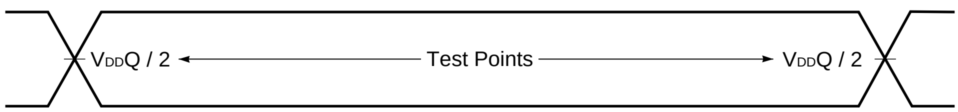
AC Characteristics (T_A = 0 to 70°C, T_A = –40 to 85°C, V_{DD} = 1.8 ± 0.1 V)

AC Test Conditions (V_{DD} = 1.8 ± 0.1 V, V_{DDQ} = 1.4 V to V_{DD})

Input waveform (Rise / Fall time ≤ 0.3 ns)

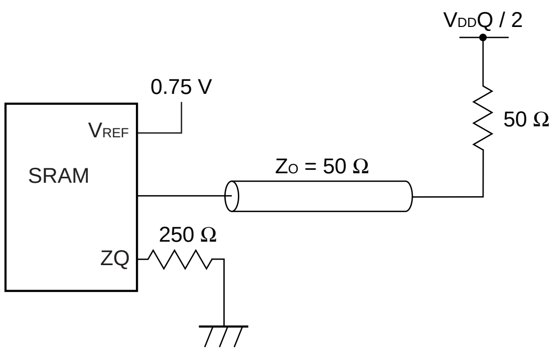


Output waveform



Output load condition

Figure 1. External load at test



Read and Write Cycle

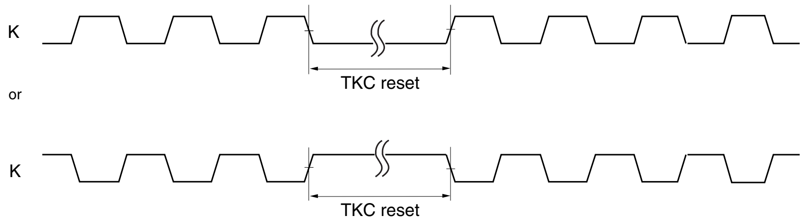
Parameter	Symbol	-E33,-E33Y (300 MHz)		-E40,-E40Y (250 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Clock							
Average Clock cycle time (K, K#, C, C#)	TKHKH	3.3	8.4	4.0	8.4	ns	1
Clock phase jitter (K, K#, C, C#)	TKC var		0.2		0.2	ns	2
Clock HIGH time (K, K#, C, C#)	TKHKL	1.32		1.6		ns	
Clock LOW time (K, K#, C, C#)	TKLKH	1.32		1.6		ns	
Clock HIGH to Clock# HIGH (K → K#, C → C#)	TKHK#H	1.49		1.8		ns	
Clock# HIGH to Clock HIGH (K# → K, C# → C)	TK#HKH	1.49		1.8		ns	
Clock to data clock (K → C, K# → C#)	TKHCH	0	1.45	0	1.8	ns	
PLL lock time (K, C)	TKC lock	20		20		μs	3
K static to PLL reset	TKC reset	30		30		ns	4
Output Times							
CQ HIGH to CQ# HIGH (CQ → CQ#)	TCQHCQ#H	1.24		1.55		ns	5
CQ# HIGH to CQ HIGH (CQ# → CQ)	TCQ#HCQH	1.24		1.55		ns	5
C, C# HIGH to output valid	TCHQV		0.45		0.45	ns	
C, C# HIGH to output hold	TCHQX	−0.45		−0.45		ns	
C, C# HIGH to echo clock valid	TCHCQV		0.45		0.45	ns	
C, C# HIGH to echo clock hold	TCHCQX	−0.45		−0.45		ns	
CQ, CQ# HIGH to output valid	TCQHQV		0.27		0.3	ns	6
CQ, CQ# HIGH to output hold	TCQHQX	−0.27		−0.3		ns	6
C HIGH to output High-Z	TCHQZ		0.45		0.45	ns	
C HIGH to output Low-Z	TCHQX1	−0.45		−0.45		ns	
Setup Times							
Address valid to K rising edge	TAVKH	0.4		0.5		ns	7
Synchronous load input (LD#), read write input (R, W#) valid to K rising edge	TIVKH	0.4		0.5		ns	7
Data inputs and write data select inputs (BWx#) valid to K, K# rising edge	TDVKH	0.3		0.35		ns	7
Hold Times							
K rising edge to address hold	TKHAX	0.4		0.5		ns	7
K rising edge to synchronous load input (LD#), read write input (R, W#) hold	TKHIX	0.4		0.5		ns	7
K, K# rising edge to data inputs and write data select inputs (BWx#) hold	TKHDX	0.3		0.35		ns	7

Notes 1. When debugging the system or board, these products can operate at a clock frequency slower than TKHKH (MAX.) without the PLL circuit being used, if DLL# = LOW. Read latency (RL) is changed to 1.0 clock cycle in this operation. The AC/DC characteristics cannot be guaranteed, however.

2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge. TKC var (MAX.) indicates a peak-to-peak value.

3. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for PLL lock retention.
PLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept NOP (LD# = HIGH) during these cycles.

4. K input is monitored for this operation. See below for the timing.



5. Guaranteed by design.

6. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.

7. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

Remarks 1. This parameter is sampled.

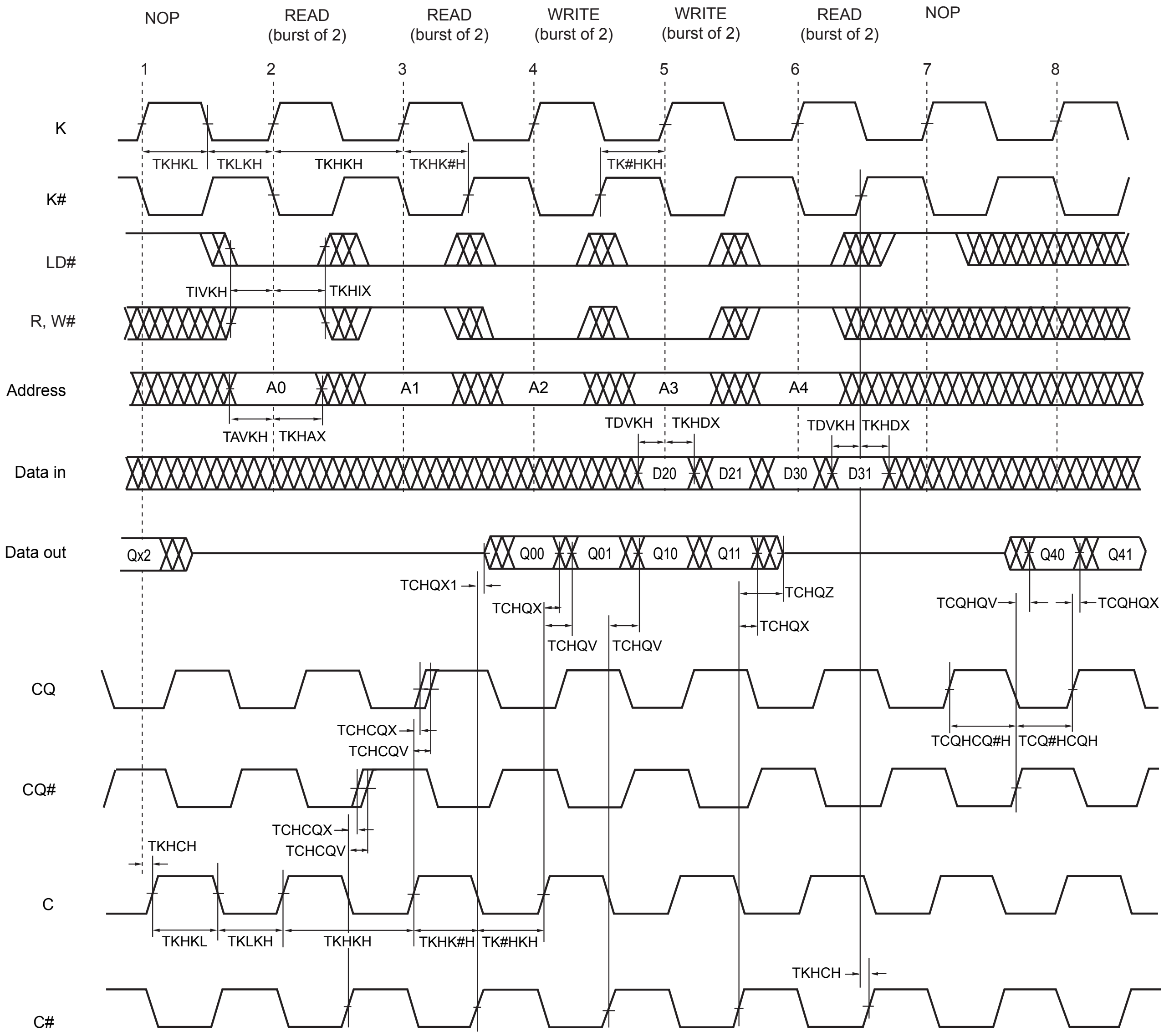
2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).

4. If C, C# are tied HIGH, K, K# become the references for C, C# timing parameters.

5. $V_{DD}Q$ is 1.5 V DC.

Read and Write Timing

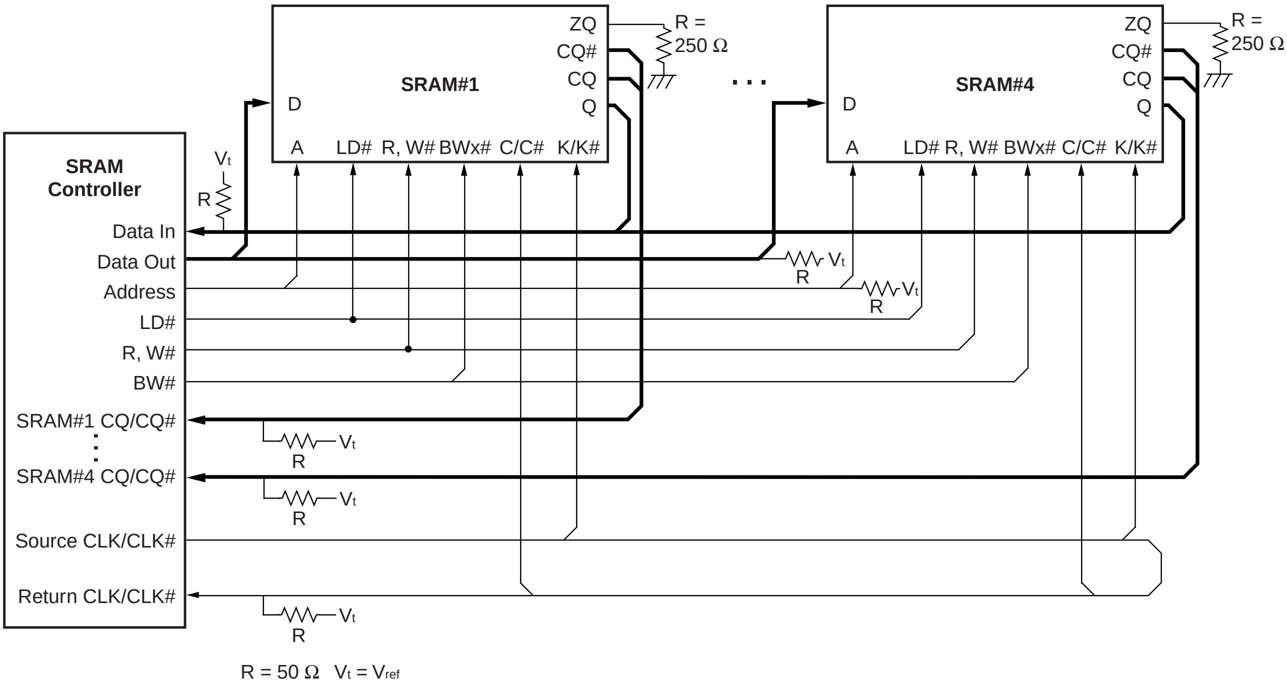


Remarks 1. Q01 refers to output from address A0+0.
Q02 refers to output from the next internal burst address following A0, i.e., A0+1.

2. Outputs are disabled (high impedance) 2.5 clock cycles after the last READ (LD# = LOW, R, W# = HIGH) is input in the sequences of [READ]-[NOP] and [READ]-[WRITE].

3. In this example, if address A4 = A3, data Q41 = D31 and Q42 = D32.
Write data is forwarded immediately as read results.

Application Example



Remark AC Characteristics are defined at the condition of SRAM outputs, CQ, CQ# and Q with termination.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

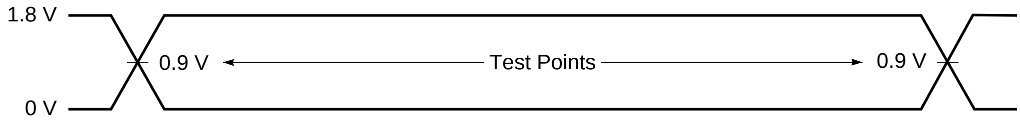
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V, unless otherwise noted)

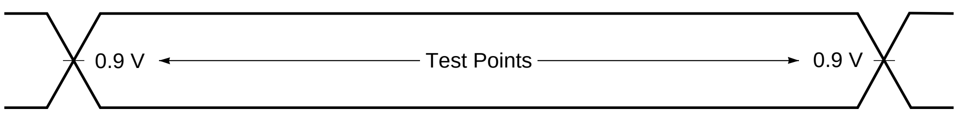
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	–5.0	+5.0	μA
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ $V_{DD}Q$, Outputs disabled	–5.0	+5.0	μA
JTAG input HIGH voltage	V_{IH}		1.3	V_{DD}+0.3	V
JTAG input LOW voltage	V_{IL}		–0.3	+0.5	V
JTAG output HIGH voltage	V_{OH1}	| I_{OHC} | = 100 μA	1.6		V
	V_{OH2}	| I_{OHT} | = 2 mA	1.4		V
JTAG output LOW voltage	V_{OL1}	I_{OLC} = 100 μA		0.2	V
	V_{OL2}	I_{OLT} = 2 mA		0.4	V

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

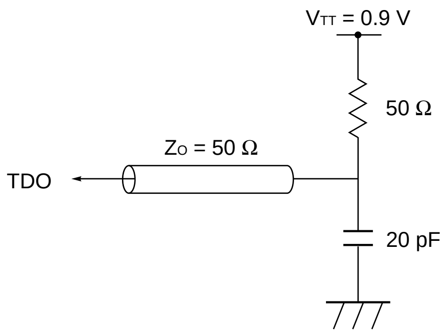


Output waveform



Output load

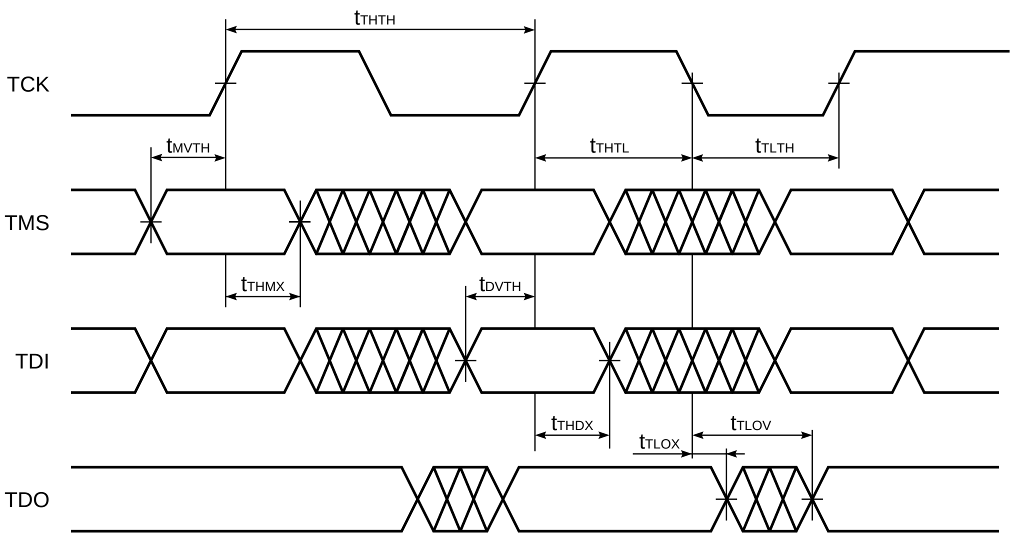
Figure 2. External load at test



JTAG AC Characteristics (T_A = 0 to 70°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock					
Clock cycle time	t_{THTH}		50		ns
Clock frequency	f_{TF}			20	MHz
Clock HIGH time	t_{THTL}		20		ns
Clock LOW time	t_{TLTH}		20		ns
Output time					
TCK LOW to TDO unknown	t_{TLOX}		0		ns
TCK LOW to TDO valid	t_{TLOV}			10	ns
Setup time					
TMS setup time	t_{MVTH}		5		ns
TDI valid to TCK HIGH	t_{DVTH}		5		ns
Capture setup time	t_{CS}		5		ns
Hold time					
TMS hold time	t_{THMX}		5		ns
TCK HIGH to TDI invalid	t_{THDX}		5		ns
Capture hold time	t_{CH}		5		ns

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	107	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD46184095B	2M x 9	XXXX	0000 0000 0101 0101	00000010000	1
μPD46184185B	1M x 18	XXXX	0000 0000 0001 1001	00000010000	1

SCAN Exit Order

Bit no.	Signal name x9	Signal name x18	Bump ID
1	C#		6R
2	C		6P
3	A		6N
4	A		7P
5	A		7N
6	A		7R
7	A		8R
8	A		8P
9	A		9R
10	Q0		11P
11	D0		10P
12	NC		10N
13	NC		9P
14	NC	Q1	10M
15	NC	D1	11N
16	NC		9M
17	NC		9N
18	Q1	Q2	11L
19	D1	D2	11M
20	NC		9L
21	NC		10L
22	NC	Q3	11K
23	NC	D3	10K
24	NC		9J
25	NC		9K
26	Q2	Q4	10J
27	D2	D4	11J
28	ZQ		11H
29	NC		10G
30	NC		9G
31	NC	Q5	11F
32	NC	D5	11G
33	NC		9F
34	NC		10F
35	Q3	Q6	11E
36	D3	D6	10E

Bit no.	Signal name x9	Signal name x18	Bump ID
37	NC		10D
38	NC		9E
39	NC	Q7	10C
40	NC	D7	11D
41	NC		9C
42	NC		9D
43	Q4	Q8	11B
44	D4	D8	11C
45	NC		9B
46	NC		10B
47	CQ		11A
48	–		Internal
49	A		9A
50	A		8B
51	A		7C
52	A		6C
53	LD#		8A
54	NC		7A
55	BW0#		7B
56	K		6B
57	K#		6A
58	NC		5B
59	NC	BW1#	5A
60	R, W#		4A
61	A		5C
62	A		4B
63	A	NC	3A
64	DLL#		1H
65	CQ#		1A
66	NC	Q9	2B
67	NC	D9	3B
68	NC		1C
69	NC		1B
70	NC	Q10	3D
71	NC	D10	3C
72	NC		1D

Bit no.	Signal name x9	Signal name x18	Bump ID
73	NC		2C
74	Q5	Q11	3E
75	D5	D11	2D
76	NC		2E
77	NC		1E
78	NC	Q12	2F
79	NC	D12	3F
80	NC		1G
81	NC		1F
82	Q6	Q13	3G
83	D6	D13	2G
84	NC		1J
85	NC		2J
86	NC	Q14	3K
87	NC	D14	3J
88	NC		2K
89	NC		1K
90	Q7	Q15	2L
91	D7	D15	3L
92	NC		1M
93	NC		1L
94	NC	Q16	3N
95	NC	D16	3M
96	NC		1N
97	NC		2M
98	Q8	Q17	3P
99	D8	D17	2N
100	NC		2P
101	NC		1P
102	A		3R
103	A		4R
104	A		4P
105	A		5P
106	A		5N
107	A		5R

JTAG Instructions

Instructions	Description
EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE / PRELOAD	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (tCS plus tCH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM Q pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	2
1	0	0	SAMPLE / PRELOAD	
1	0	1	RESERVED	2
1	1	0	RESERVED	2
1	1	1	BYPASS	

Notes 1. TRISTATE all Q pins and CAPTURE the pad values into a SERIAL SCAN LATCH.

2. Do not use this instruction code because the vendor uses it to evaluate this product.

Output Pin States of CQ, CQ# and Q

Instructions	Control-Register Status	Output Pin Status	
		CQ,CQ#	Q
EXTEST	0	Update	High-Z
	1	Update	Update
IDCODE	0	SRAM	SRAM
	1	SRAM	SRAM
SAMPLE-Z	0	High-Z	High-Z
	1	High-Z	High-Z
SAMPLE	0	SRAM	SRAM
	1	SRAM	SRAM
BYPASS	0	SRAM	SRAM
	1	SRAM	SRAM

Remark The output pin statuses during each instruction vary according to the Control-Register status (value of Boundary Scan Register, bit no. 48).

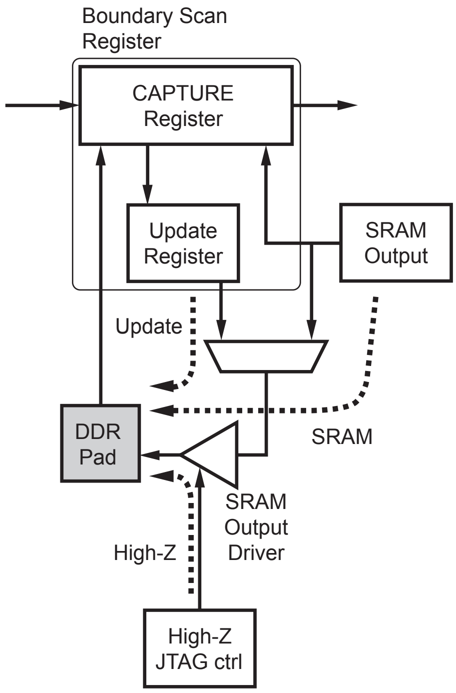
There are three statuses:

Update : Contents of the "Update Register" are output to the output pin (DDR Pad).

SRAM : Contents of the SRAM internal output "SRAM Output" are output to the output pin (DDR Pad).

High-Z :The output pin (DDR Pad) becomes high impedance by controlling of the "High-Z JTAG ctrl".

The Control-Register status is set during Update-DR at the EXTEST or SAMPLE instruction.

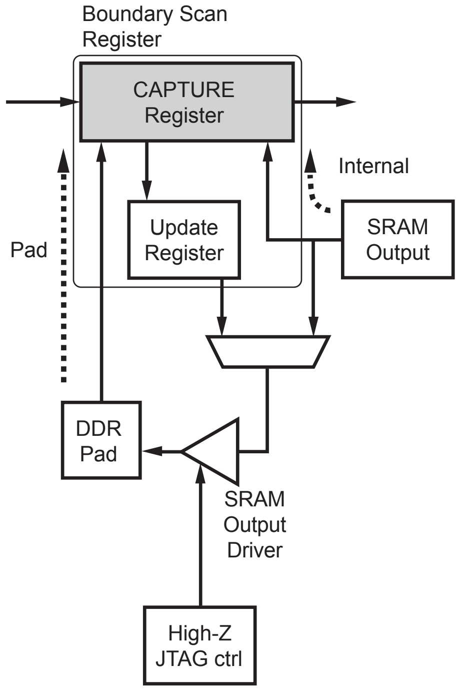


Boundary Scan Register Status of Output Pins CQ, CQ# and Q

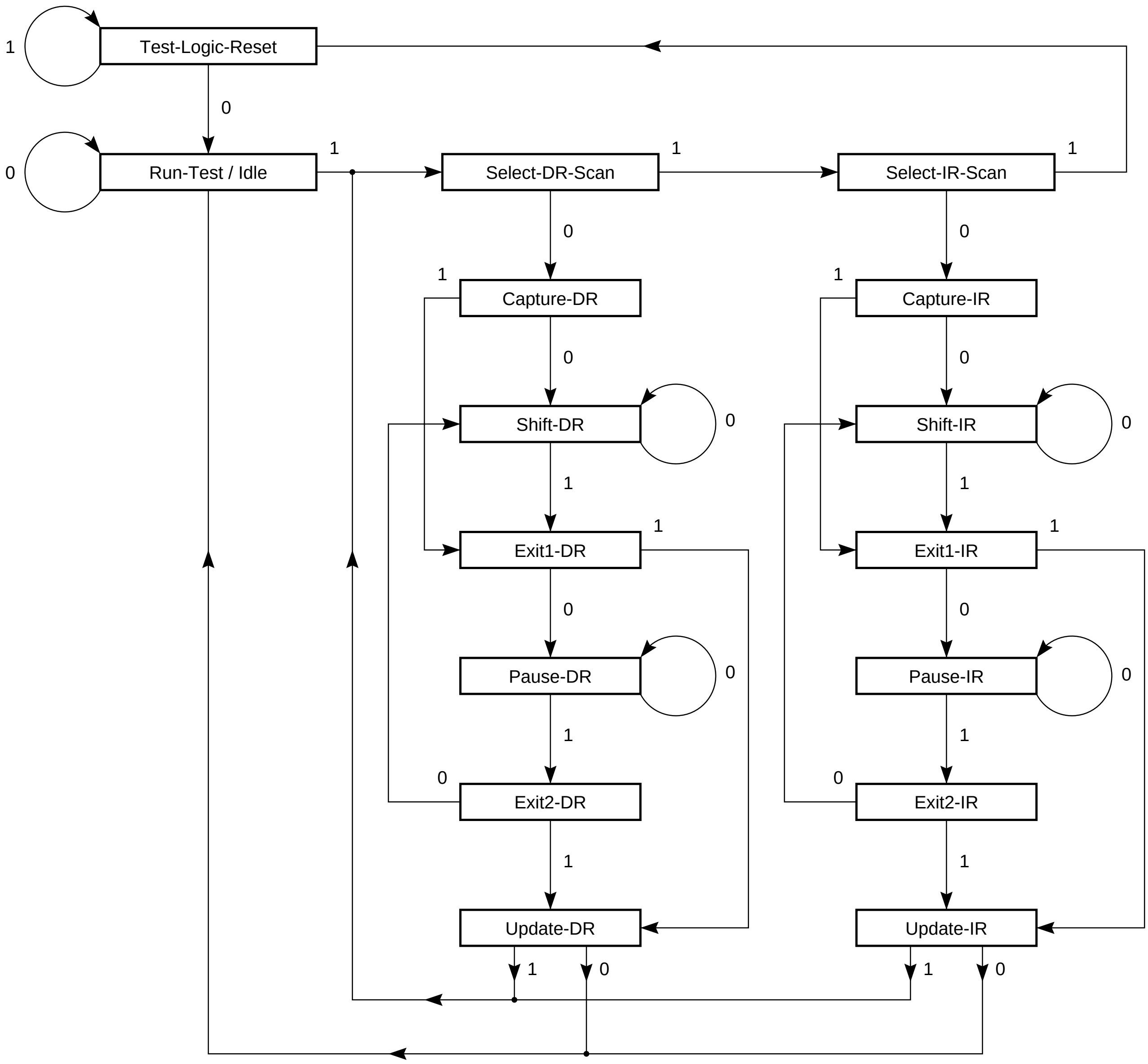
Instructions	SRAM Status	Boundary Scan Register Status		Note
		CQ,CQ#	Q	
EXTEST	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
IDCODE	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	
SAMPLE-Z	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
SAMPLE	READ (Low-Z)	Internal	Internal	
	NOP (High-Z)	Internal	Pad	
BYPASS	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	

Remark The Boundary Scan Register statuses during execution each instruction vary according to the instruction code and SRAM operation mode.
There are two statuses:

Pad : Contents of the output pin (DDR Pad) are captured in the "CAPTURE Register" in the Boundary Scan Register.
Internal : Contents of the SRAM internal output "SRAM Output" are captured in the "CAPTURE Register" in the Boundary Scan Register.



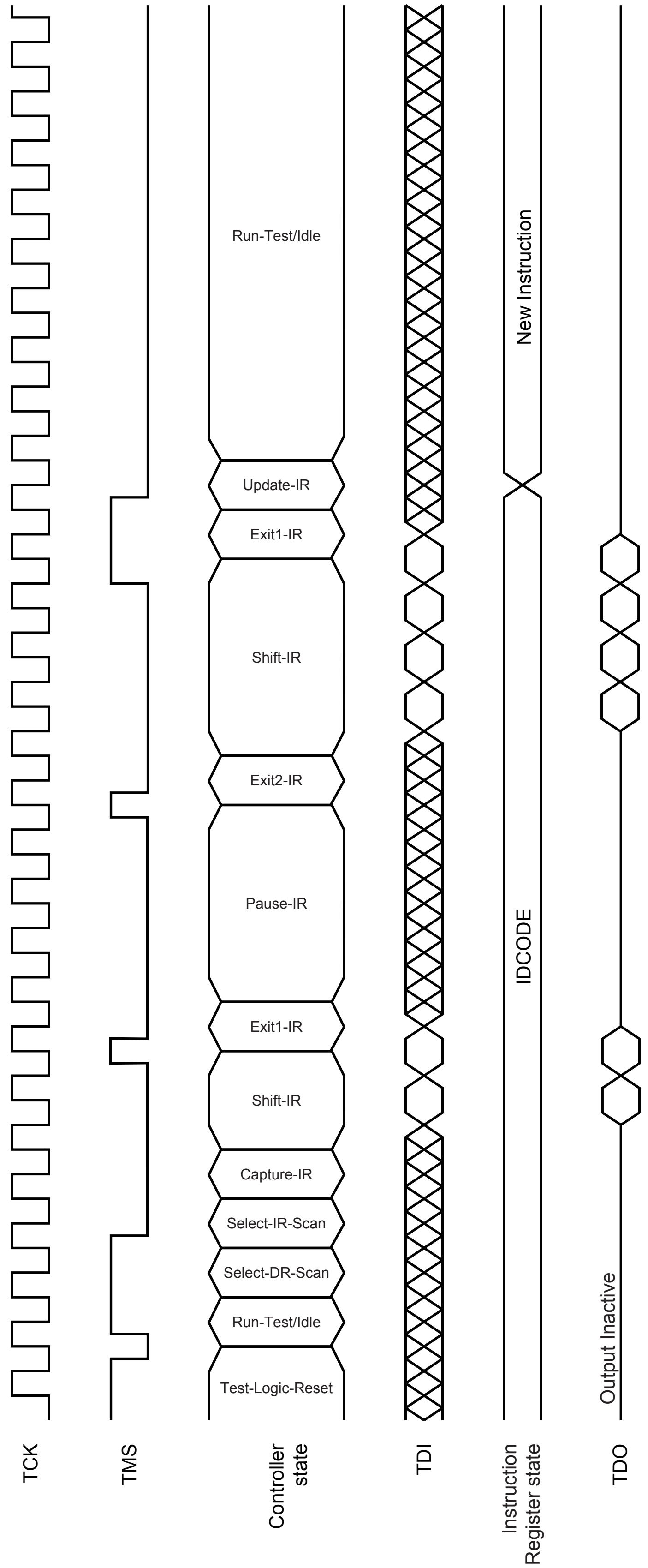
TAP Controller State Diagram



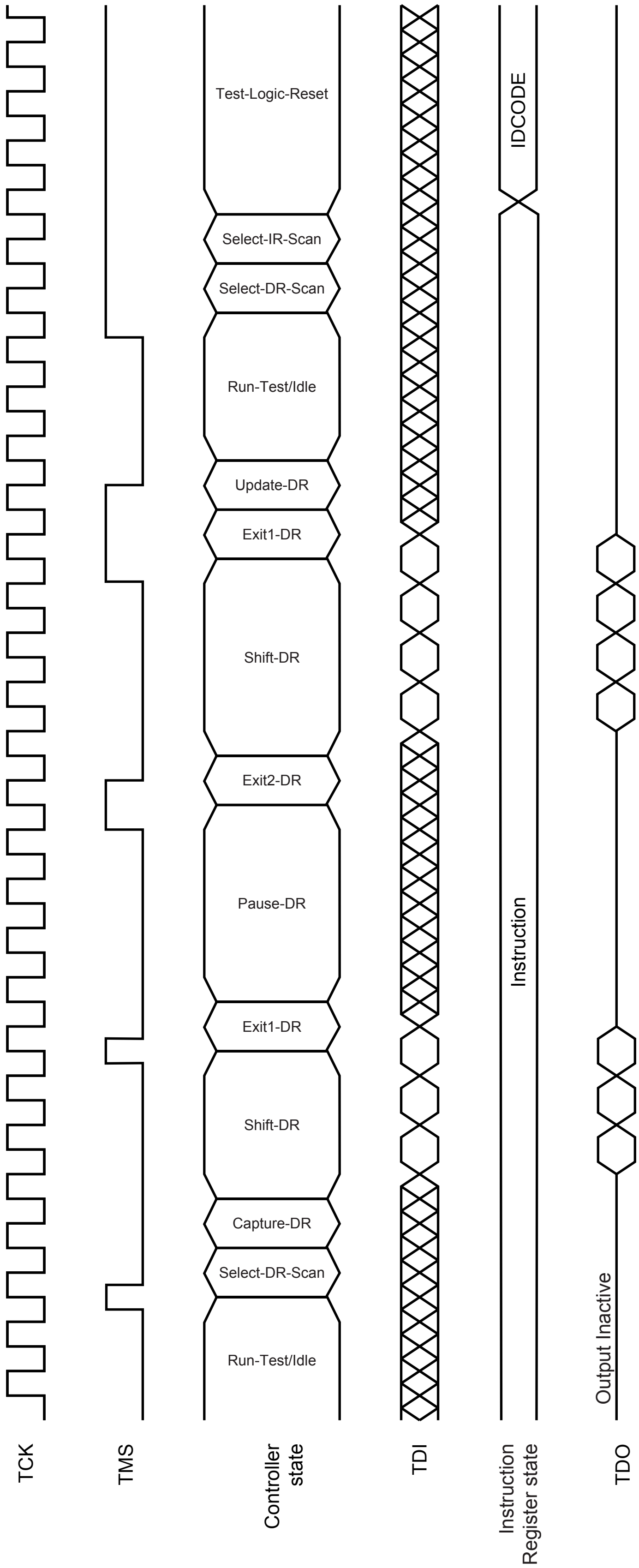
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS may be left open but fix them to V_{DD} via a resistor of about 1 kΩ when the TAP controller is not used. TDO should be left unconnected also when the TAP controller is not used.

Test Logic Operation (Instruction Scan)

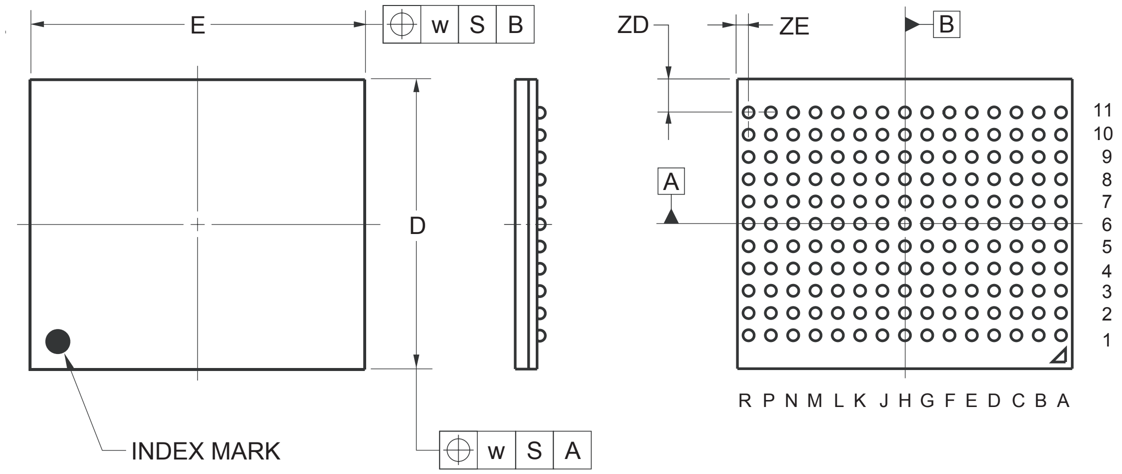


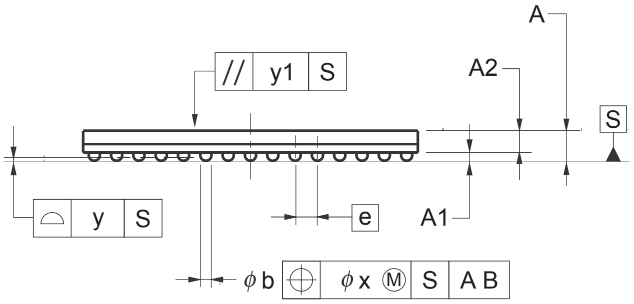
Test Logic (Data Scan)



Package Dimensions

165-PIN PLASTIC BGA(13x15)





(UNIT:mm)

ITEM	DIMENSIONS
D	13.00±0.10
E	15.00±0.10
w	0.30
A	1.35±0.11
A1	0.37±0.05
A2	0.98
e	1.00
b	0.50 +0.10 −0.05
x	0.10
y	0.15
y1	0.25
ZD	1.50
ZE	0.50

T165F1-100-EQ1

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD46184095BF1-EQ1	:	165-pin PLASTIC BGA (13 x 15)
μPD46184185BF1-EQ1	:	165-pin PLASTIC BGA (13 x 15)

Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

Rev.	Date	Description	
		Page	Summary
Rev.1.00	’12.06.01	-	New Data Sheet
Rev.2.00	’12.11.09	ALL	Addition : -E33,-E33Y series, Lead series Deletion : -E50,-E50Y series