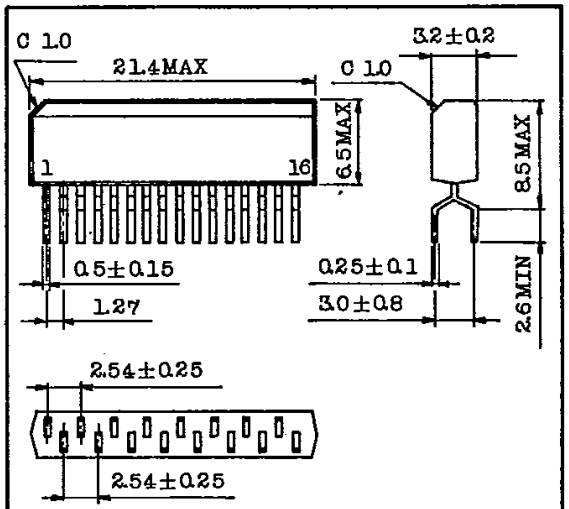
GND ISOLATOR

TA7414P is a ground isolator IC for car audio equipments.
This IC is contain dual channel differential amplifier and audio muting circuit.

- Dual Channel Differential Amplifier
- High Common Mode Rejection Ratio
  CMRR=55dB(Typ.)
  (f=1kHz, V_{CM}=-10dBm)
- Low Distortion
  THD=0.01%(Typ.)
  (V_{OUT}=100mVrms)
- Low Noise
  V_{NO}=5μVrms(Typ.)
  (R_g=10kΩ, BW=20Hz~20kHz)
- Audio Muting Circuit
  Attenuation=80dB(Typ.)
  (V_{OUT}=-10dBm)
- Operating Supply Voltage
  $V_{CC(opr)}$=8~16V

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.2 leads.

JEDEC	—
TOSHIBA	Z16A-P

Weight : 1.0g(TYP.)

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage*	$V_{CC(surge)}$	50	V
Supply Voltage	V_{CC}	18	V
Power Dissipation (Note)	P_D	750	mW
Operating Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~150	°C

* Condition : Series resistance 100Ω insert Pin ① (V_{CC})

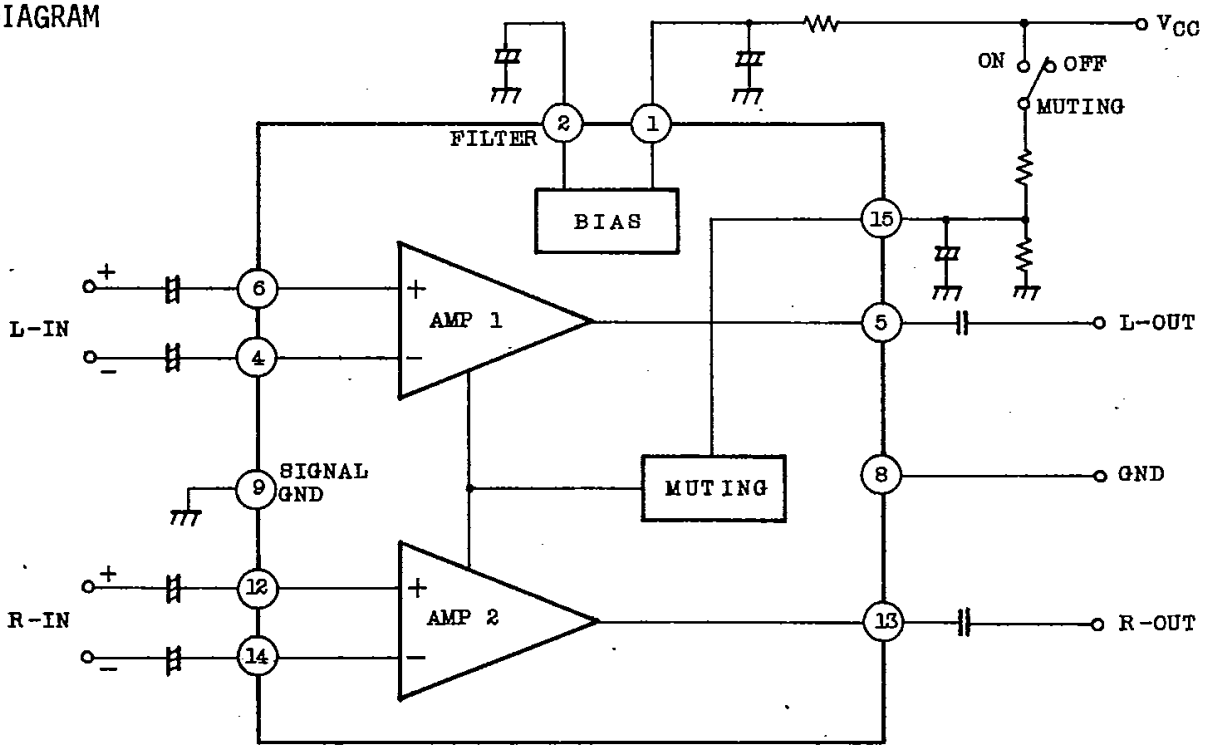
Note: Derated above Ta=25°C in the proportion of 6mW/°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=13.2V, R_L=15kΩ, f=1kHz, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CCQ}	1	V_{NO}=0, MUTE:OFF	-	3	5	mA
Voltage Gain	G_V	1	V_{OUT}=-10dBm	-2	0	2	dB
Maximum Output Voltage	V_{OM}	1	V_{CC}=8V, THD=0.1%	-10	-8	-	dBm
Total Harmonic Distortion	THD	1	V_{OUT}=100mV_{rms} BW=400Hz~80kHz	-	0.01	0.03	%
Cross Talk	C.T	1	V_{IN}=-10dBm	-	65	-	dB
Input Impedance	Z_i	1	V_{OUT}=-10dBm	-	70	-	kΩ
Output Impedance	Z_o	1	V_{OUT}=-20dBm	-	0.45	-	kΩ
Output Noise Voltage	V_{NO}	2	Rg=10kΩ, BW=20Hz~20kHz	-	5	10	μV_{rms}
Muting Attenuation	ATT	3	V_{OUT}=-10dBm	60	80	-	dB
Muting Threshold Voltage	V_M	3	ATT=3dB	1.7	2.2	2.7	V
Common Mode Rejection Ratio	CMRR	4	V_{CM}=-10dBm	46	55	-	dB
Common Mode Input Voltage	V_{CM} (MAX)	4	V_{CC}=8V, CMRR=40dB	1.0	1.6	-	V_{rms}

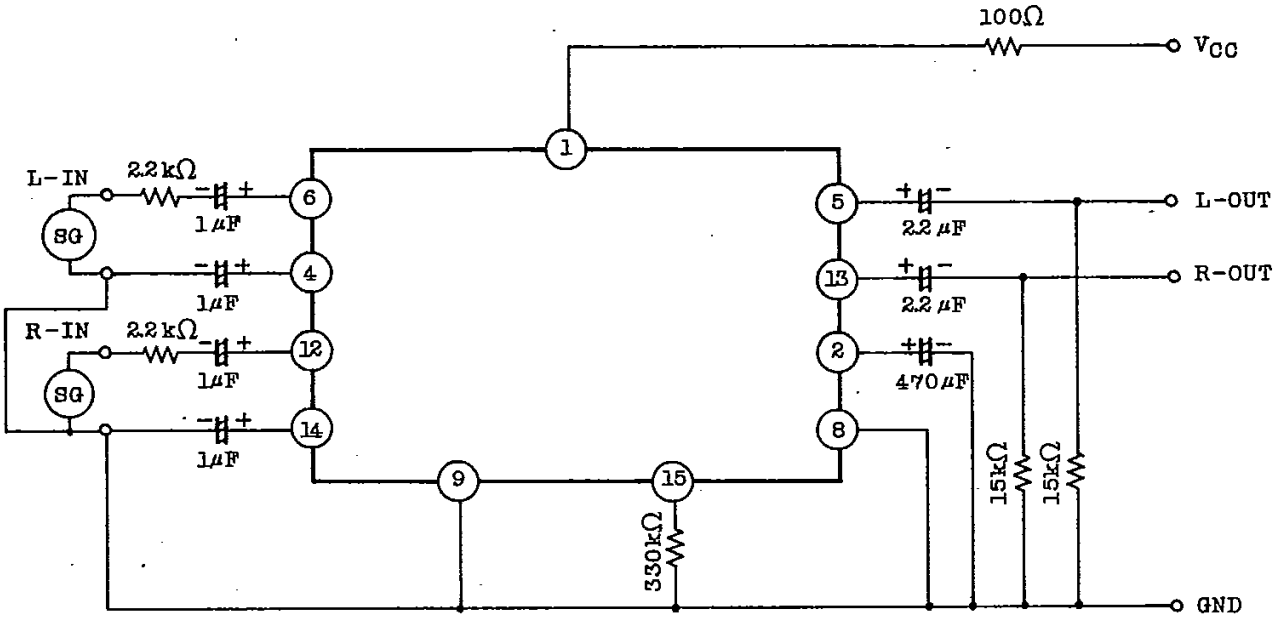
BLOCK DIAGRAM



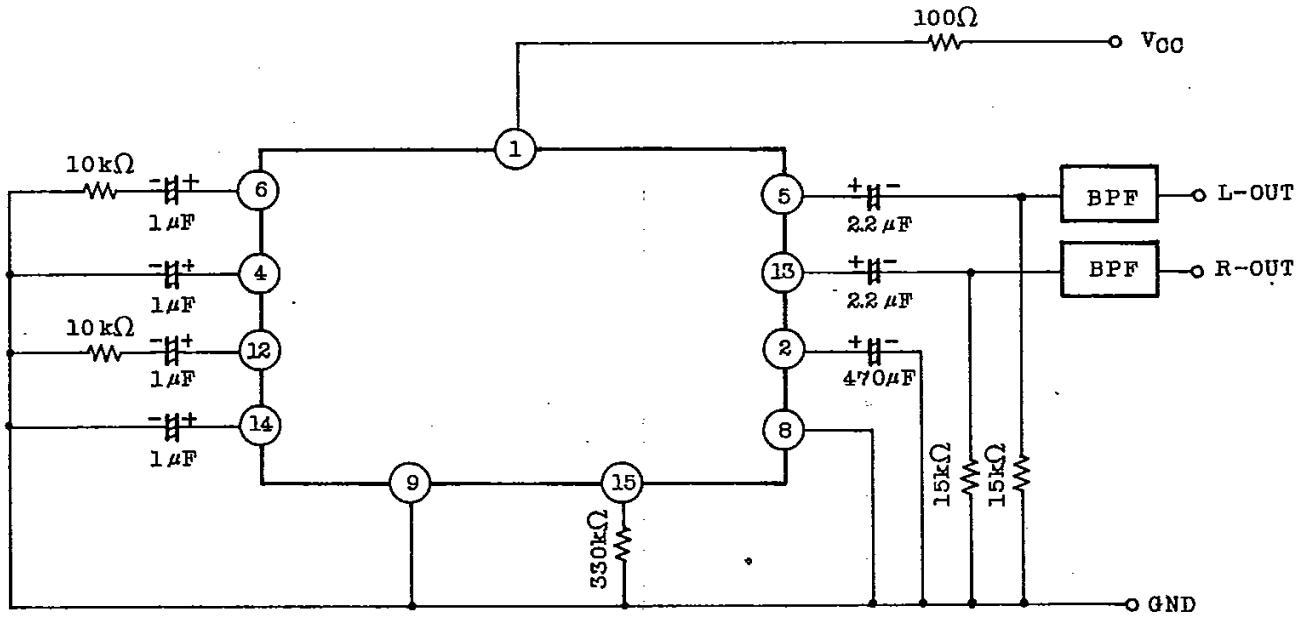
③ : OPEN

⑦⑩⑪⑮⑯ : CONNECT TO GND OR OPEN

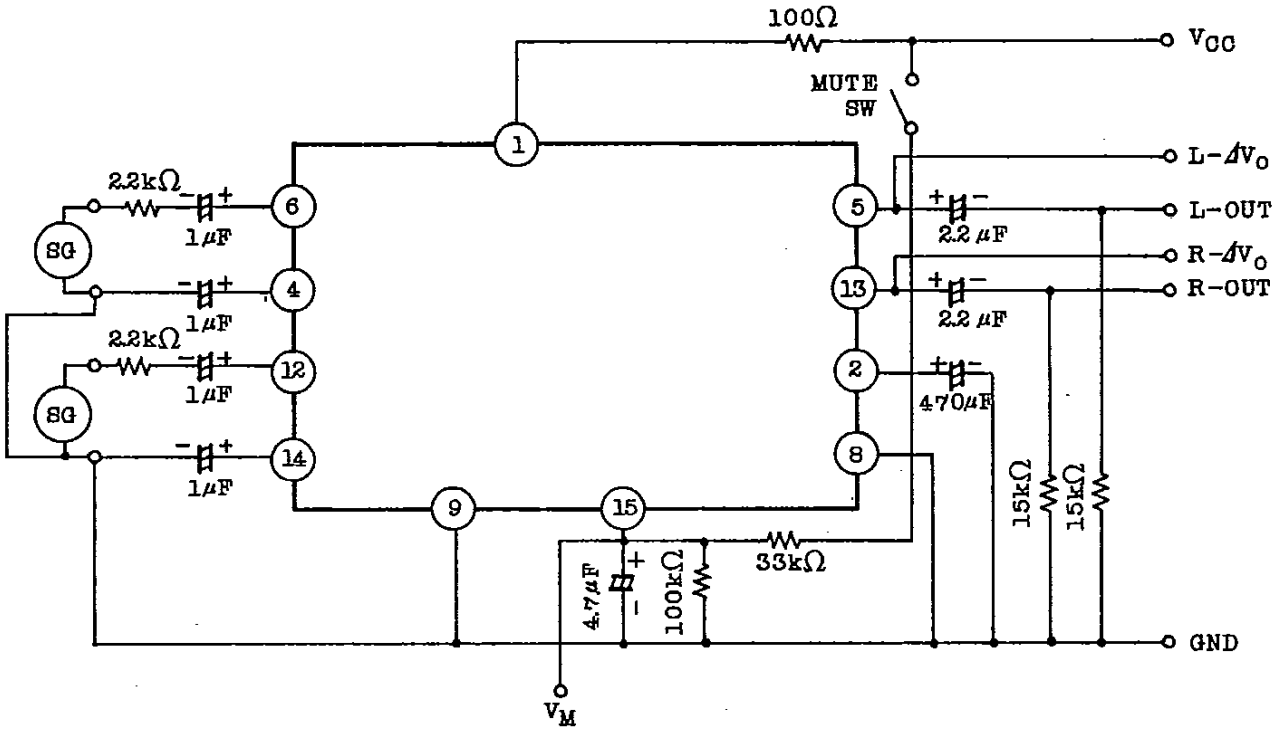
TEST CIRCUIT 1



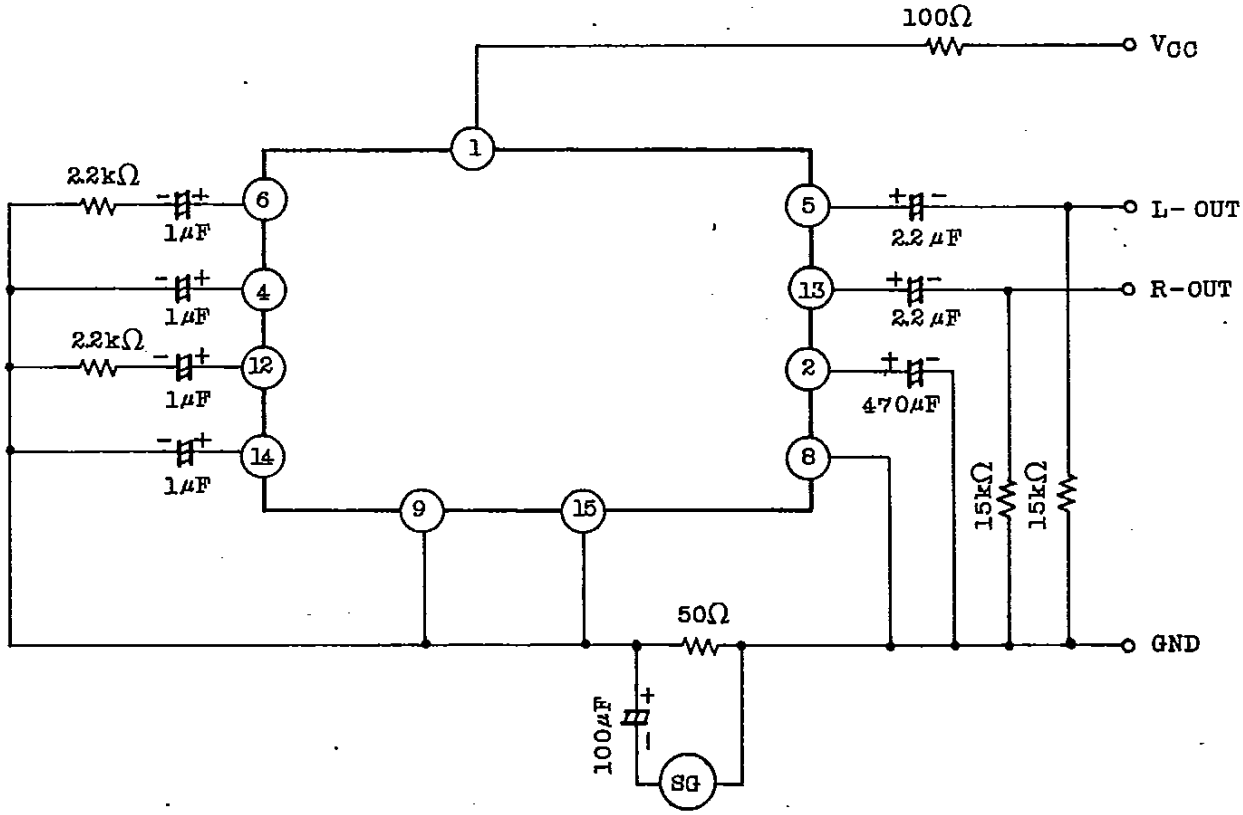
TEST CIRCUIT 2



TEST CIRCUIT 3

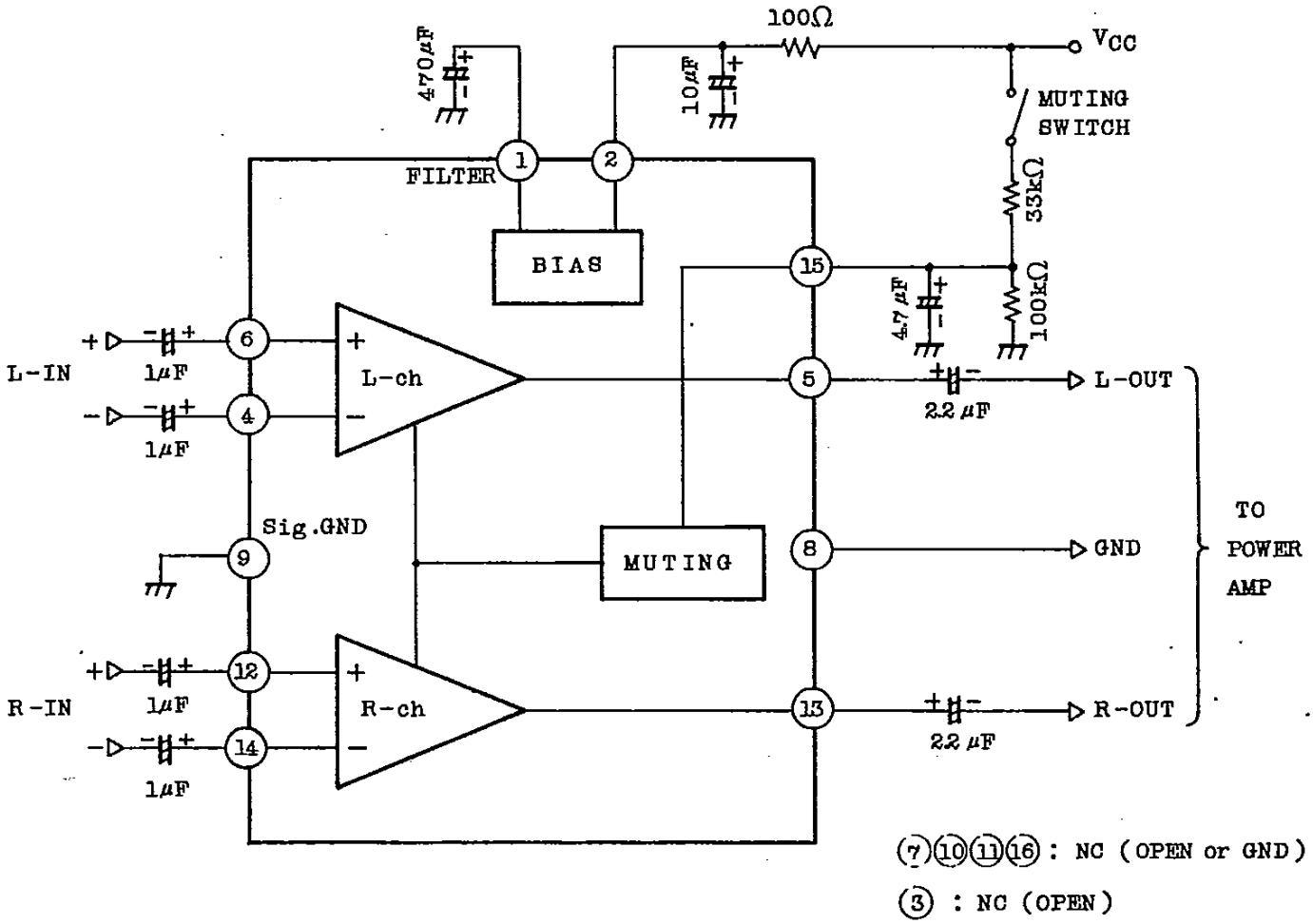


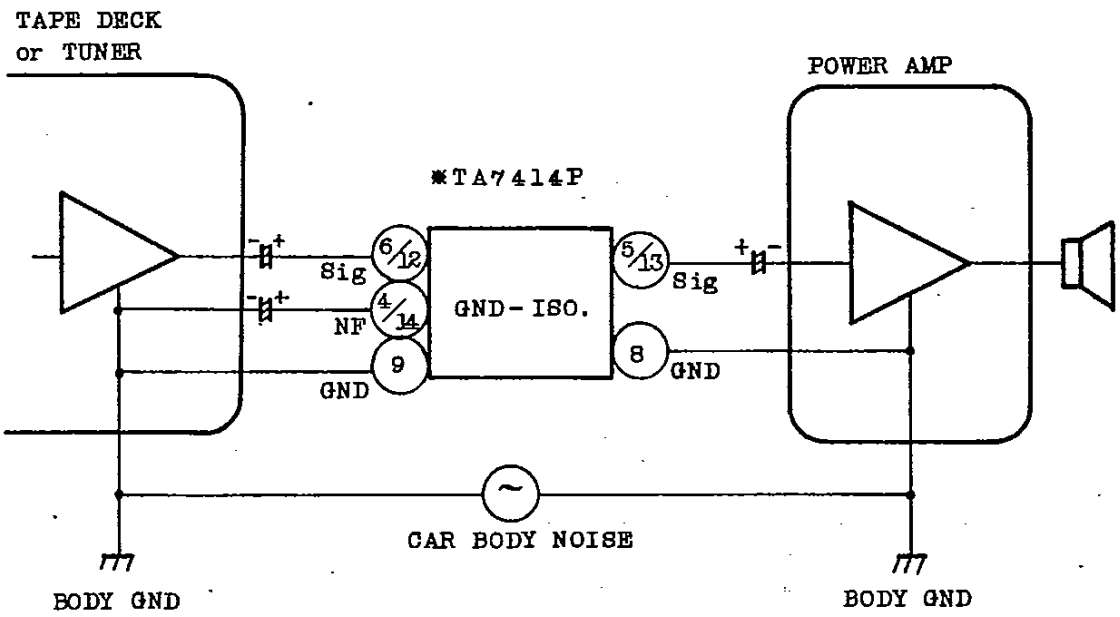
TEST CIRCUIT 4



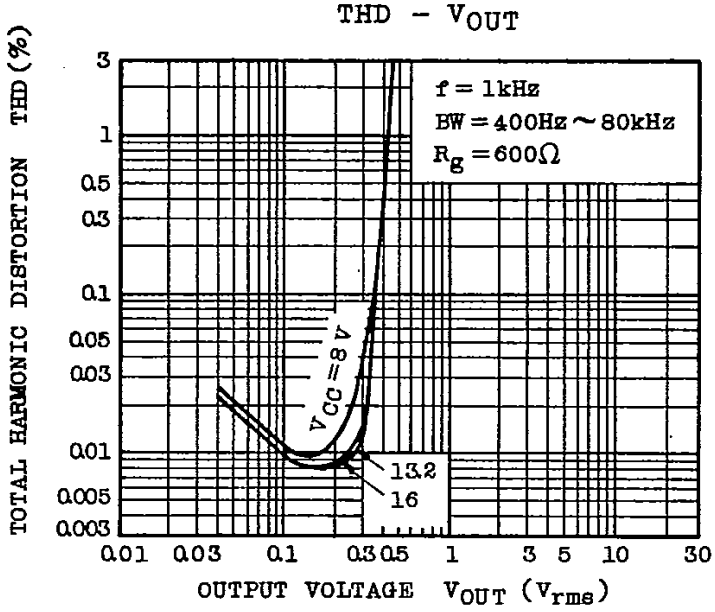
Note : ③ Pin must be open at test circuit.

APPLICATION CIRCUIT

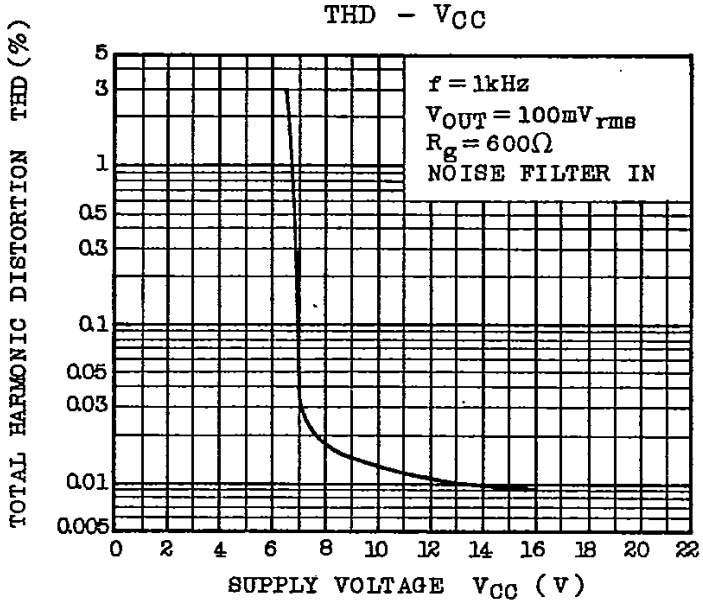




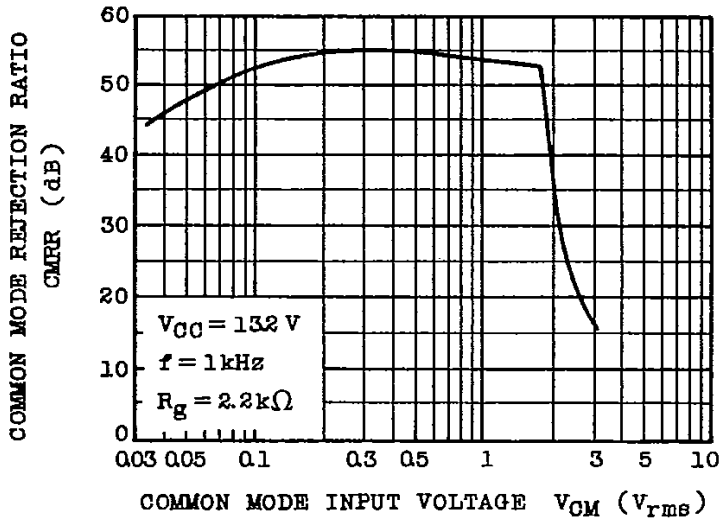
THD – V_{OUT}



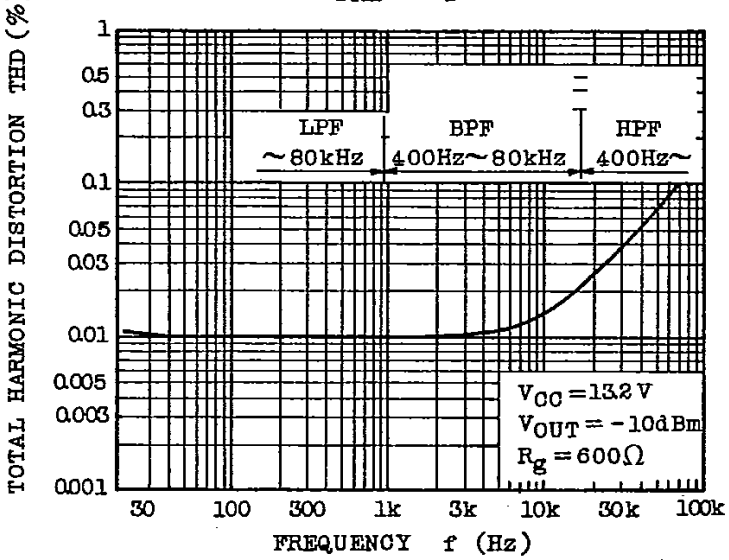
THD – V_{CC}



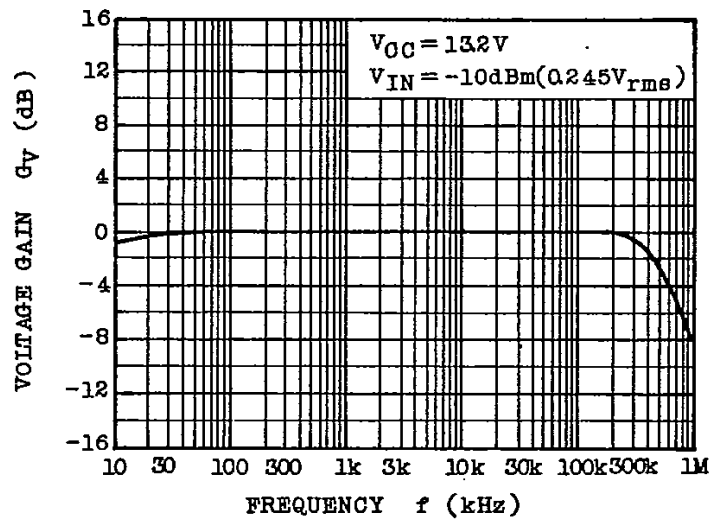
CMRR – V_{CM}



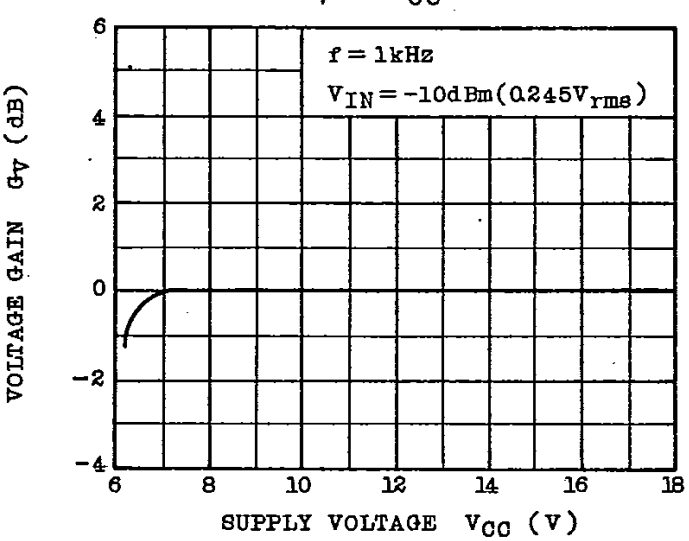
THD – f



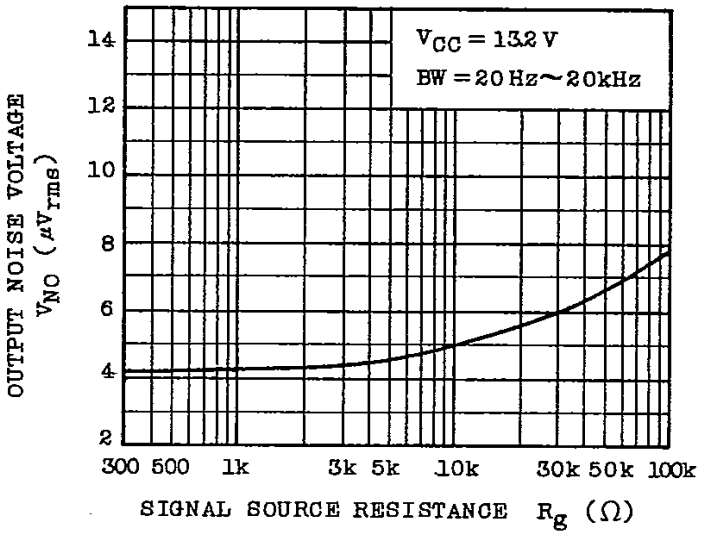
G_V – f



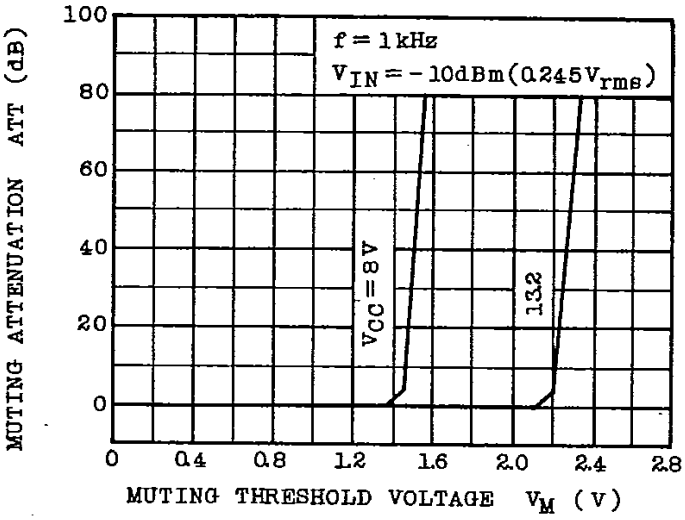
G_V – V_{CC}



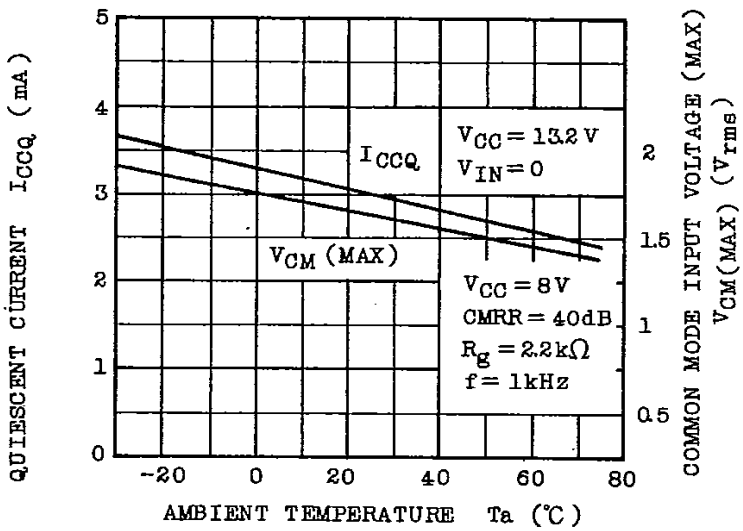
V_{NO} – R_g



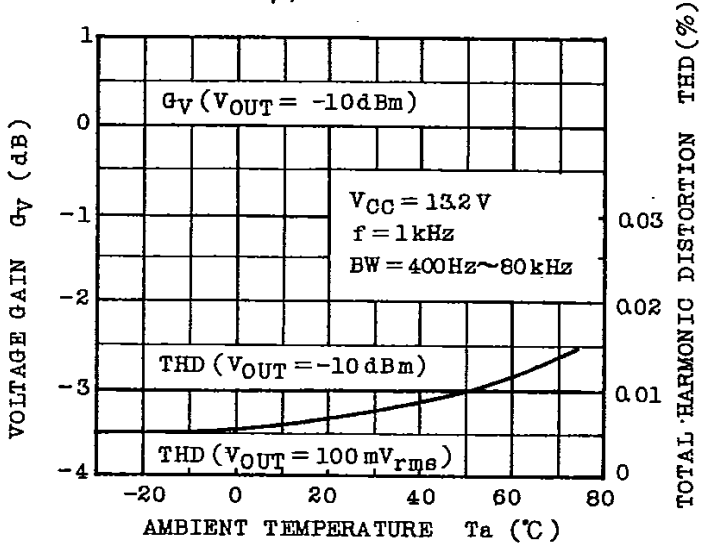
ATT – V_M



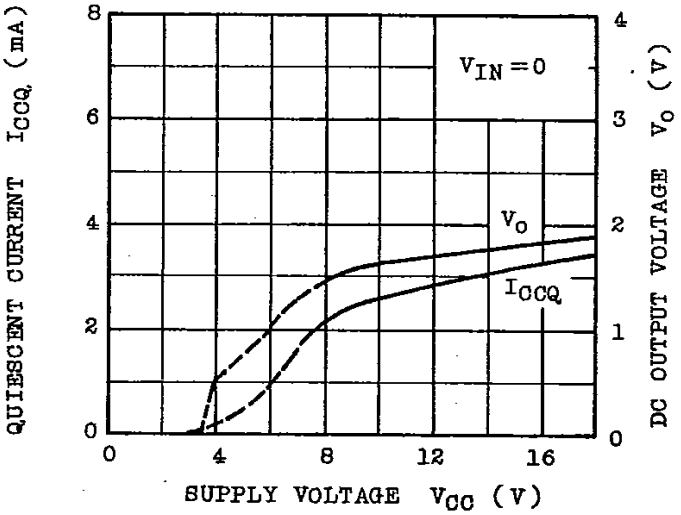
$V_{CM(MAX)}$, I_{CCQ} – Ta



G_V, THD – Ta



I_{CCQ}, V_O – V_{CC}



CMRR – Ta

