calogic
LLC

High-Speed Analog N-Channel Enhancement-Mode DMOS FETS

SD200 / SD201 / SD202 / SD203 / SSTSD201 / SSTSD203

FEATURES

- **High gain . . . . . 8.0 dB min @ 1 GHz**
- **Low Noise. . . . . 5.0 dB max @ 1 GHz**
  (SD202, SD203, SSTSD203)
  Low Interelectrode Capacitances

APPLICATIONS

- **High Gain VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

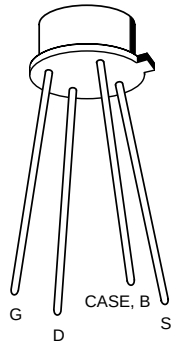
DESCRIPTION

The SD200 series is manufactured utilizing Calogic's proprietary DMOS design and processing techniques. The device is designed to operate well through 1 GHz while maintaining excellent frequency response, power gain, and low noise. The DMOS structure is an inherently low capacitance and very high speed design resulting in a device that bridges JFETS and GaAs products in performance characteristics.

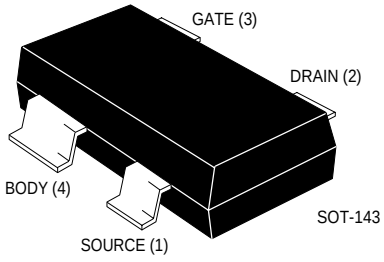
ORDERING INFORMATION

Part	Package	Temperature Range
SD200DC	4 Lead TO-52 Package	-55°C to +125°C
SD201DC	4 Lead TO-52 Package	-55°C to +125°C
SD202DC	4 Lead TO-52 Package	-55°C to +125°C
SD203DC	4 Lead TO-52 Package	-55°C to +125°C
SSTSD201	Surface Mount SOT-143	-55°C to +125°C
SSTSD203	Surface Mount SOT-143	-55°C to +125°C
XSD200	Sorted Chips in Carriers	-55°C to +125°C
XSD201	Sorted Chips in Carriers	-55°C to +125°C
XSD202	Sorted Chips in Carriers	-55°C to +125°C
XSD203	Sorted Chips in Carriers	-55°C to +125°C

PIN CONFIGURATION

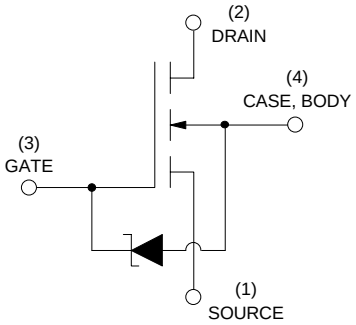


CD10-1 SD201, SD203, zener protected
CD10-2 SD202, SD204, non-zener



PART MARKINGS (SOT-143)	
P/N	**MARKING**
SSTSD201	201
SSTSD203	203

SCHEMATIC DIAGRAM



BODY INTERNALLY CONNECTED TO CASE.
DIODE PROTECTION ON SD201/SD203 ONLY.

ABSOLUTE MAXIMUM RATING (T_A = +25°C unless otherwise noted)

PARAMETER Breakdown Voltages	SD200	SD201	SD202	SD203	UNIT
V_{DS}	+25	+25	+20	+20	V
V_{DB}	+25	+25	+20	+20	V
V_{GS}	±40	-0.3	±40	-0.3	V
		+20		+20	V
V_{GB}	±40	-0.3	±40	-0.3	V
		+20		+20	V
V_{GD}	±40	-0.3	±40	-0.3	V
		+20		+20	V

I_D	Continuous Drain Current	50 mA
P_T	Power Dissipation (at or below T_C = +25°C)	1.8 W
	Linear Derating Factor	18 mW/ °C
P_D	Power Dissipation (at or below T_A = +25C)	360 mW
	Linear Derating Factor	3.6 mW/ °C
T_j	Operating Junction Temperature Range	-55°C to + 125°C
T_s	Storage Temperature Range	-65°C to +175°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

SYMBOL	PARAMETER		200, 201			202, 203			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
STATIC											
BV_{DS}	Drain-Source Breakdown Voltage		25	30		20	25		V	I_D = 1.0µA, V_{GS} = V_{BS} = 0	
BV_{DB}	Drain-Body Breakdown Voltage		25			20			V	I_D = 1.0µA, V_{GB} = 0 Source OPEN	
$I_{D(OFF)}$	Drain-Source OFF Current				1.0				µA	V_{DS} = 25 V	V_{GS} = V_{BS} = 0
								1.0		V_{DS} = 20 V	
I_{GBS}	Gate-Body Leakage Current	SD200			±0.1				nA	V_{GV} = ±40 V	V_{DB} = V_{SB} = 0
		SD202						±0.1			
		SD201			1.0				µA	V_{GB} = 20 V	
		SD203						1.0			
$V_{GS(th)}$	Gate Threshold Voltage		0.1	1.0	2.0	0.1	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 1µA, V_{SB} = 0	
$r_{DS(ON)}$	Drain-Source ON Resistance			40	70		35	50	ohms	V_{GS} = 5 V, I_D = 1 mA, V_{SB} = 0	
DYNAMIC											
g_{fs}	Common-Source Forward Transcondconductance		13	14		17	20		mS	I_D = 20 mA, V_{DS} = 15 V f = 1 KHz, V_{SB} = 0	
c_{iss}	Common-Source Input Capacitance			2.4	3.0		3.0	3.6	pF	I_D = 20 mA	V_{DS} = 15 V f = 1 MHz V_{SB} = 0
c_{oss}	Common-Source Output Capacitance			1.0	1.2		1.0	1.2		V_{GS} = 0	
c_{rss}	Common-Source Reverse Transfer Capacitance			0.2	0.3		0.2	0.3			
G_{ps}	Common-Source Power Gain		8.0	10		8.0	10		dB		V_{DS} = 15 V f = 1 GHz ID = 20 mA V_{SB} = 0
NF	Noise Figure			4.5	6.0		4.0	5.0			
P_i	Intercept Point			29			29		dBm	Δf = 2 MHz	