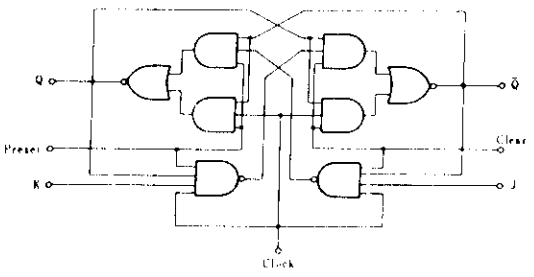
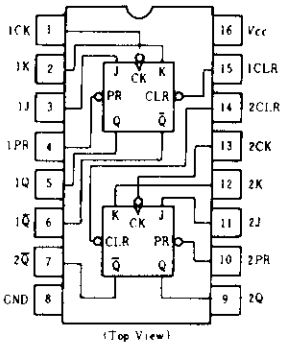
HD74LS112 ● Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

■BLOCK DIAGRAM(½)



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	30	MHz
Pulse width	Clock High	t_w	20	–		ns
	Clear, Preset Low		25	–		
Setup time	"H" Data	t_{su}	20↓	–		ns
	"L" Data		20↓	–		
Hold time		t_h	0↓	–		ns

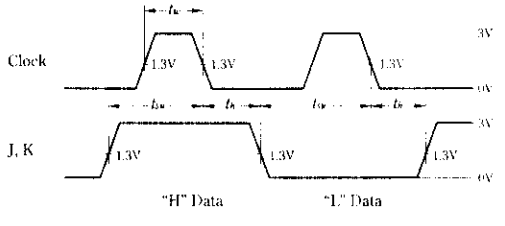
Note) ↓; The arrow indicates the falling edge.

■FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\bar{Q}_0$

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
Q_0; level of Q before the indicated steady-state input conditions were established.
$\bar{Q}_0$; complement of Q_0 or level of Q̄ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■TIMING DEFINITION



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$	–	–	0.5	V
				$I_{OL}=4mA$	–	–	0.4	
Input current	J, K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	Clear				–	–	60	
	Preset				–	–	60	
	Clock				–	–	80	
	J, K	I_{IL}**	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	Clear				–	–	−0.8	
	Preset				–	–	−0.8	
	Clock				–	–	−0.8	
	J, K	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	Clear				–	–	0.3	
	Preset				–	–	0.3	
	Clock				–	–	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25V$		–	4	8	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$
** I_{IL} should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn.
At the time of measurement, the clock input is grounded.

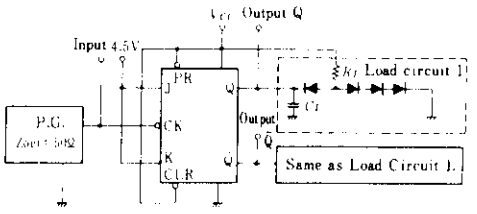
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clear Preset Clock	Q, $\overline{Q}$	$C_L=15pF$, $R_L=2k\Omega$	30	45	–	MHz
Propagation delay time	t_{PLH}				–	11	20	ns
	t_{PHL}				–	15	30	ns

■TESTING METHOD

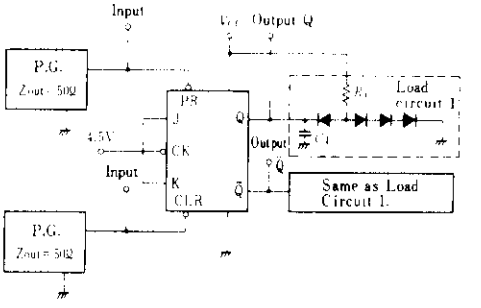
1) Test Circuit

1.1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q,$\bar{Q}$)



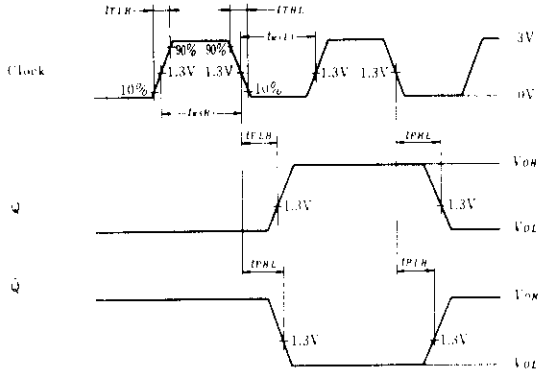
Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

1.2) t_{PHL}, t_{PLH} (Clear, Preset→Q,$\bar{Q}$)

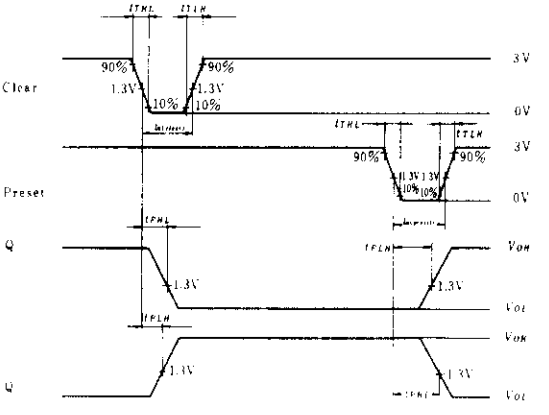


Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform

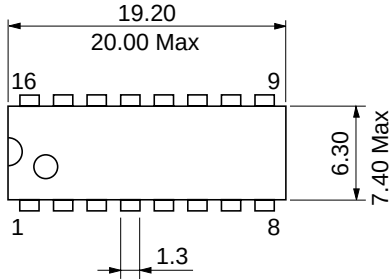


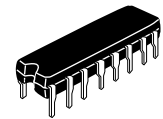
Note) Clock input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz, duty cycle=50% and: for f_{max}, t_{TLH}=$t_{THL} \leqq 2.5$ns.

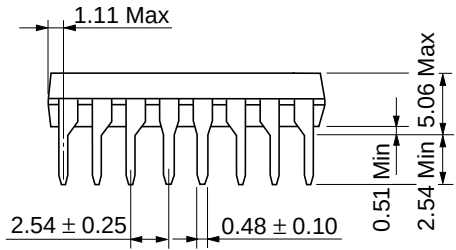


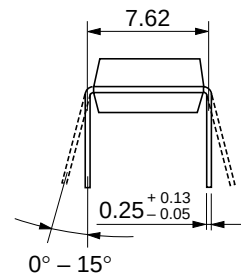
Note) Clear and preset input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz

Unit: mm



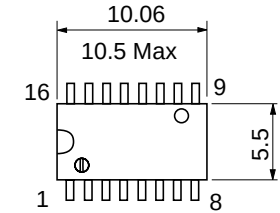


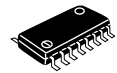


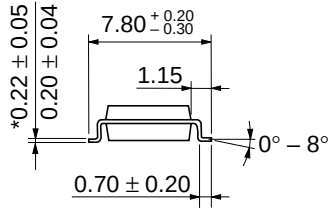


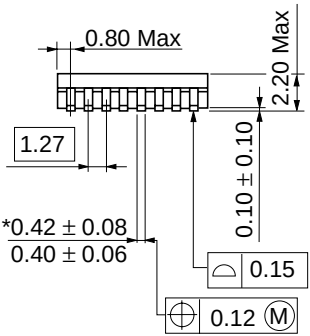
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





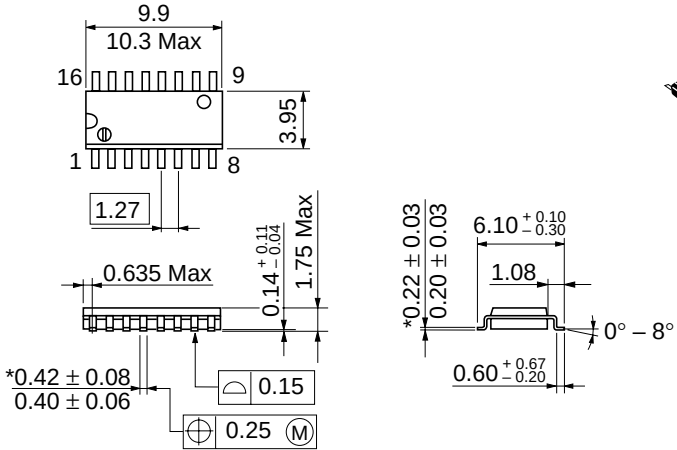


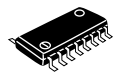


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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